RCE for Pixel Rd53 Chip Readout

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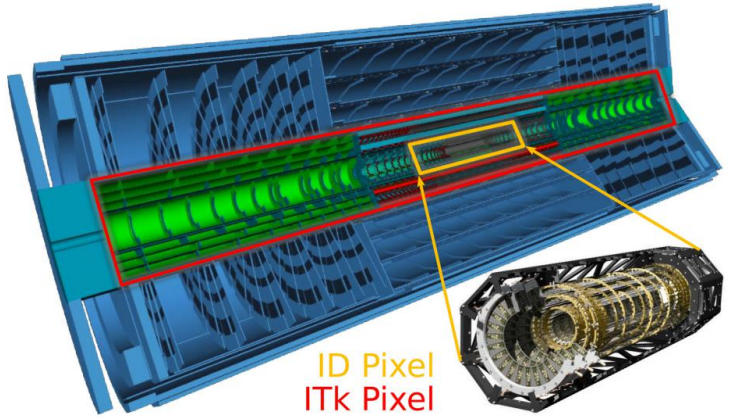
Abstract:

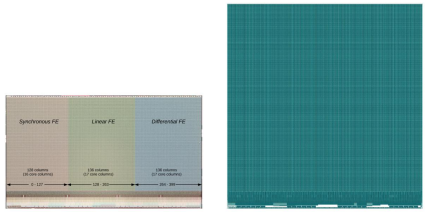
The RCE (Reconfigurable Cluster Element) platform is a general-purpose System-On-Chip data acquisition system, which is broadly deployed in various experiments, including ATLAS. A new generation of bench-top RCE system, based on Xilinx UltraScale+ MPSoC, is developed to support the Rd53a/b module and system testing with high performance. The RCE system also serves as the primary platform for validating the data transmission design of the ATLAS ITk pixel system with the same or equivalent components as the eventual ITk pixel system.

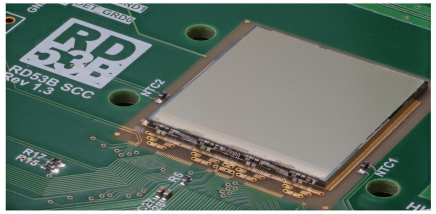
ATLAS Inner Tracker Upgrade and Pixel FE

- ATLAS ITk Upgrade, ~2025-2027
  - current Inner Detector -> all-silicon ITk
  - pixel: 1.7m^2 -> 13m^2 (5e9 channels)
  - tracking coverage η: 2.5 -> 4.0
  - trig rate: 100 kHz -> 1 MHz
  - pixel data rate increased by a factor of O(**100**)

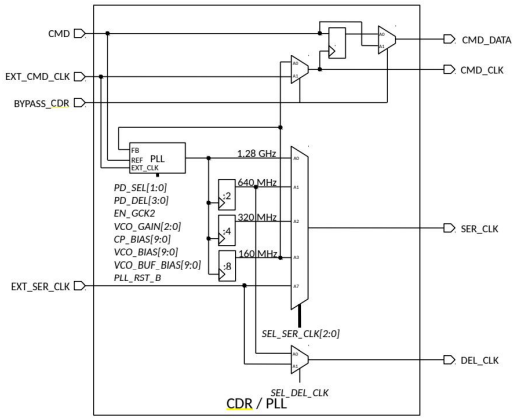


- Rd53 Front-End chip for pixel detector
  - Common design framework for the ATLAS and CMS experiments
  - chip is fully controlled with a single serial input stream
    - Lock and Data Recovery circuit (CDR) to extract clock from the 160Mbps Cmd input
  - All data, messages, and configuration read-back are output on high speed serial ports
    - up to **4x 1.28 Gbps** nominal bandwidth





ITkPixV1 chip on Single Chip Card (SCC) [3]



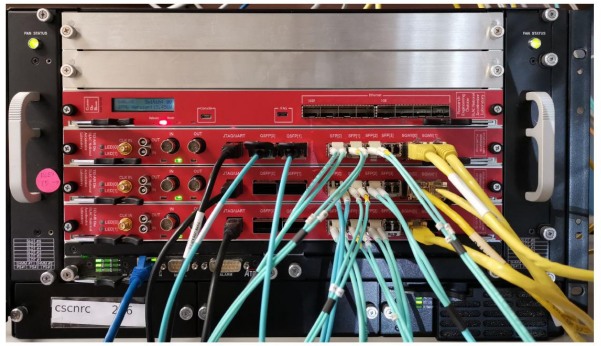
- High-performance DAQ system is critical

https://twiki.cern.ch/twiki/bin/viewauth/Atlas/RCEGen3SDK

RCE for Pixel RD53a/b readout

- RCE is broadly deployed by many experiments, such as ATLAS, HPS, ProtoDUNE and LSST
  - For example, quality assurance and control system during the construction of the recent ATLAS inner-most pixel layer, IBL(Insertable B-layer)
- New gen.: Xilinx ZCU102 board with **UltraScale+ ZYNQ** MPSoC XCZU9EG
- Custom FMC adaptor and ATCA system (blade+RTM) to direct run RD53a/b
  - FMC adaptor and ATCA system follow same design
  - **SelectIO HP** pins for 160Mbps Cmd and 1.28Gbps data
  - Retimer (industrial ICs: 160MHz clock, PLL, and flip-flop) on the FMC/RTM to reduce Cmd stream random jitter to ~**2ps**
  - adjustable Cmd pre-emphasis and data equalizer ICs for lossy data transmission chain

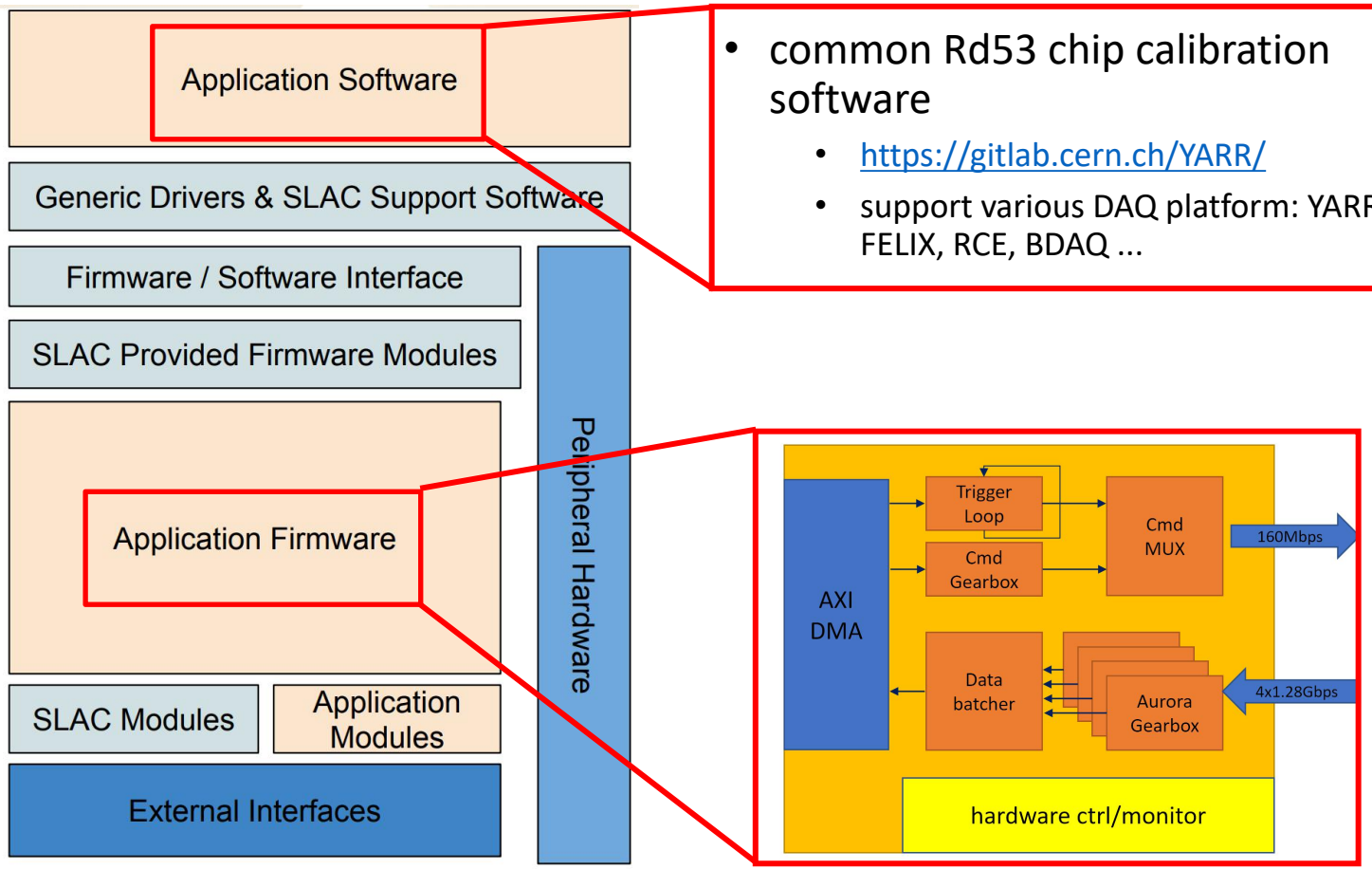
Front: 10G optical fiber to back-end DAQ system



Back: miniDP cable interface to pixel detector

RCE Software & Firmware Development

- common FW&SW library to support various DAQ interface/format/protocols
- Hardware Abstraction SW library
  - Rogue: https://github.com/slaclab/rogue
  - Python bindings for rapid DAQ prototyping and GUIs, can be configured for pure C++ use
- FW building blocks for a wide range of Xilinx FPGAs/SoCs (RCE like, PCIe cards)
  - https://github.com/slaclab/rce-gen3-fw-lib
  - example: https://github.com/slaclab/rce-gen3-fw-examples
  - Ruckus: Vivado Build System based on Makefiles, https://github.com/slaclab/ruckus
- RCE Advantage: CPU embedded in FPGA fabric with direct access to I/O ports and firmware resources



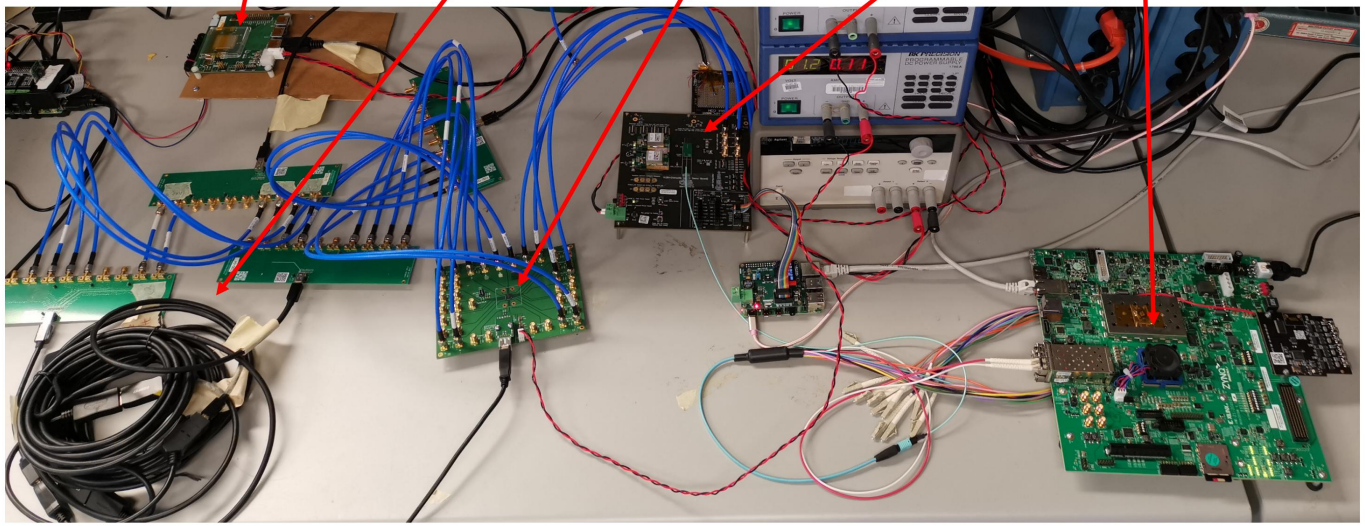
RD53(ITkPixV1) Data Transmission chain Test

- Sending high volume of data from ITk pixel detector to DAQ is difficult
  - balance between data transmission bandwidth, stability, and material usage is required
  - radiation level near the beam pipe prevent the placement of optical components close to the pixel chips
- data transmission within ITk detector volume is a combination of flex and **TwinAx** links
  - signal is carried to larger radii for optical conversion
- **A demonstration system** stably runs at the design rate of 1.28 Gb/s, with measured BER<1e-12
  - ITk pixel system data transmission design is validated with equivalent components as the eventual system

A. Young: Radiation hard TwinAx for ATLAS ITk pixel electrical data transmission

https://indico.cern.ch/event/1019078/contributions/4444263/

ITkPixV1 + cables + GBCRv2 + lpGBTv0 + DAQ

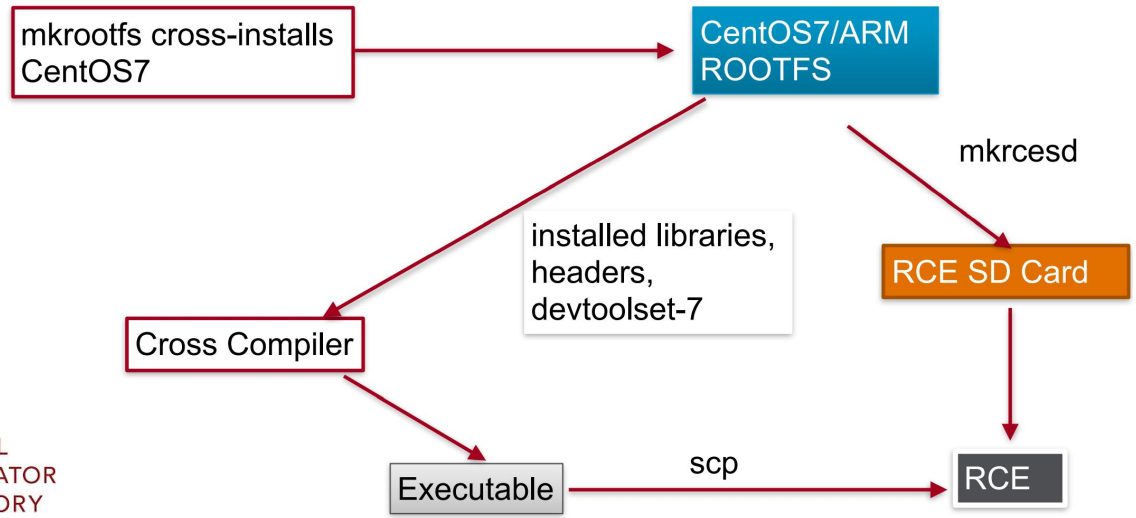


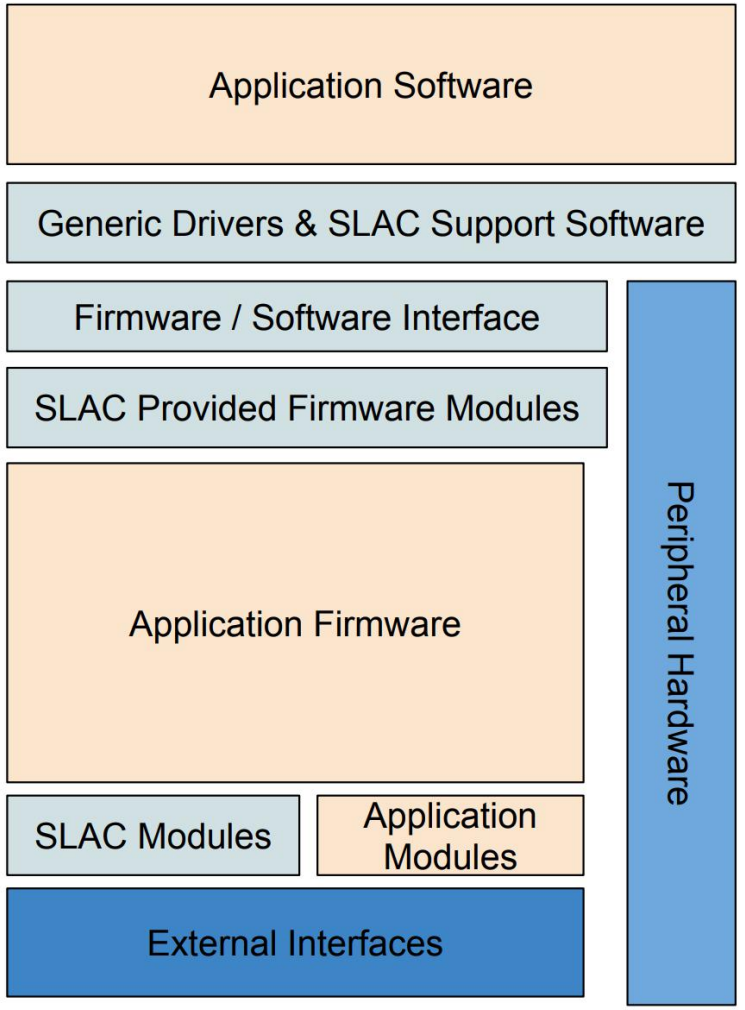
- ITkPix is ATLAS version Rd53b
- cables to emulate the flex, twinax and interface PCBs with -20dB @640MHz signal loss
- GBCRv2 for rx-equalizing
- lpGBT/VTRx+ for data aggregation and optical conversion

Backup

RCE Software Framework

- Operating Systems:
  - **CentOS7:** 64bit for ZCU102, 32bit for RCE gen-3 (COB and HSIO2)
  - Arch Linux(abandoning), RTEMS without SMP support (abandoned)
  - Ubuntu LTS might be an option for next version ARM OS
- RCE Software Development Kit
  - host OS: CentOS7 x86/64
  - format and install root file system to SD card
  - Crosstool-ng to generate cross compilers for ARM and AARCH64





What is RCE(Reconfigurable Cluster Element)

Design of the SLAC RCE Platform: A general purpose ATCA based data acquisition system

Publisher: IEEE | Cite This | PDF

14 Author(s) R. Herbst ; R. Claus ; M. Freytag ; G. Haller ; M. Huffer ; S. Maldonado ; K. Nishimura ; C. O'Grady ; J. Pa… View All Authors

1 Paper Citation
125 Full Text Views

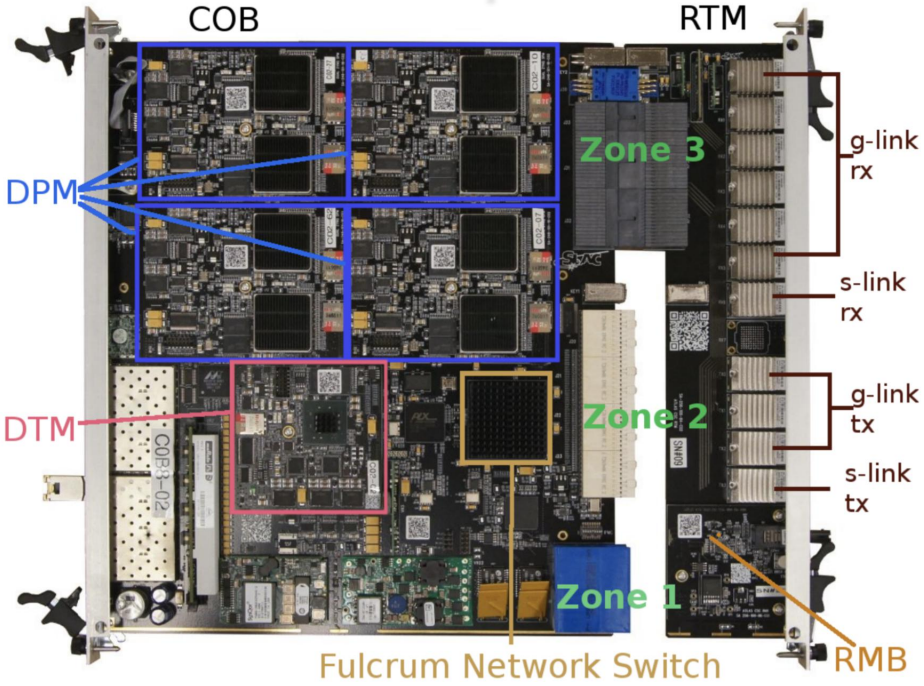
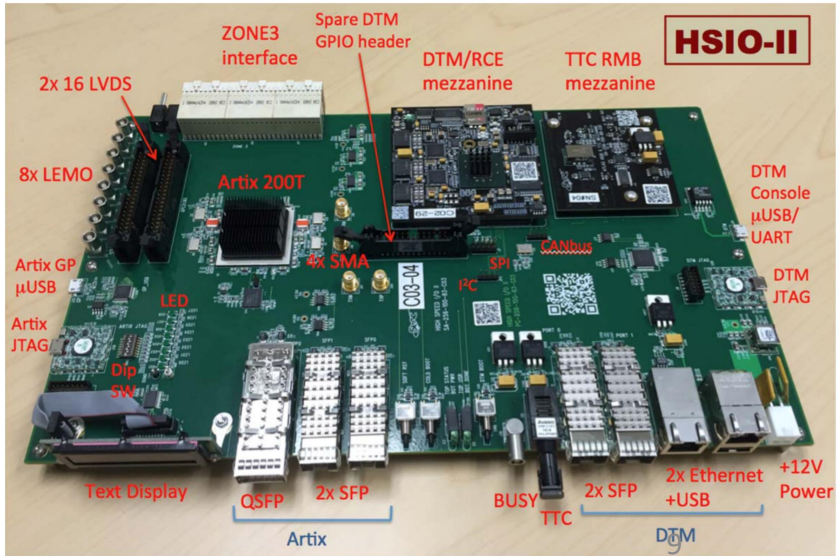
Abstract

Document Sections

I. Introduction
II. RCE Platform Architecture
III. Packaging and Dataflow

Abstract:
The SLAC RCE platform is a general purpose clustered data acquisition system implemented on a custom ATCA compliant blade, called the Cluster On Board (COB). The core of the system is the Reconfigurable Cluster Element (RCE), which is a system-on-chip design based upon the Xilinx Zynq family of FPGAs, mounted on custom COB daughter-boards. The Zynq architecture couples a dual core ARM Cortex A9 based processor with a high performance 28nm FPGA. The RCE has 12 external general purpose bi-directional high speed links, each supporting serial rates of up to 12Gbps. 8 RCE nodes are included on a COB, each with a 10Gbps connection to an on-board 24-port Ethernet switch integrated circuit. The COB is designed to be used with a standard full-mesh ATCA backplane allowing multiple RCE nodes to be tightly interconnected with minimal interconnect latency. Multiple shelves can be clustered using the front panel

https://ieeexplore.ieee.org/document/7431254

Old Gen RCE SoC Readout

- Reconfigurable Cluster Element (RCE) is a SLAC R&D project for a generic SoC DAQ/trigger system, starting from 2007
  - CPU and FPGA fabric within a same chip for a compact data passage
  - tight coupling between firmware and software
- Gen 3 (2013) based on Zynq-7000 SoC
  - **COB** (Cluster-On-Board): ATCA blade with custom RTM specialized for user applications, up to 4 DPMs and 1 DTM
  - **HSIO2**: standalone bench-top readout board, 1 DTM
  - RCE mezzanine card:
    - **DPM** (Data Processing Modules) and **DTM** (Data Transmission Module, network connectivity)
    - Xilinx Zynq-based SoC, multi-core ARM CPU, GB of memory, DMA interface to FPGA fabric, Versatile high/low-speed I/O interface