Contribution ID: **172** Type: **Poster**

New Generation RCE system for the Rd53 Pixel Front End chip readout

Tuesday, 21 September 2021 18:00 (2 minutes)

The RCE (Reconfigurable Cluster Element) platform is a general-purpose system-on-chip data acquisition system, which is broadly deployed in various experiments, including ATLAS. A new generation of bench-top RCE system, based on Xilinx UltraScale+ MPSoC, is developed to support the Rd53a/b module and system testing with high performance. The RCE system also serves as the primary platform for validating the data transmission design of the ATLAS ITk pixel system with the same or equivalent components as the eventual ITk pixel system.

Summary (500 words)

The RCE (Reconfigurable Cluster Element) platform is a general-purpose system-on-chip data acquisition system, varying from a compact standalone bench-top form to ATCA compliant system. It is broadly deployed by several experiments, such as ATLAS, HPS, ProtoDUNE and LSST. Especially, the RCE was used as the platform for quality assurance and control system during the construction of the ATLAS inner-most pixel layer, IBL(Insertable B-layer).

In this work, we present the new generation bench-top RCE system, based on Xilinx UltraScale+ MPSoC Evaluation board ZCU102. A custom FMC adaptor card successfully runs Rd53a and ITkPixV1(Rd53b), which is used by ATLAS and CMS phase 2 pixel upgrades, at full speed. With industrial ICs, this card delivers ultra-low jitter (< 4ps random-jitter) with pre-emphasis for the Cmd at 160 Mb/s which cannot be run from an FPGA MGT directly. Rx data equalizing is also provided in the FMC card. These features are essential for the lossy transmission chain. Following the design of the FMC card, an ATCA blade and RTM is produced to read out a large number of Rd53 chips. This ATCA blade emulates the lpGBT functionalities with a large FPGA to aggregate the frontend 1.28Gb/s data links to 10Gb/s optical links for backend readout. Well-designed firmware and software are essential for a high-performance readout and calibration system. Raw data de-compressing by FPGA for Rd53b can improve chip calibration performance by a factor of 5. The ARM NEON SIMD(Single instruction multiple data) libraries can boost data processing speed by a factor of 3. Moreover, a look-up-table S-curve fitting engine reduces the fitting time by a factor of 10 for threshold scan. All the performance improvements allow the RCE system to take full advantage of the high output bandwidth (5.12Gbps) of the Rd53.

The RCE system also serves as the primary platform for validating the data transmission design of the ATLAS ITk pixel system, which is one of the most challenging tasks of the ATLAS Phase-2 upgrade. Up- and downlink communication from DAQ to the ITk periphery is foreseen to be largely optical and expected to be realized with lpGBT and VTRx+ ASICs. Radiation levels close to the beam pipe prevent the placement of optical components close to the readout chips such that the first stage of transmission within ITk volume, up to 6m in length, with a combination of flex and twinax electrical links to carry signals to larger radii for optical conversion. A balance between data transmission bandwidth, stability, and material usage is required. A demonstration system is composed of an ATLAS ITkPixV1 chip, passive electrical links and interface PCBs with -20dB@640MHz signal loss, connecting to the opto-conversion stage that consists of a custom signal equalizer chip, GBCRv2, and lpGBT/VTRx+ for data aggregation and optical conversion. This whole data transmission chain is readout with RCE DAQ via optical link. This system stably runs at the design frontend data speed of 1.28 Gb/s, with measured BER<1e-12. The ITk pixel system data transmission design is validated with equivalent components as the eventual system.

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Session Classification: Posters Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience