Installation, integration, and first operating experiences of the ALICE ITS Upgraded Readout System

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on behalf of the ALICE Collaboration

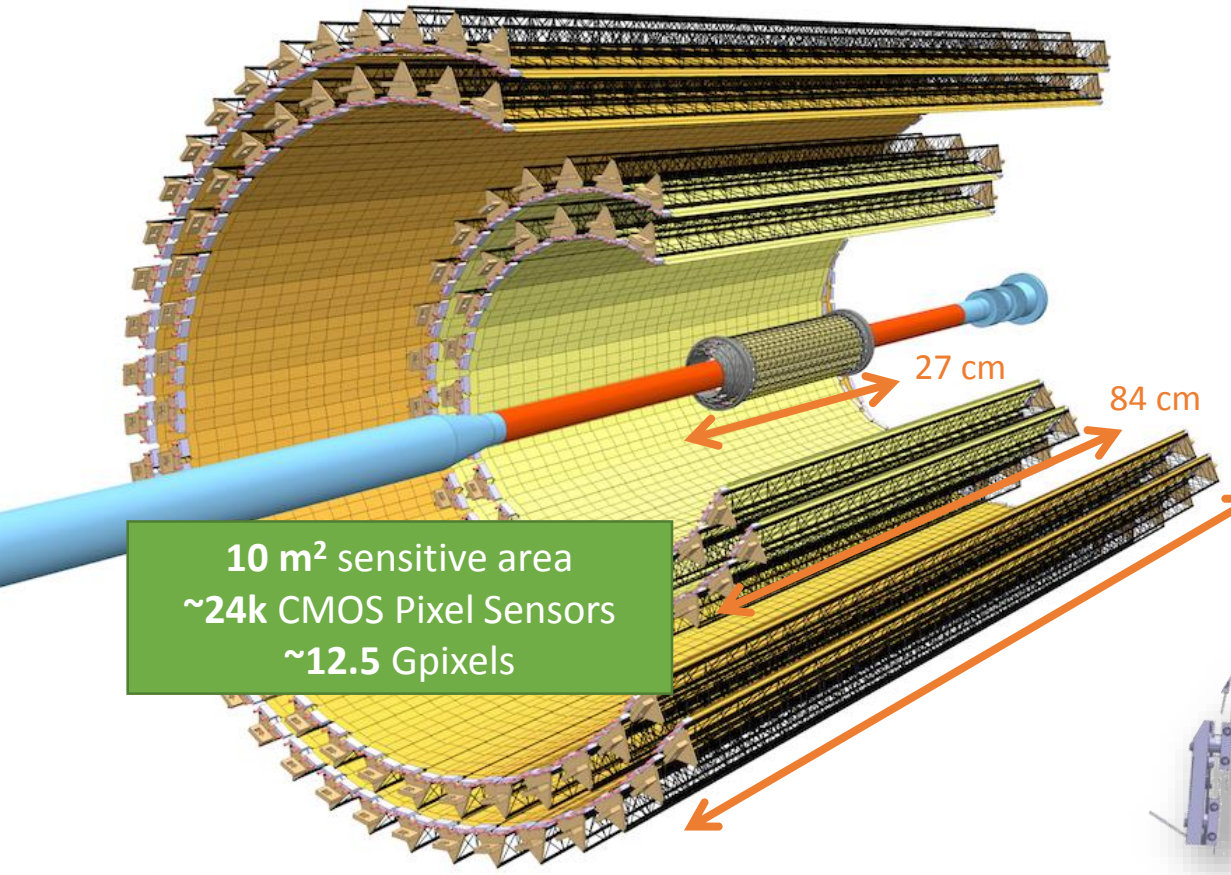
21st September 2021

TWEPP 2021 - Topical Workshop on Electronics for Particle Physics

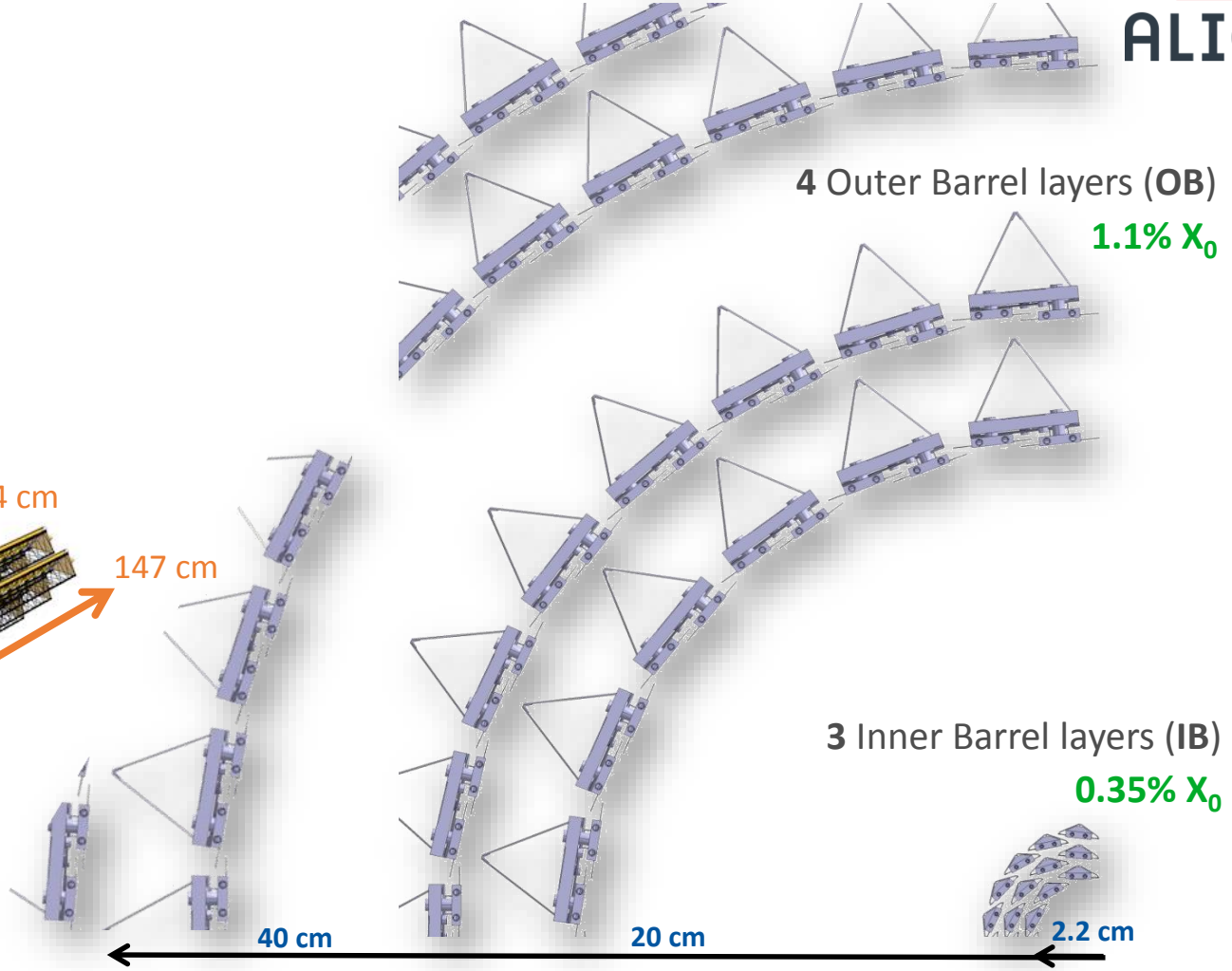
Outline

- Installation of the detector and the readout system
- Commissioning and first experience with the systems in the final configuration
- Challenges, issues and selected lessons

ALICE ITS Upgrade Detector Layout



10 m² sensitive area
~24k CMOS Pixel Sensors
~12.5 Gpixels



4 Outer Barrel layers (**OB**)
1.1% X_0

3 Inner Barrel layers (**IB**)
0.35% X_0

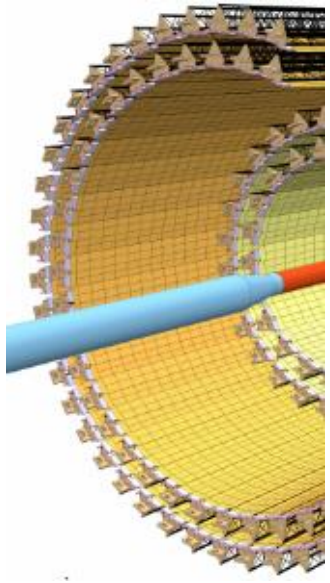
# STAVES:	**192**	48	42	30	24	20	16	12
# CHIPS:	**24120**	9408	8232	3360	2688	432		

ITS System Overview

ALICE

ALICE *Miniframe*

Inside the magnet



624 Data Cables
Twinax, Copper, ~7 m

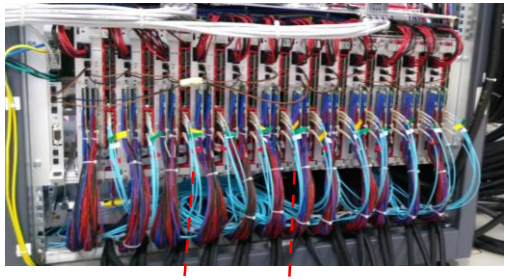
Outer Layer

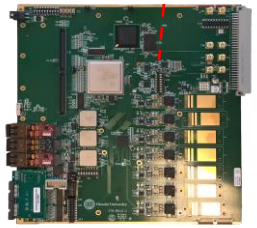
CLK, CTRL
DATA 28×400 Mb/s

Inner Layer

CLK, CTRL
DATA 9×1200 Mb/s

PP1 = 16 electronics subracks





One READOUT UNIT
for each *STAVE (**192**)*

960 GBT LINKS
576 Upstream
384 Downstream

3200Mb/s

282 Detector Power Cables

POWER BOARDS **(144)**

PP0 Patch Panel 0

Service *Power* Cables **(496)**

Service *Sense* Cables **(272)**

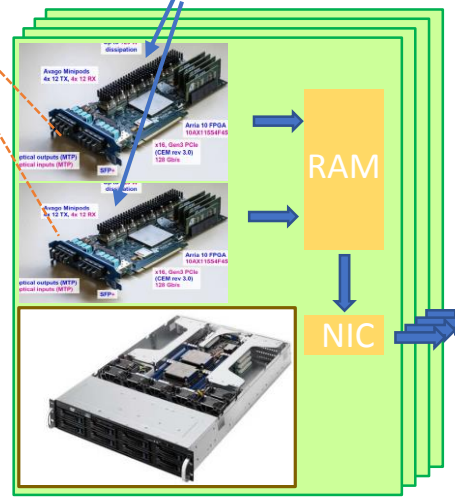
Power System – CAEN
12 A3486, 13 Easy Crates
61 A3009, 732 channels

Central Trigger Processor

192 GBT LINKS
Timing/Trigger

624 GBT LINKS
192 control
192 control/data
240 data

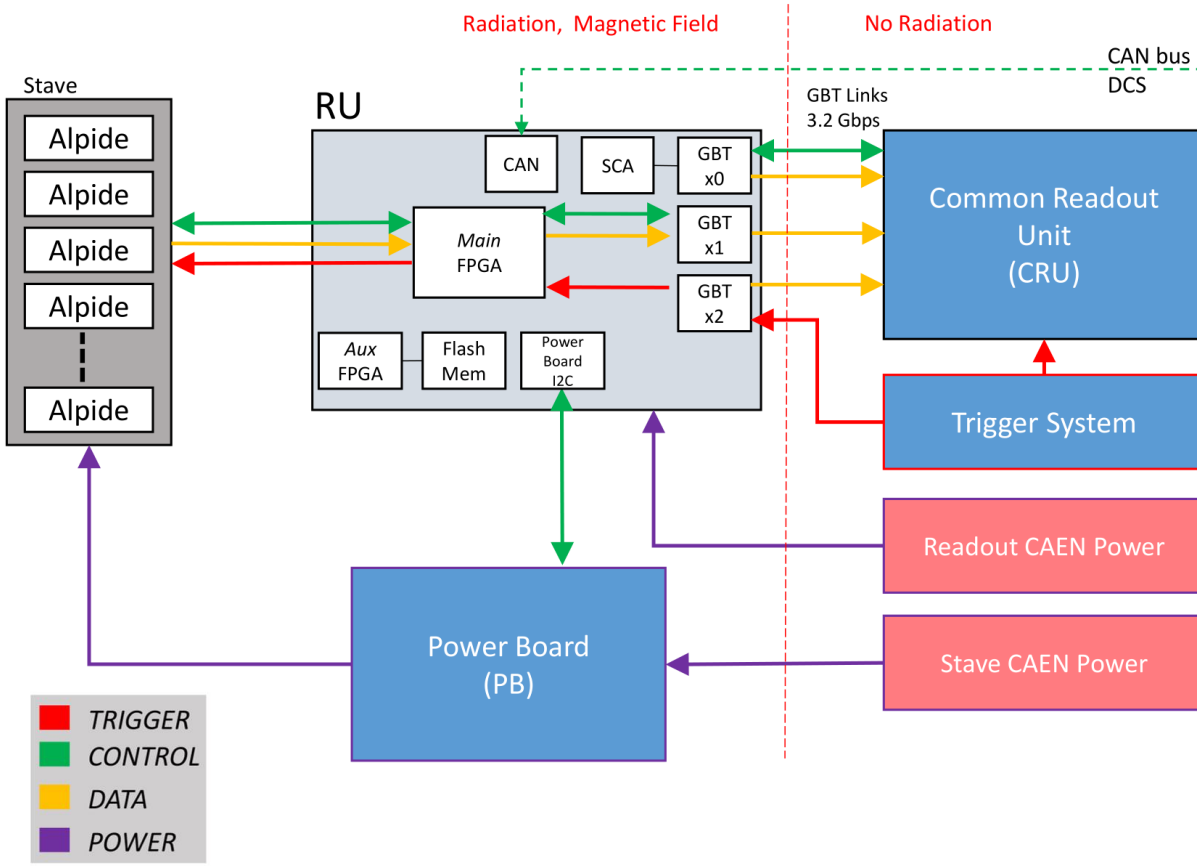
Common Readout Unit (CRU)

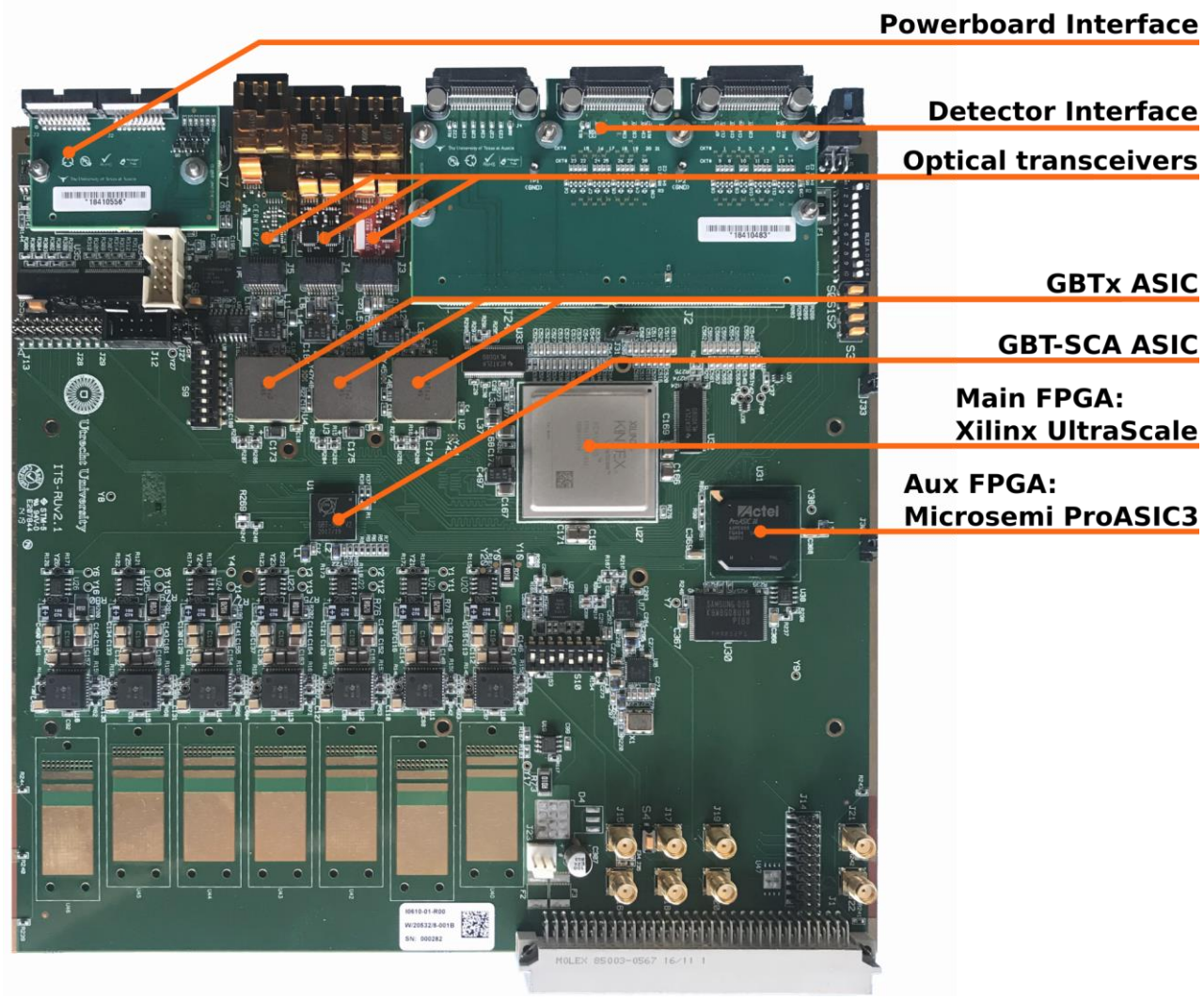


Event Building Farm

11x First Level Processors (FLP)

ITS Readout Unit

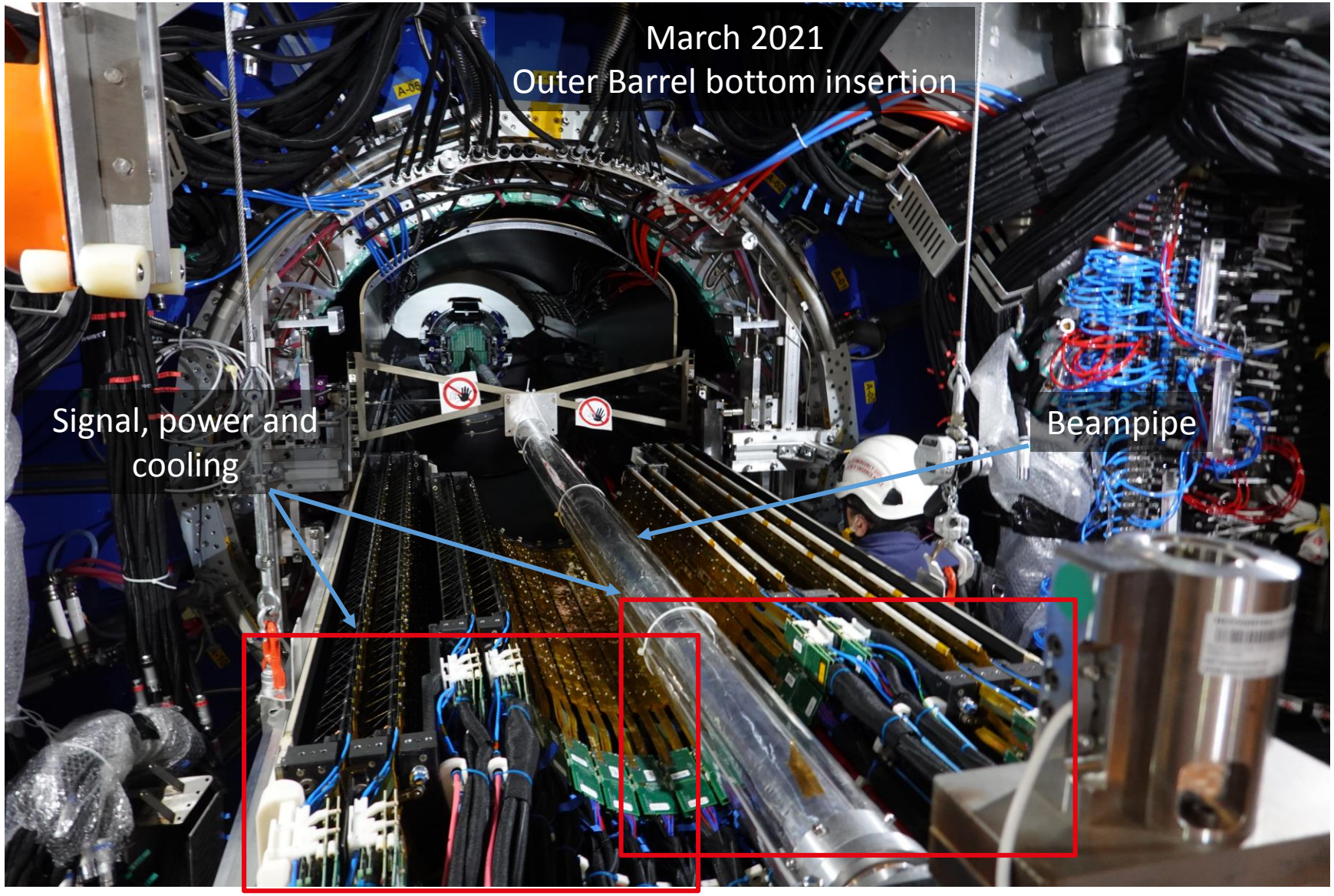




Detector and System Installation

ALICE ITS2 - Installation

ALICE ITS2 - Installation



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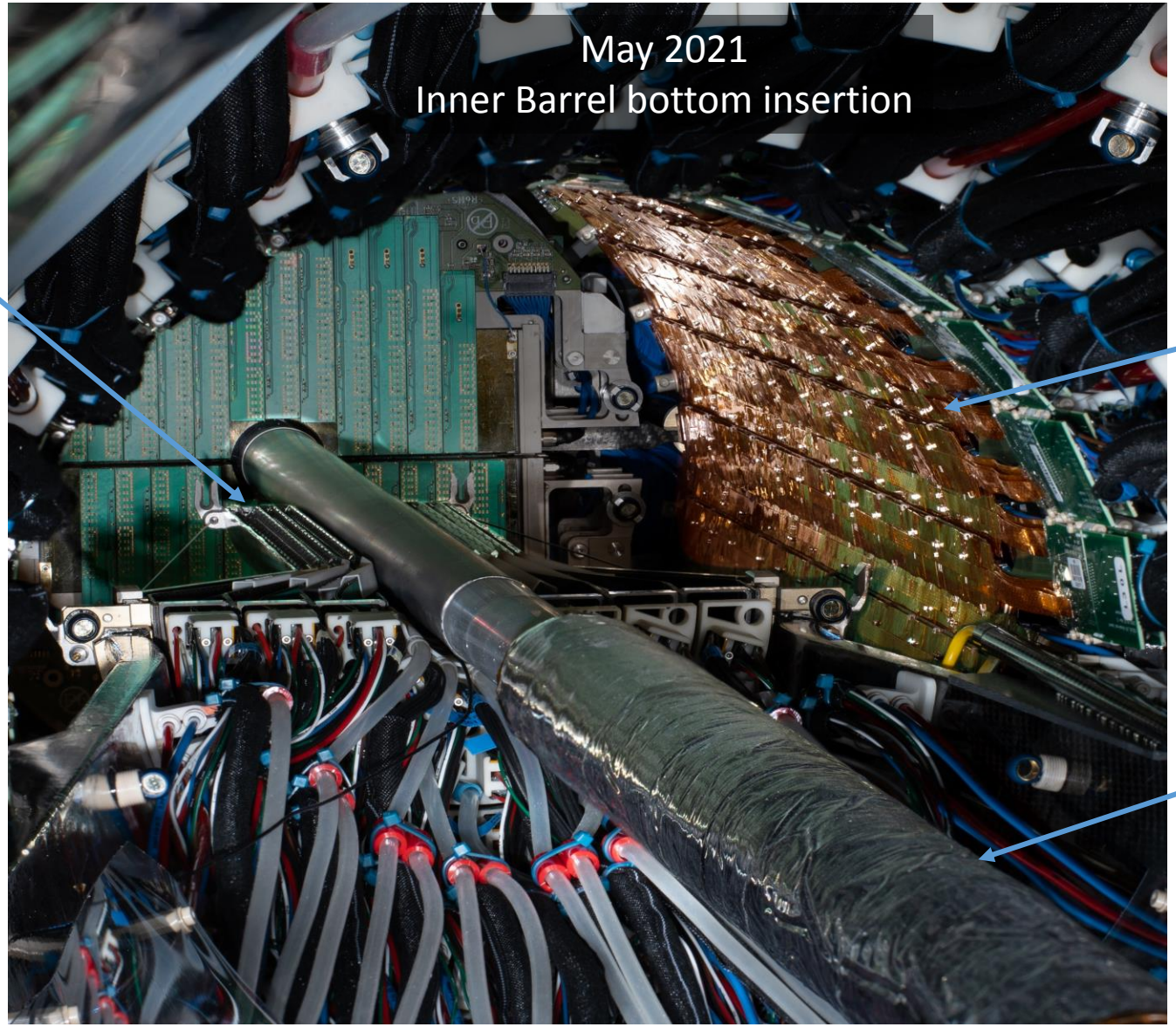

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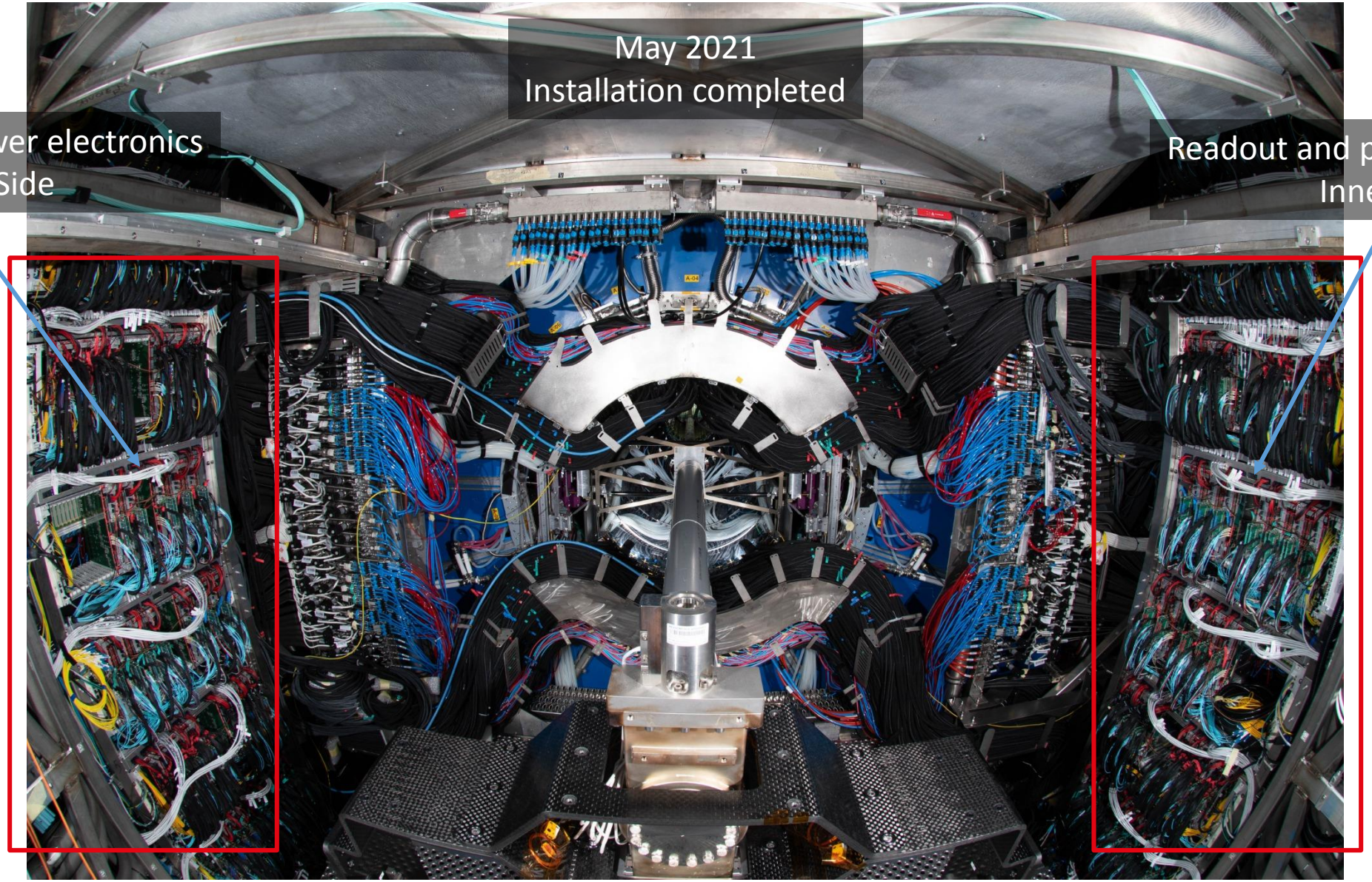
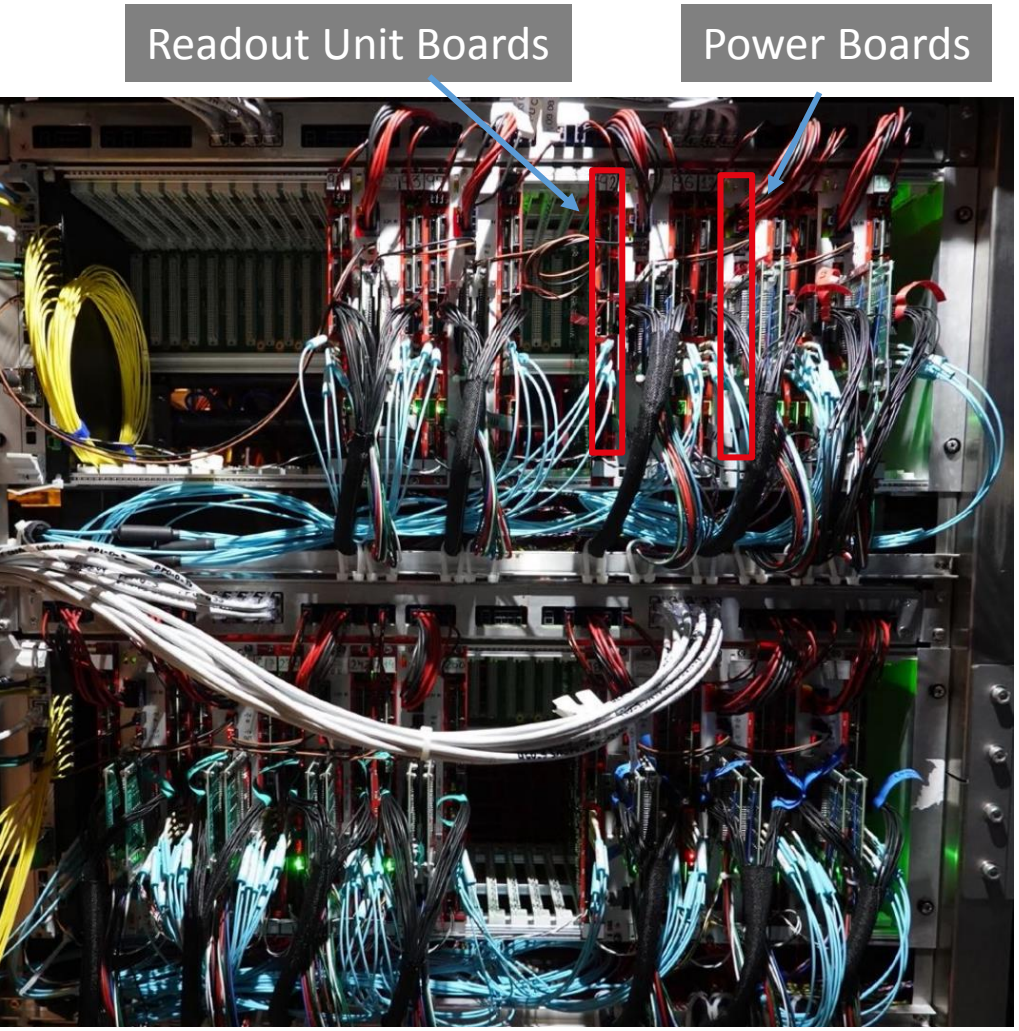
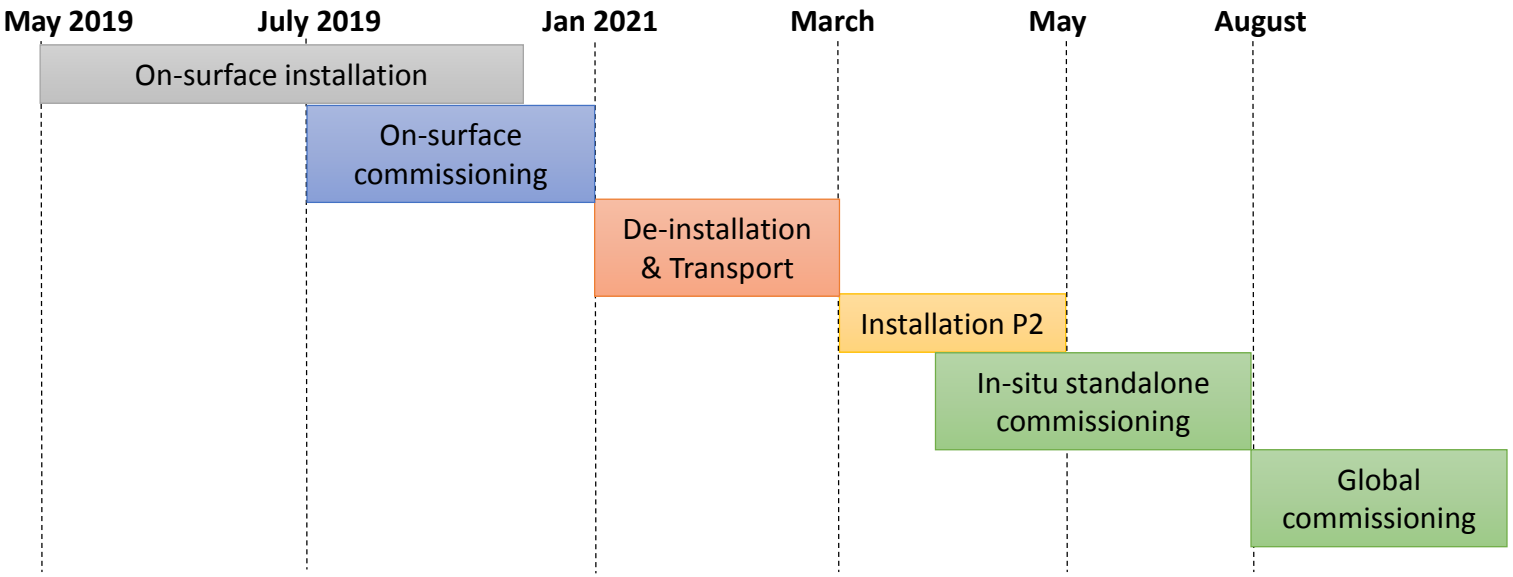


Integration and Commissioning

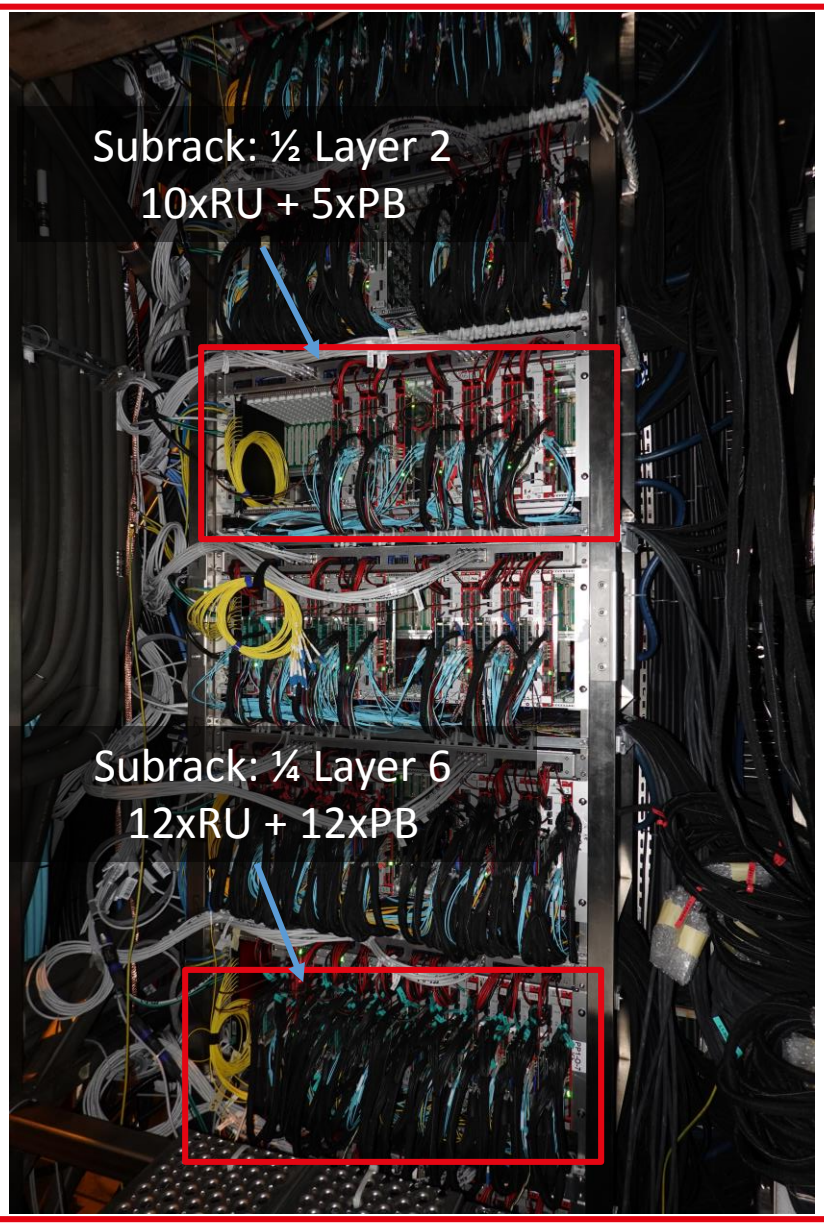
Readout Electronics - Integration and commissioning



- On-surface commissioning
- In-situ commissioning
- **Detector validated post installation**
- Gradual increase of integration complexity



Readout Electronics - Integration and commissioning



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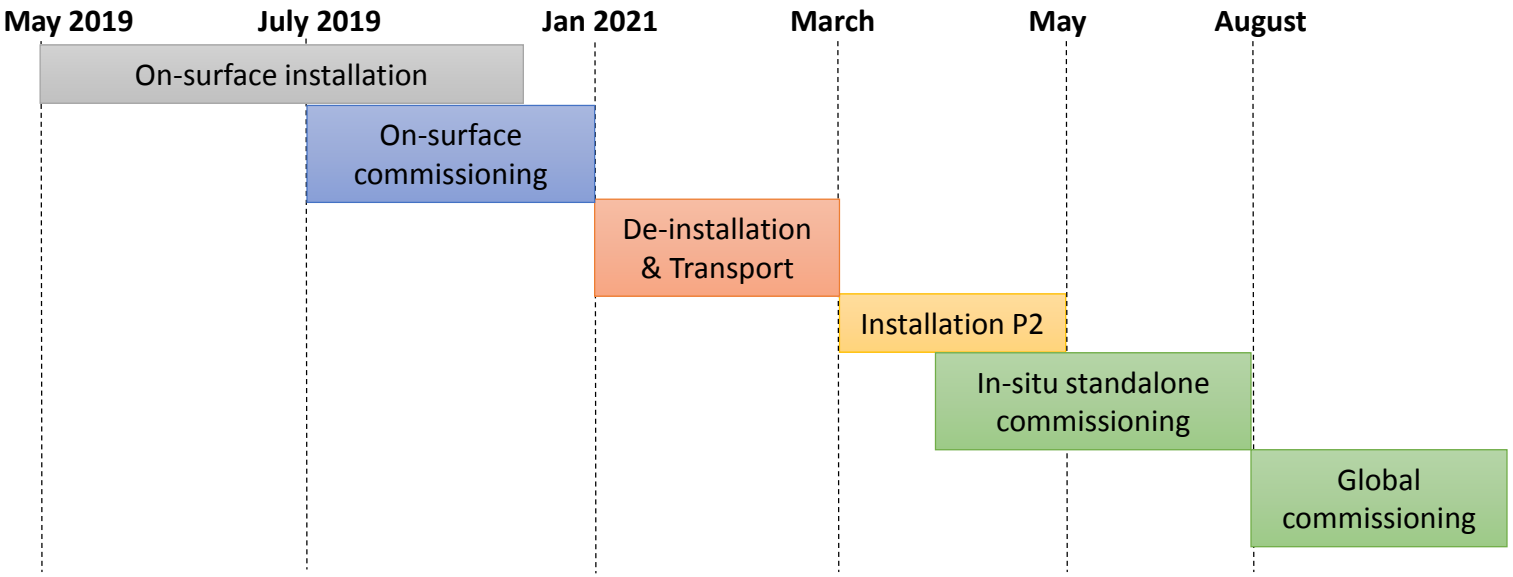
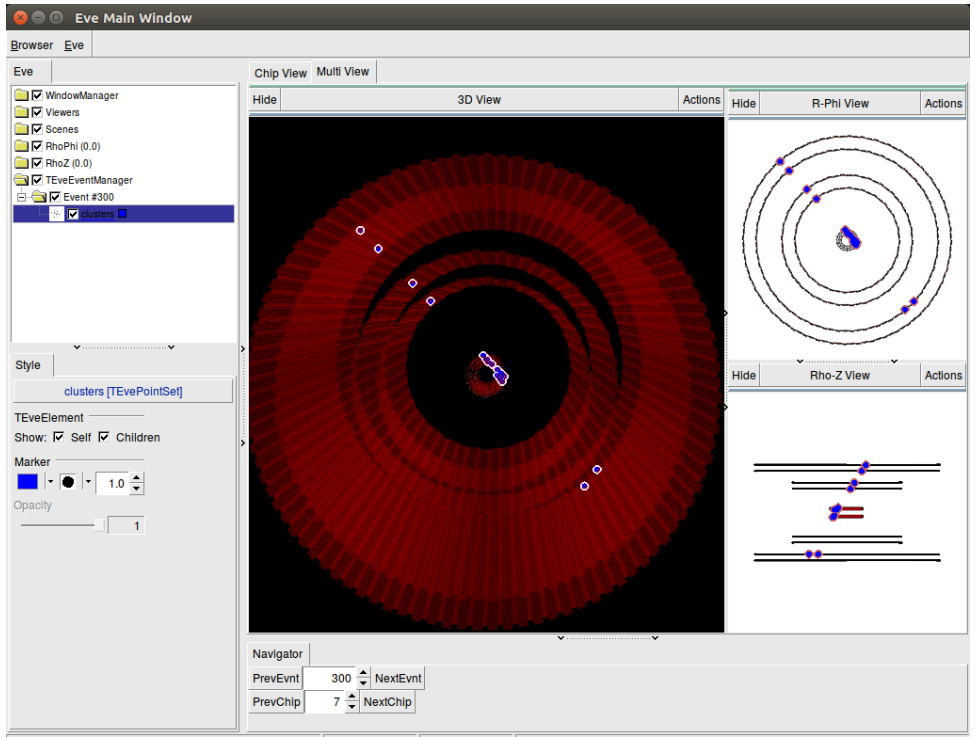


Readout Chain – Integration and commissioning

- Gradual integration of system components
  - Detector Staves **(D)** + Readout Unit **(RU)** + Common Readout Unit/First Level Processor **(CRU/FLP)**
  - **D** + **RU** + **CRU/FLP** + Trigger System **(LTU)**
  - **D** + **RU** + **CRU/FLP** + **LTU** + DAQ Backend **(EPN)**
  - **D** + **RU** + **CRU/FLP** + **LTU** + **EPN** + Online data analysis **(QC)**
- Standalone and global data runs are executed routinely
  - Ongoing finalization of the detector control and calibration software
  - Ongoing integration and debugging of the data processing chain
- Longest runs: 20h FHR at 11kHz / 12h FHR at 44.9kHz
- Core functionality of readout firmware and hardware validated
  - Next: Optimize data diagnostics and maximum throughput

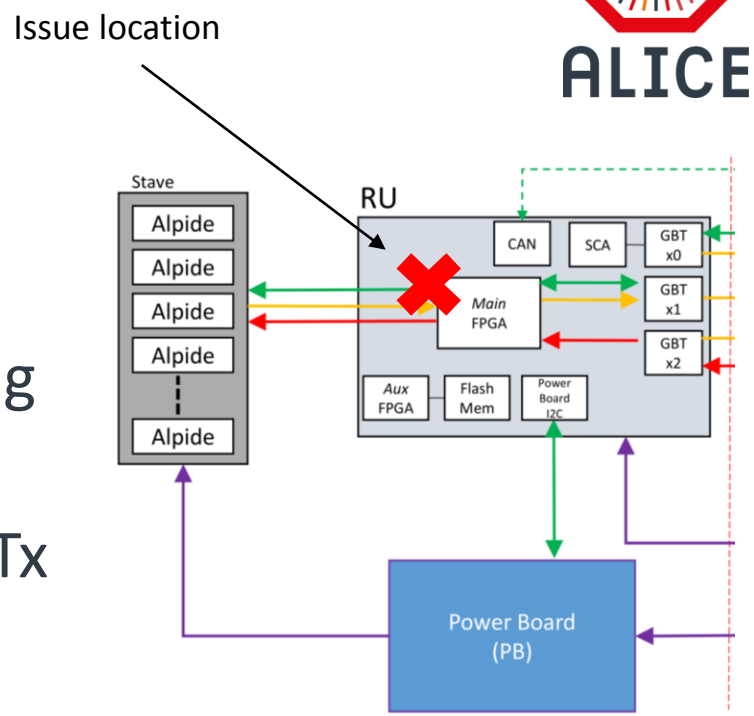


Readout Test	Status	Average System Data Rate	# Runs / Total Hours
Cosmic + noise (uncalibrated)	DONE	~7 GB/s	20 / 160h
pp emulation / 45kHz	ONGOING	~12GB/s	
Pb-Pb emulation / 45kHz	ONGOING	~40GB/s	

Challenges, issues and selected lessons

Lesson 1: Detector data link issue

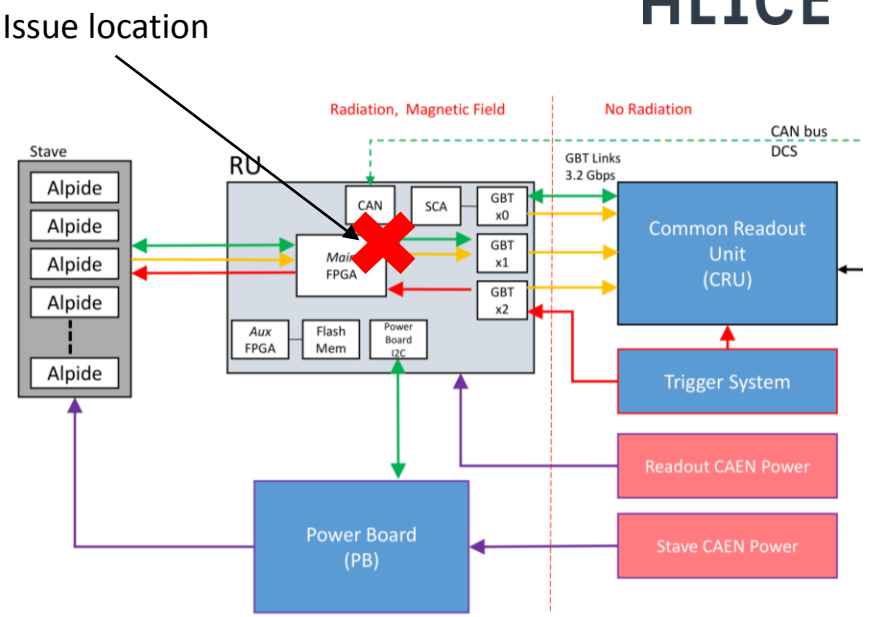
- FPGA transceiver in stuck state:
  - Could **not** be recovered by any type of reset
    - Required FPGA reprogram/power-cycle
- Appeared sporadically during on-surface commissioning
  - But could not be reproduced in the lab
- Issue caused by using the clock recovered from the GBTx as reference clock for the FPGA Transceivers
- Solution:
  - **Switched to local oscillator clock**
- Lesson:
  - Stability over time of the transceivers reference clock also important, in addition to frequency and low jitter



Lesson 2: Corrupt slow control transactions

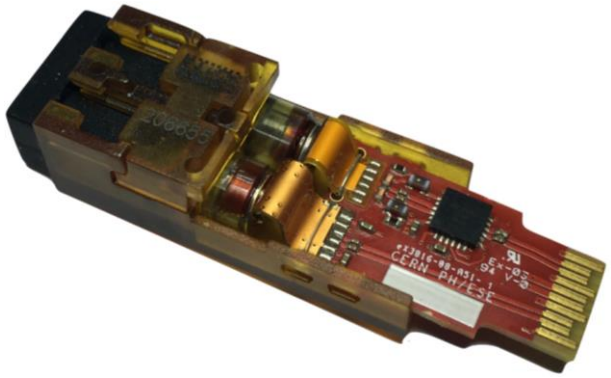
- Power control registers mysteriously overwritten with garbage values:
  - **Critical registers** controlling the detector power affected
- Appeared sporadically in-situ at experiment
  - Never detected in lab or on-surface commissioning
- Events correlated with switch of central ALICE clock
  - GBTx chip outputs noise on e-links when reconfigured
- Solution:
  - **Add very simple redundancy to the control protocol**

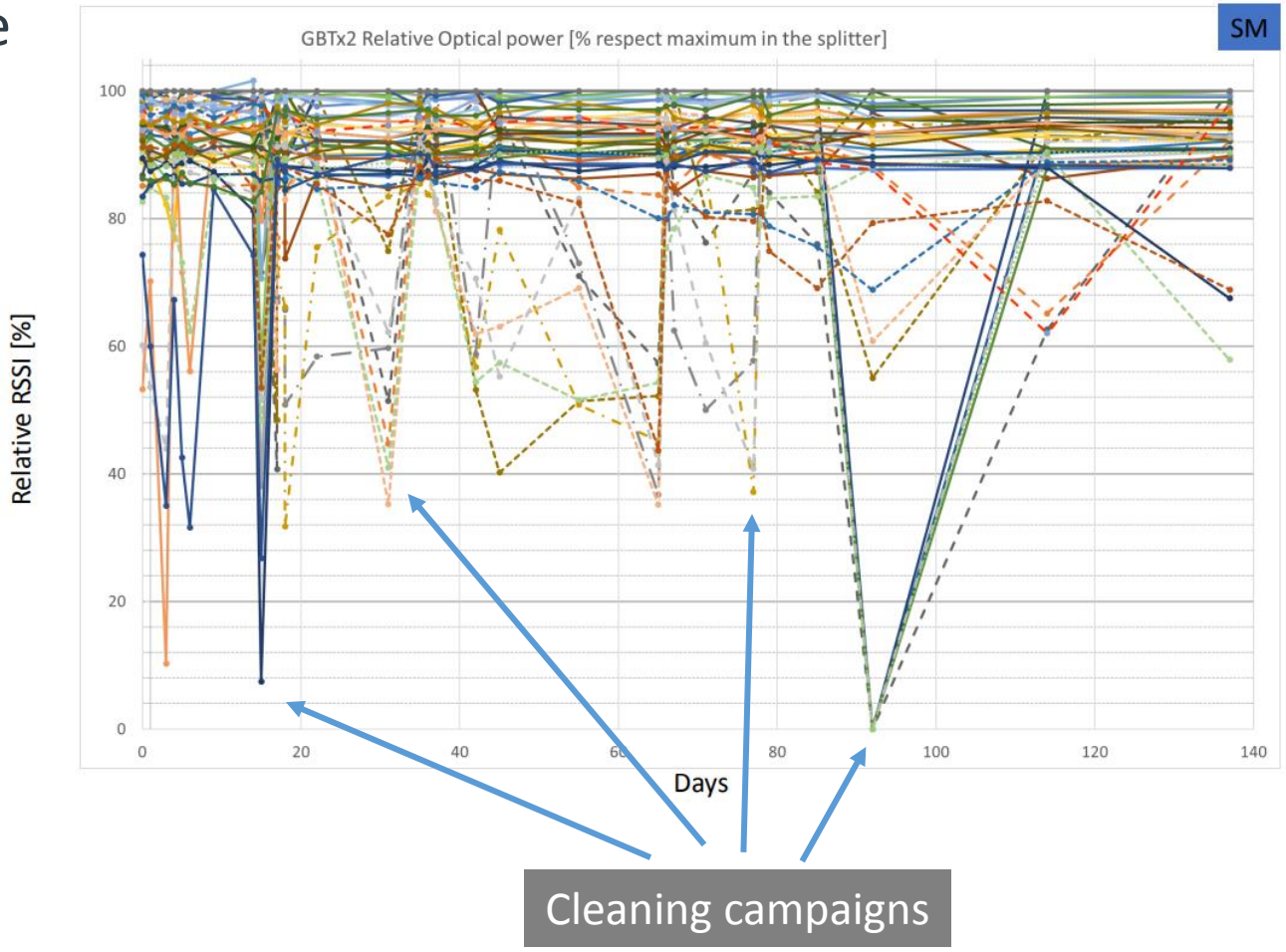
- Lessons:
  - One should try to anticipate low probability behavior at design time
  - Checks and redundancy should be implemented on all interfaces



Lesson 3: VTRx deterioration

- Gradual optical power and performance **deterioration** of certain VTRx modules
- First observations during on-surface commissioning
  - ~40% of links prone to degradation
  - Time to failure: ~500h for up to 50%
- At high temperature gradients the optical fiber gets **contaminated by glue vapors** from the VTRx module





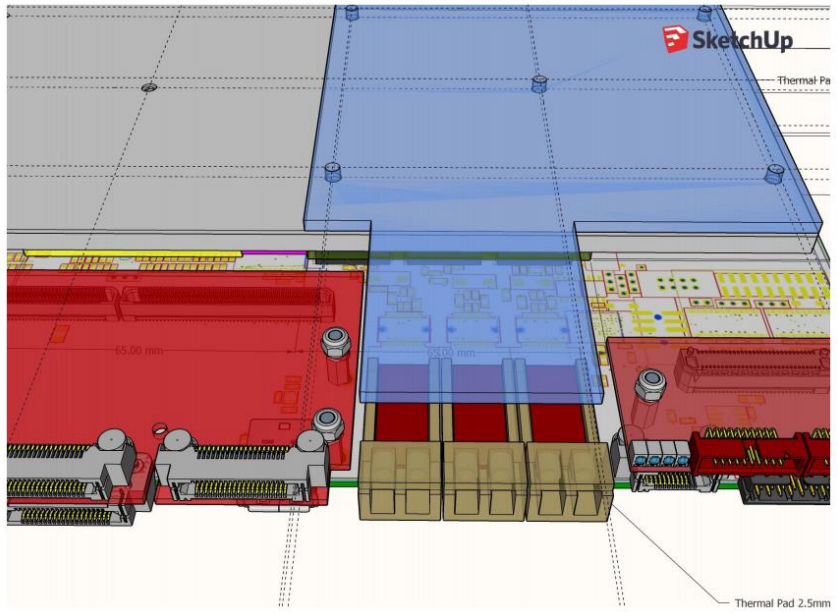
Also see [Grace Cummings: CMS HCAL VTRx-induced communication loss and mitigation]

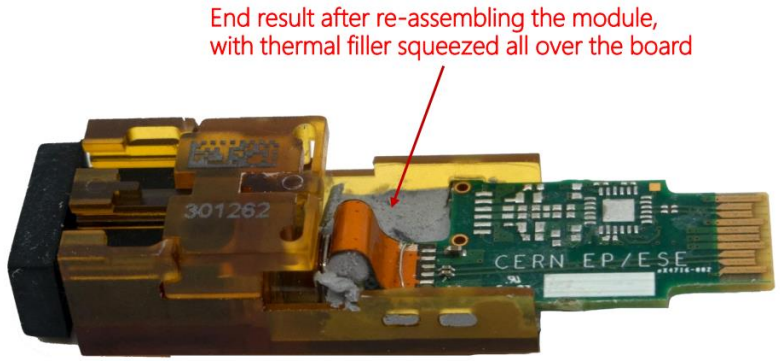
Lesson 3: VTRx deterioration, continued

- Solution(s):
  - Three mitigation interventions are currently **ongoing**

1. **Unmount, re-bake and re-mount** every VTRx
   - 192 Single Mode modules + 192 Multi Mode modules
2. **Improve cooling** of the VTRx to reduce internal thermal gradients
3. **Increase optical power margins** adding optical repeaters (see next lesson)

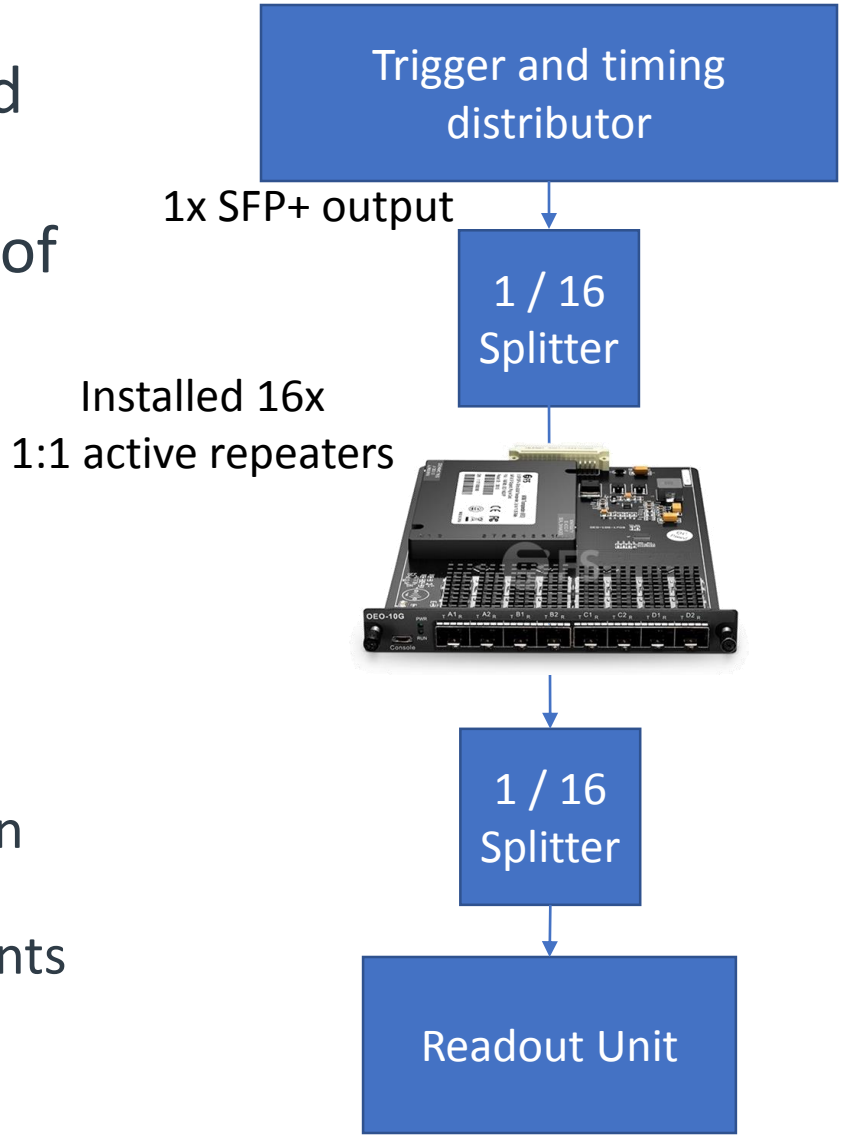
- Lesson:
  - Certain issues will only appear when systems scale up
  - Be prepared to deal with nonconformity of acquired electronics components





Lesson 4: Trigger network margin

- Optical power margin of trigger link defined from lab-characterization and datasheets
- **Insufficient** to withstand the deterioration of the VTRx
- Solution:
  - Add off-the-shelf commercial active optical repeater to **increase power margin**
    - Optical power margin: 4.5 => 7dB
    - Negligible impact on timing
- Lesson:
  - Full system integration and long-term operation will never miss to surprise
  - Investigate if affordable off-the-shelf components can improve margins



Summary

- ITS installed March/May 2021
- Standalone commissioning **completed** - global commissioning **ongoing**

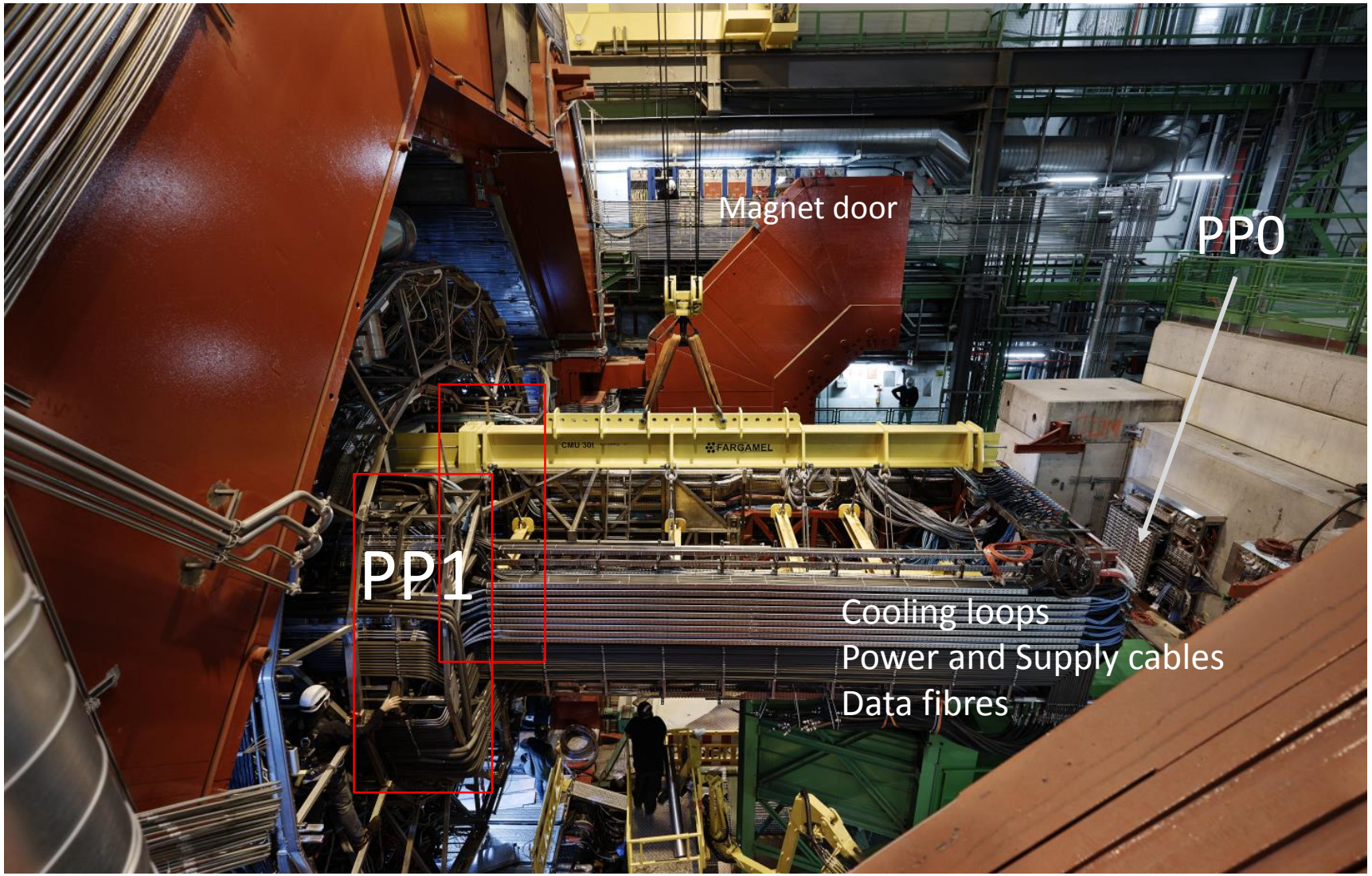
- Selected lessons:
  - Stability over time of the transceivers reference clock also important
  - Simple checks and redundancy should be implemented on all interfaces
  - Be prepared to deal with nonconformity of acquired electronics components

  - The benefits of on-surface commissioning largely outweigh the cost
  - Certain issues will only appear when systems scale up
  - Full system integration and long-term operation will **never miss to surprise**

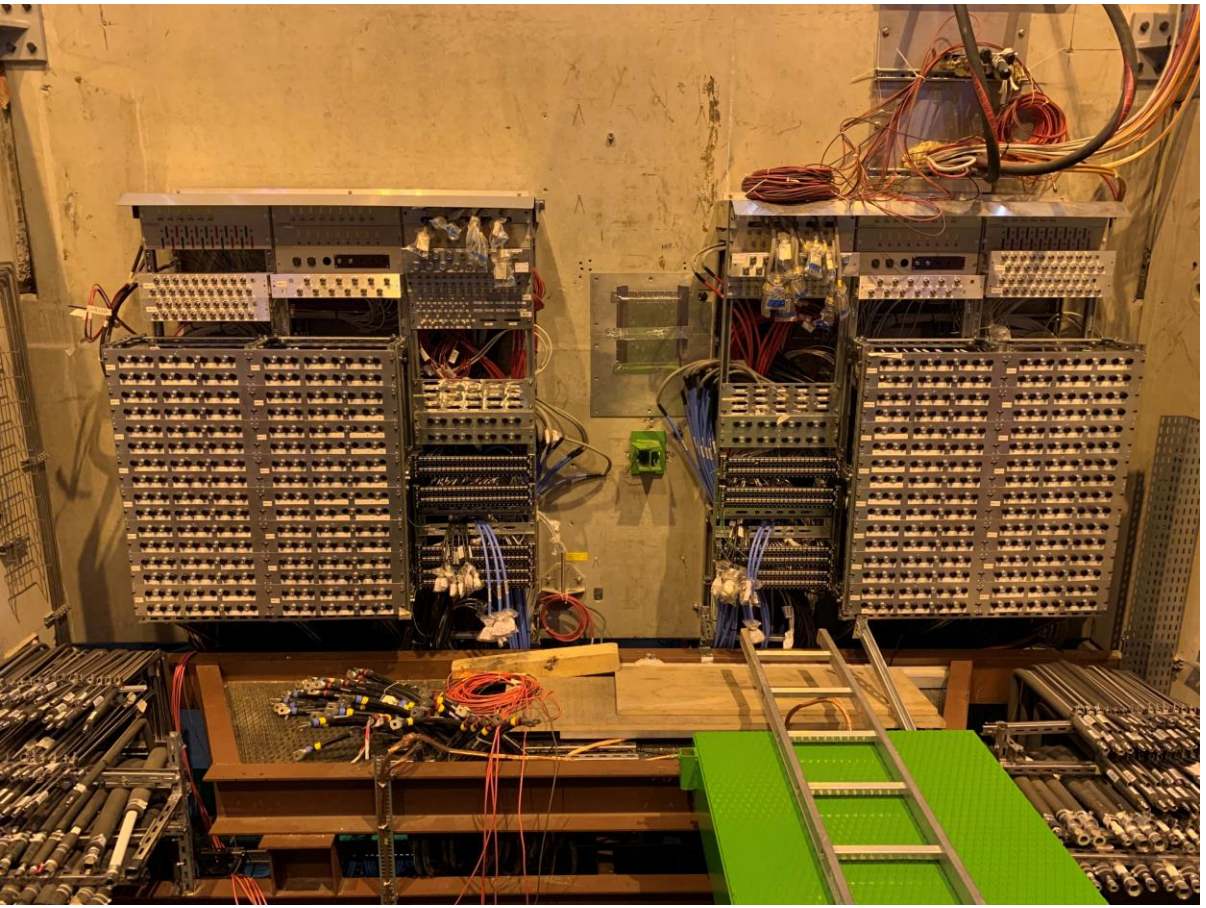
ITS readout system is ready for LHC pilot beam late October 2021

Backup

ALICE Miniframe



Patch Panel 0



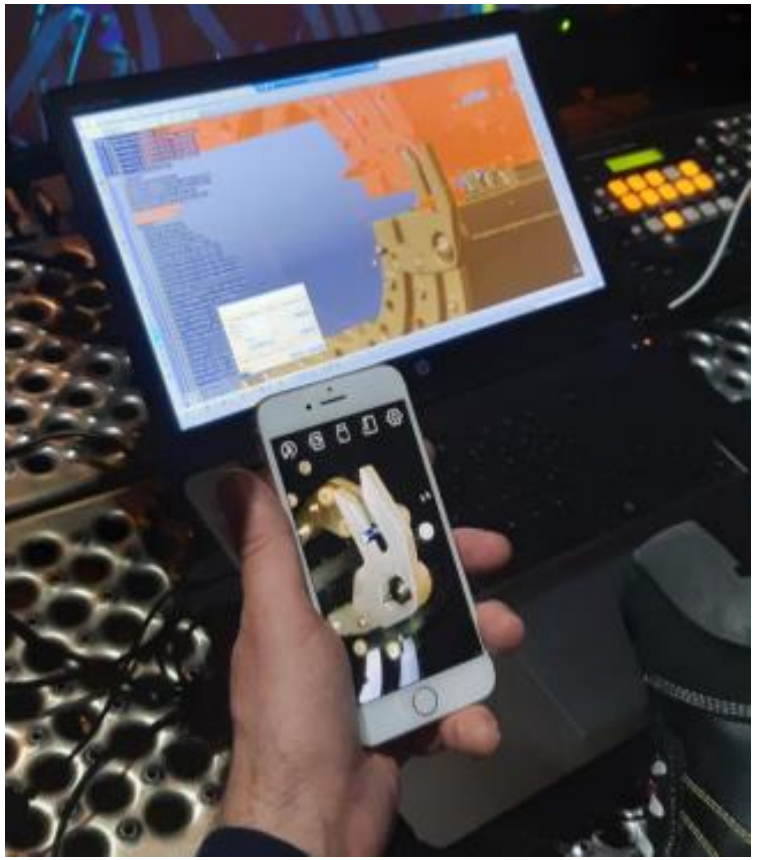
Fiber optics patch panel

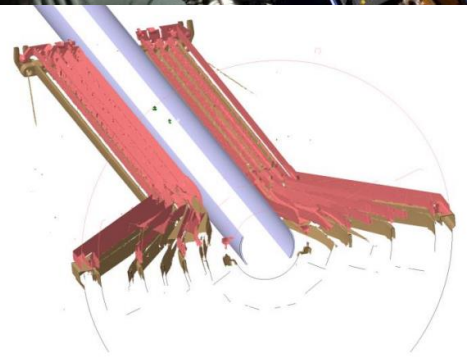
ALICE ITS2 - Installation

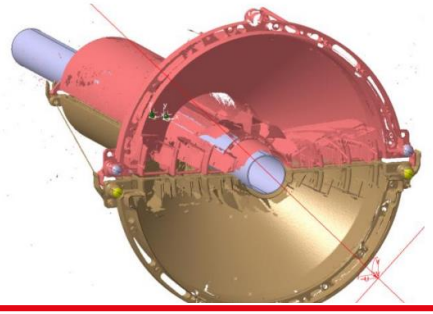
May 2021
Inner Barrel matching

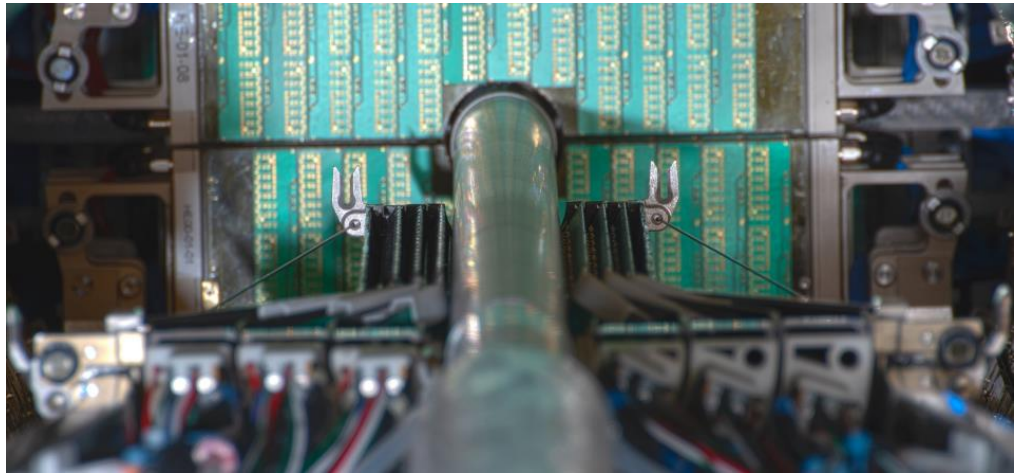
Real time verification using 6 cameras

Comparison with 3D CAD scans





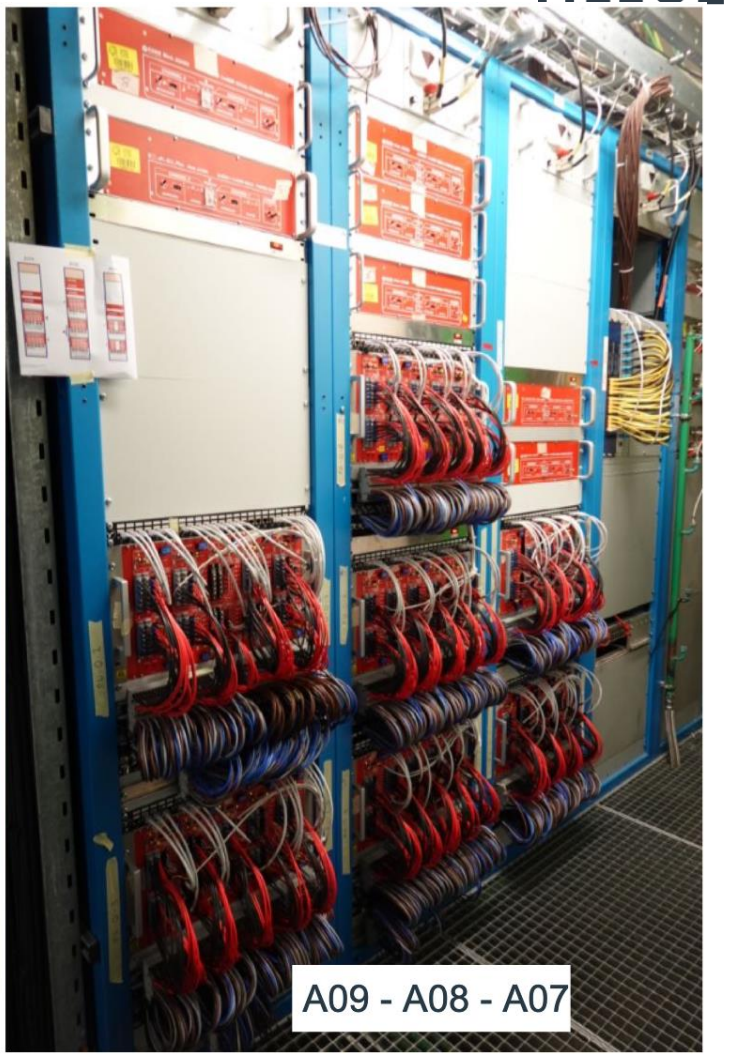




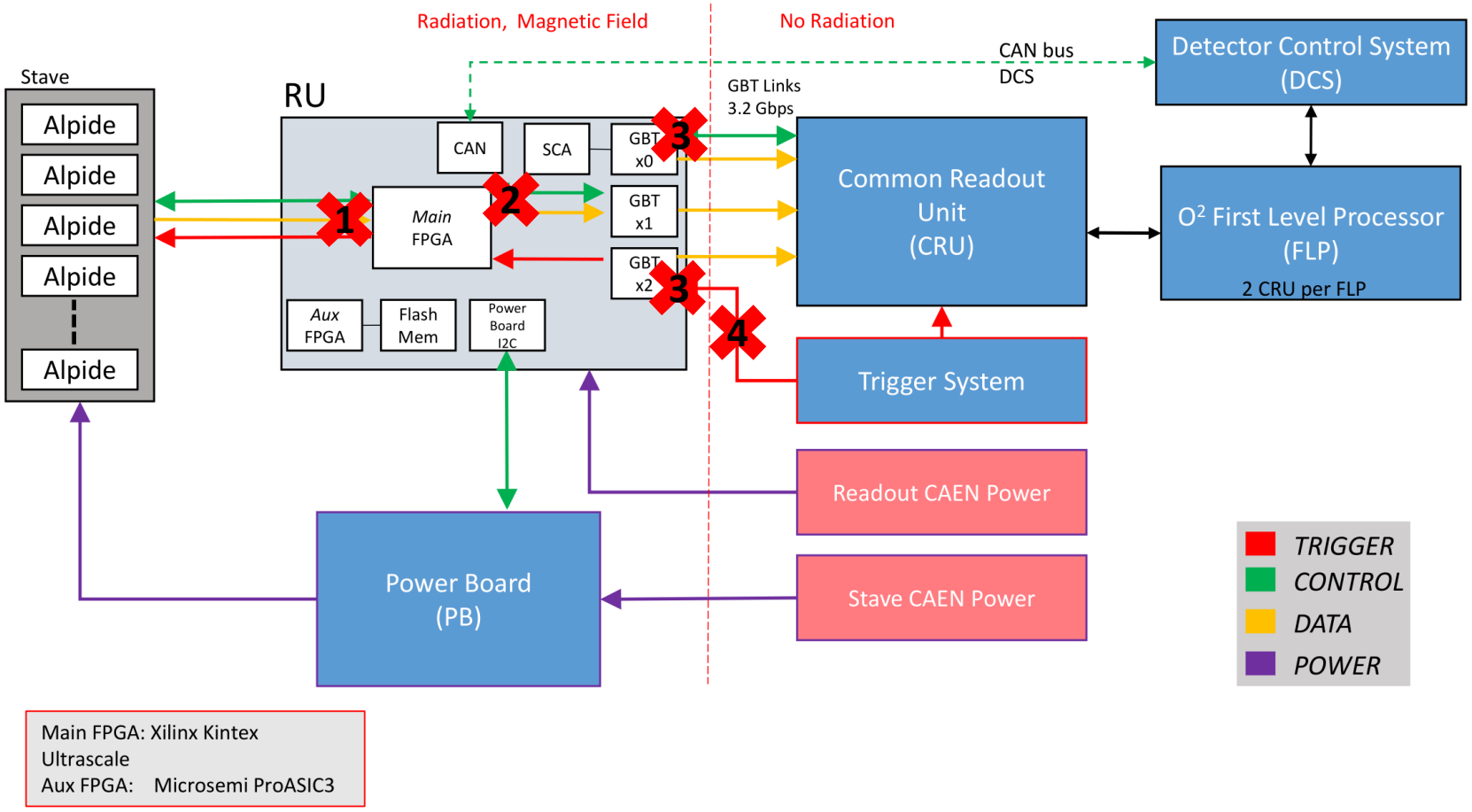
ITS CAEN System

1 Mainframe

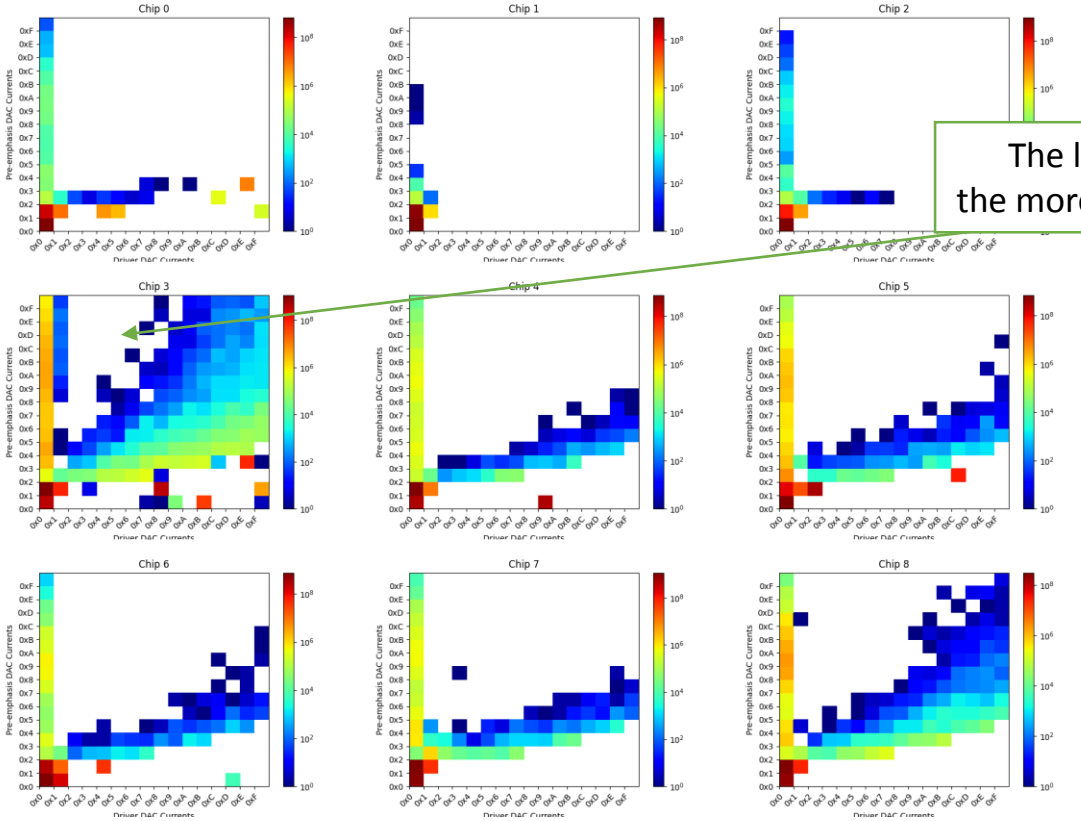
12* A3486
13* Easy Crates
61* A3009

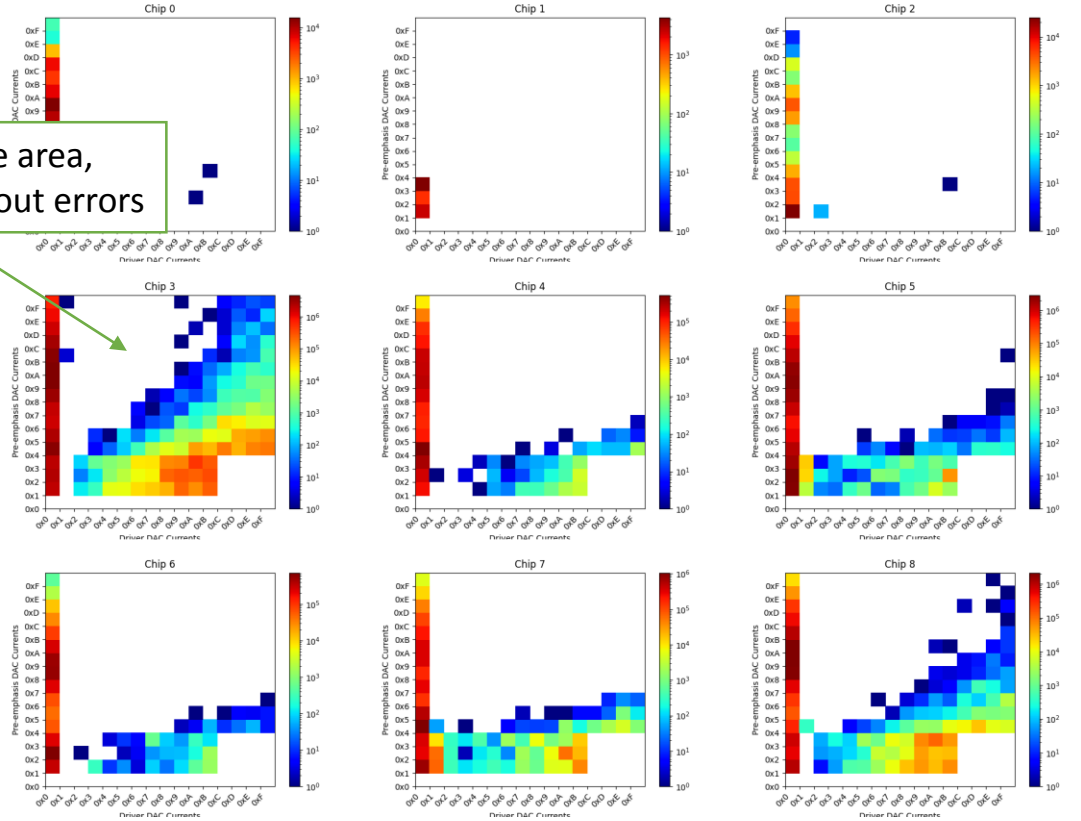


Issue location



Transceiver Reference Clock Comparison





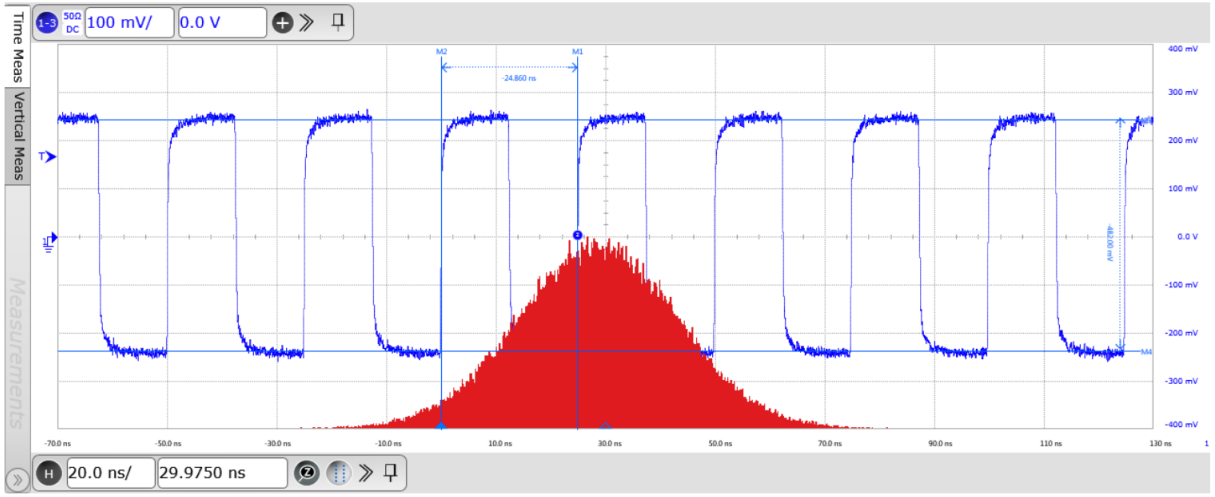
The larger the white area,
the more settings without errors

External Clock

Lab setup: possible higher quality than experiment

Local Clock

Clock Jitter Measurement



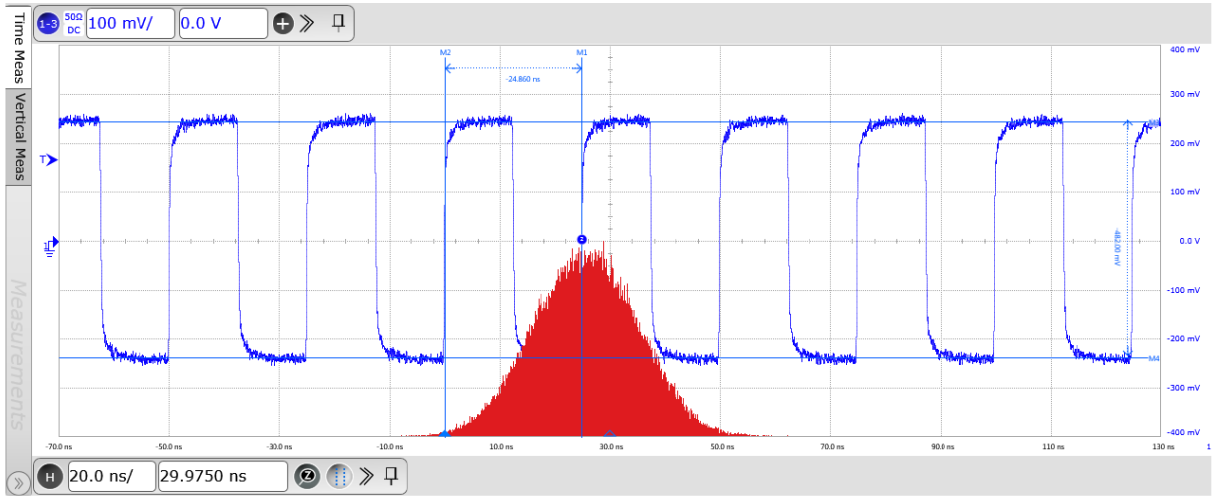
Markers Results

Marker	Horizontal	Vertical	ΔX	1/ΔX	ΔY	ΔY/ΔX	Delta To
M1	24.8600 ns	----------		---		---	--
M2	0.0 s	----------	-24.860000 ns	-40.225261 MHz		---	1
M3	----------	248.000000 mV		---		---	--
M4	----------	-234.000000 mV		---	-482.000000 mV	---	3

Measurements Results

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
Clock TIE(1-3)	-3.40 ps	-2.3966 ps	-18.71 ps	14.52 ps	33.24 ps	3.6495 ps	130720
Period(1-3)	24.95166 ns	24.9508547 ns	24.92788 ns	24.97177 ns	43.88 ps	5.1819 ps	114380

Local Clock



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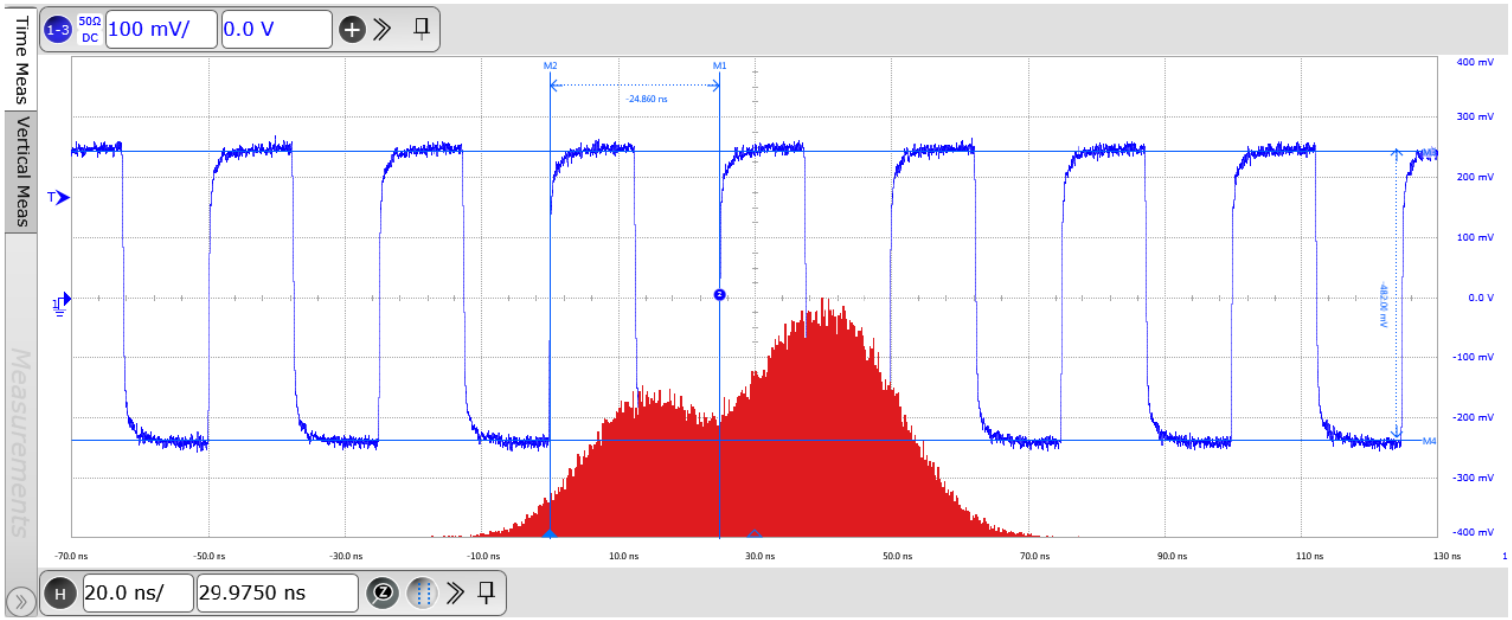
Measurements Results

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
Clock TIE(1-3)	-1.55 ps	-90.8 fs	-17.99 ps	22.07 ps	40.05 ps	4.6711 ps	124544
Period(1-3)	24.95682 ns	24.9509824 ns	24.92115 ns	24.98050 ns	59.34 ps	7.4525 ps	108976

External Clock (LTU)

Clock Jitter Measurement – Post Data Run



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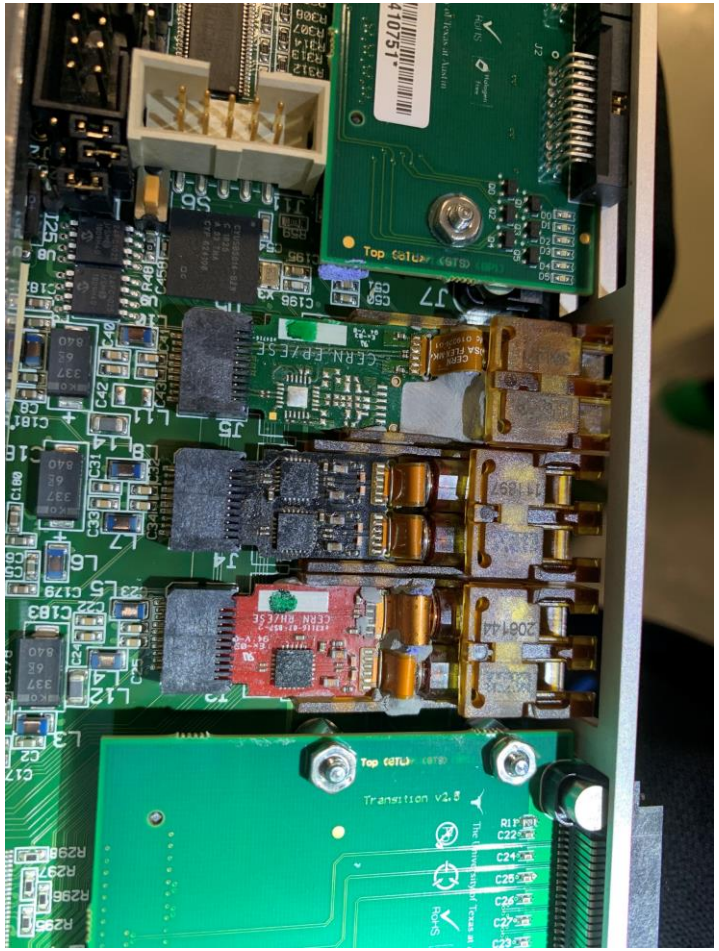
Measurements Results

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
Clock TIE(1-3)	-7.31 ps	-796.8 fs	-27.71 ps	24.41 ps	52.12 ps	7.8998 ps	88256
Period(1-3)	24.96125 ns	24.9510382 ns	24.91553 ns	24.99297 ns	77.45 ps	13.2058 ps	77224

VTRx extension cooling plate



VTRx extension cooling plate

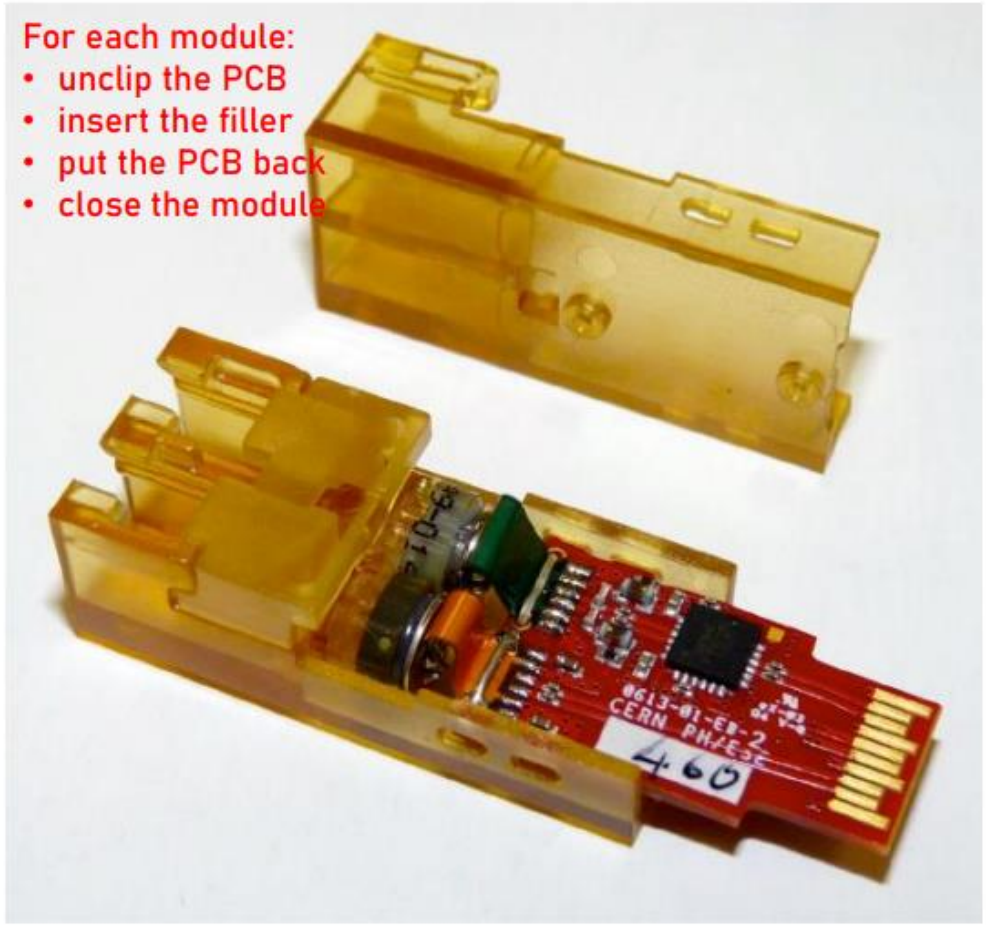
Gap Padding

Found 12mm padding is too much due to more rigid filler (different batches due to availability): to avoid risk bending the PCB decided to reduce it to 10mm

Plates Padding

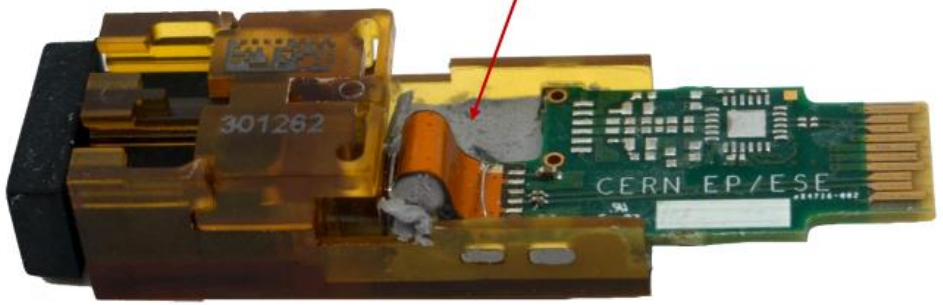
0.3 mm working well, unfortunately few pads bi-adhesive (the only available in time)

VTRx thermal gap filler installation



- 1 mm thick, double-layered extremely soft padding material fill the gaps between flex, PCB and ROSA/TOSA
  - Improving head transfer
- ~200 MM, ~240 SM modules patched
- Average of 80 modules day^{-1} person^{-1} achievable
- Preparing the filler material is the operation taking most of the time
- Unplugging/plugging the PCB unavoidably stresses the flexes
  - ~3% failure ratio

End result after re-assembling the module, with thermal filler squeezed all over the board



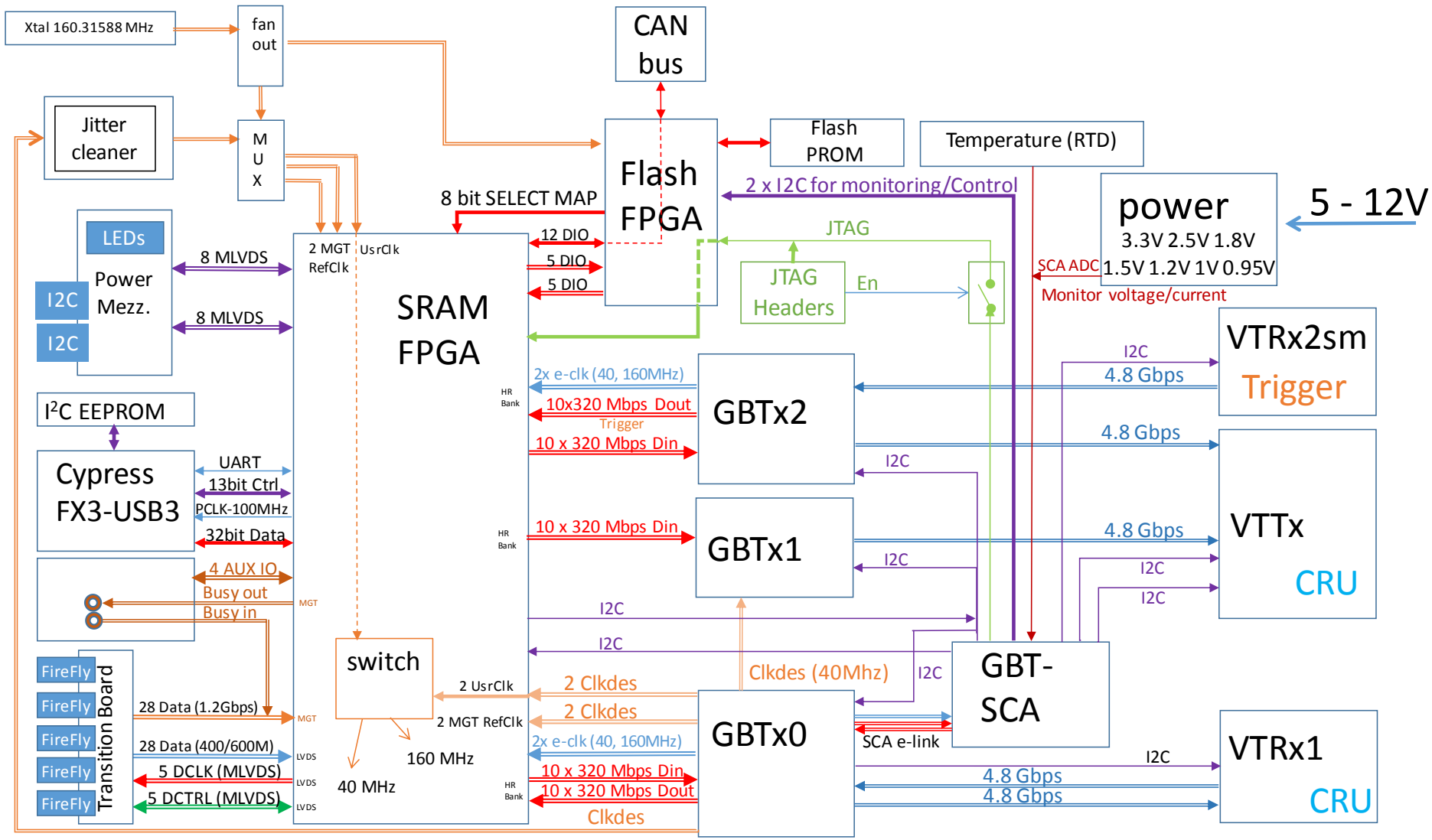
Maximum data rates for the various channels

Channel	Capacity	Unit
Detector IB Link (layers 0, 1, 2)	960	Mb/s
Detector OB Link (layers 3, 4, 5, 6)	320	Mb/s
RU-CRU GBT Link	3200	Mb/s
CRU to FLP RAM	13750	MB/s
FLP to O2-EPN	8625	MB/s
CRU to O2-EPN	4312	MB/s
Total ITS to EPN	40000	MB/s

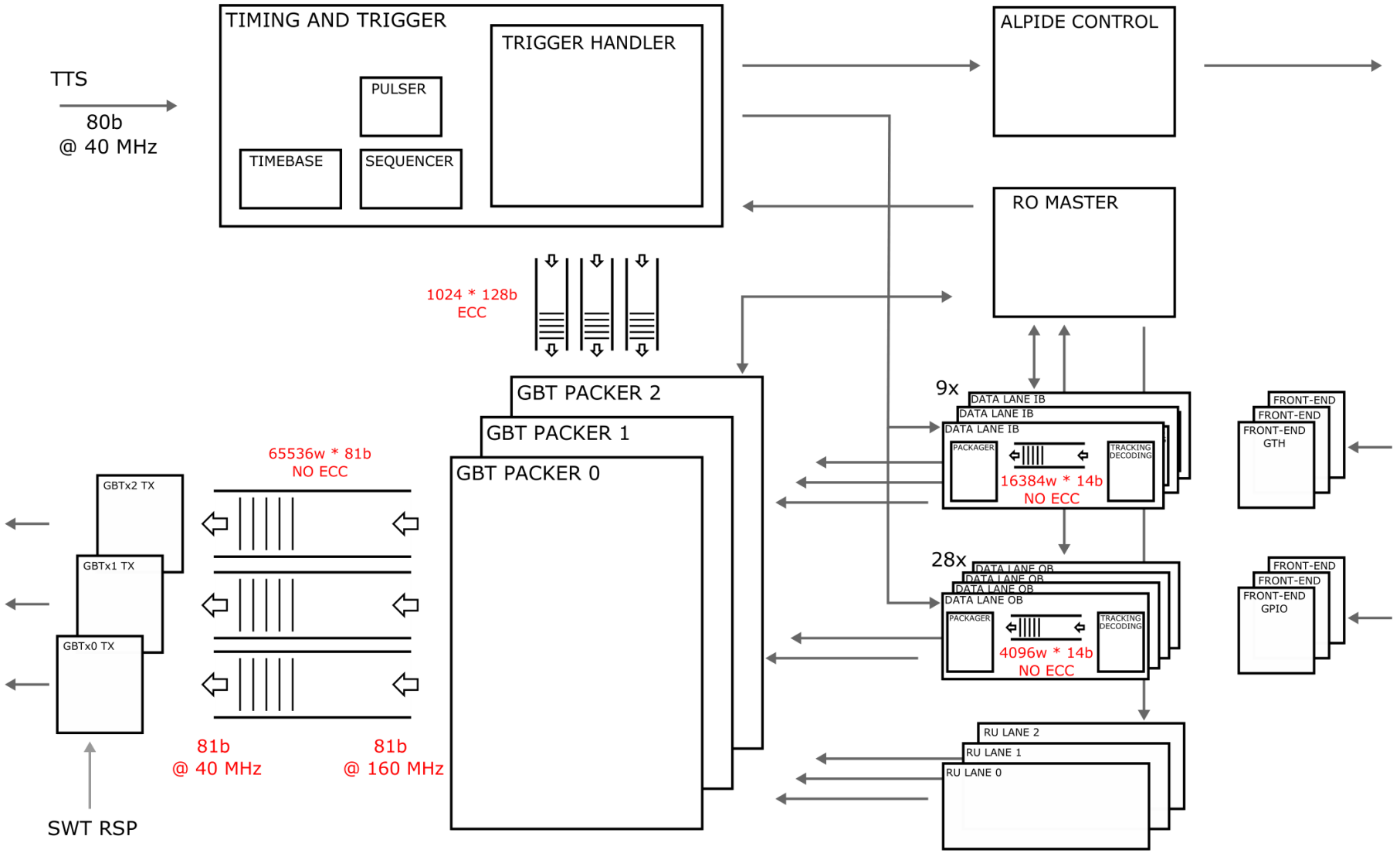
Readout System Architecture

Layer	RU	GBT Links/RU	RU/CRU	CRU	FLP
0	12	**3**	6	2	1
1	16	**3**	8	2	1
2	20	**3**	5	4	2
3	24	2	12	2	1
4	30	2	8,7,8,7	4	2
5	42	2	11,10,11,10	4	2
6	48	2	12	4	2
Total	**192**			**22**	**11**

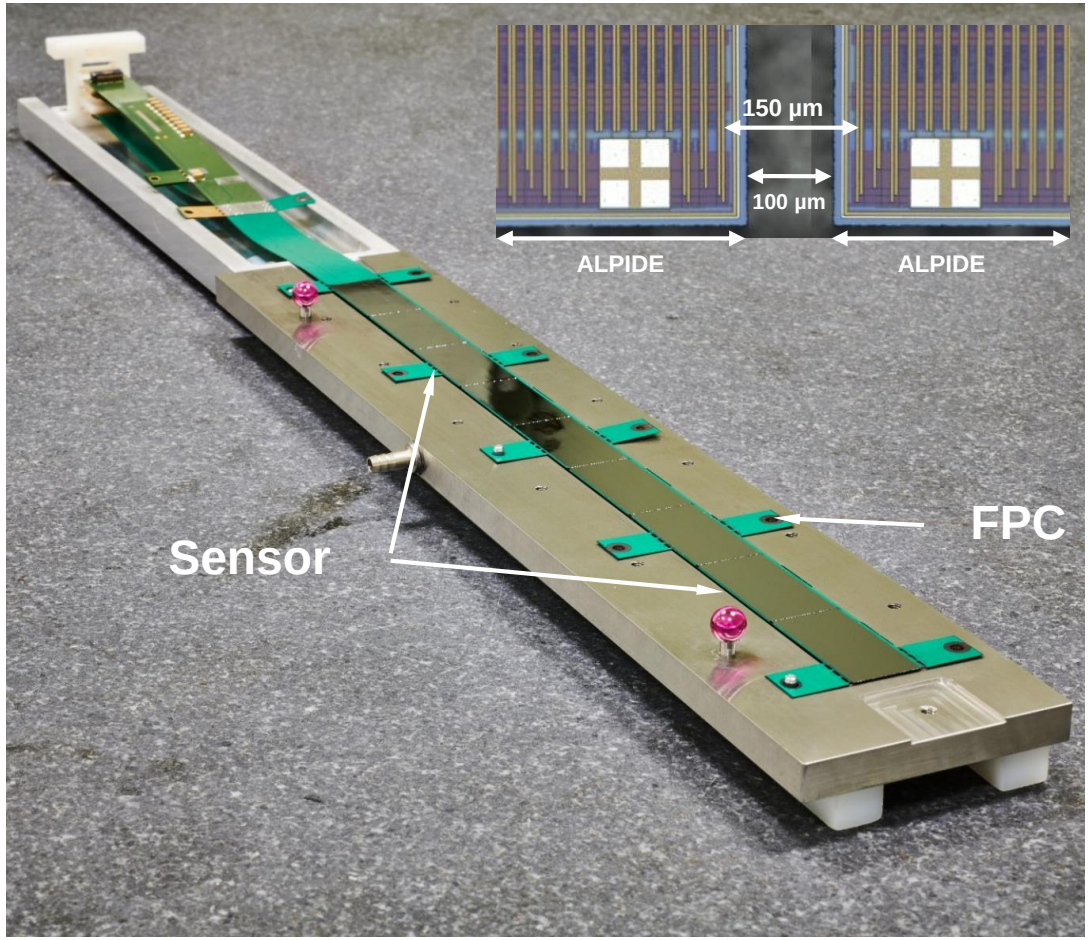
RU Block Diagram

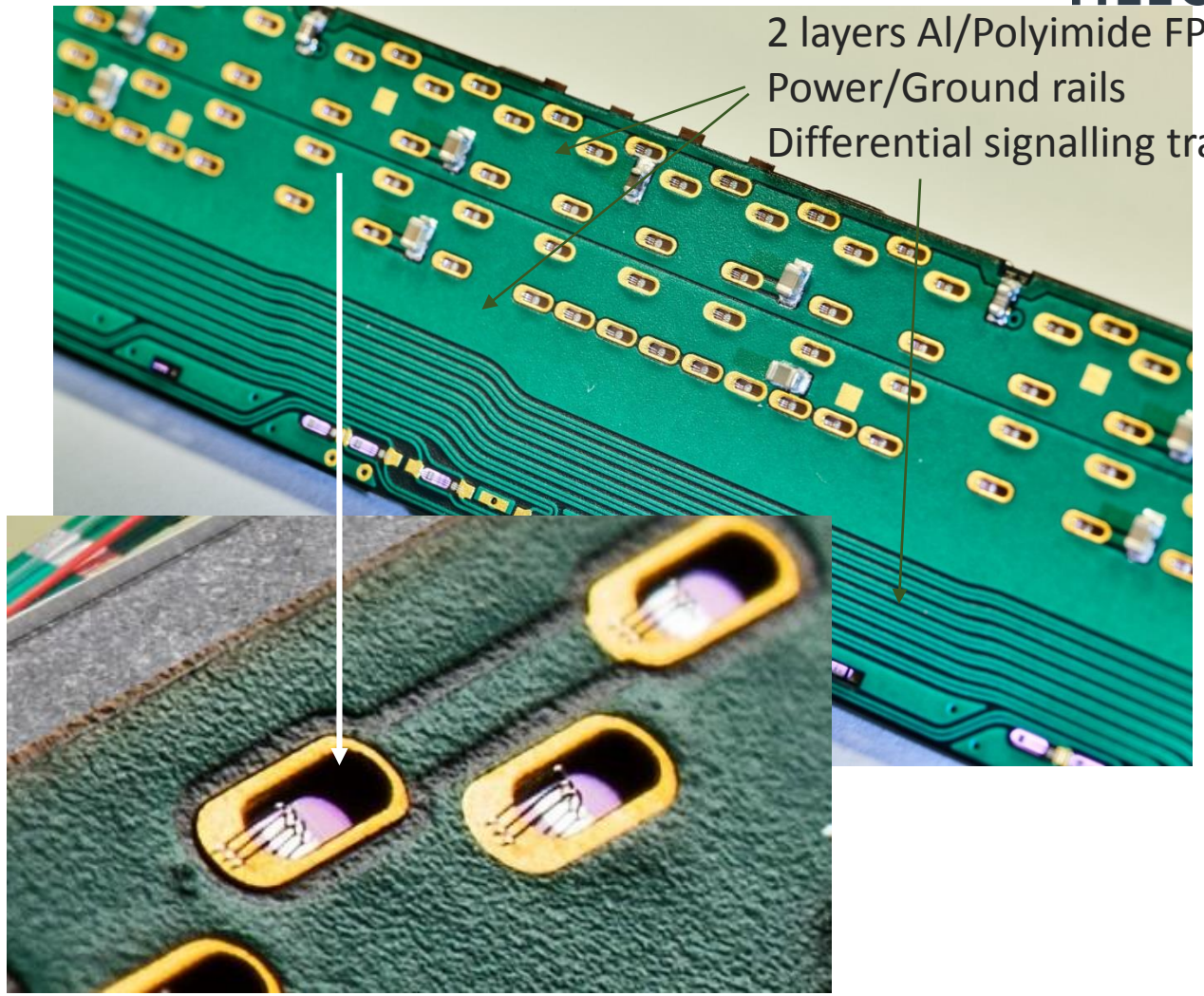


Readout Unit FPGA Firmware

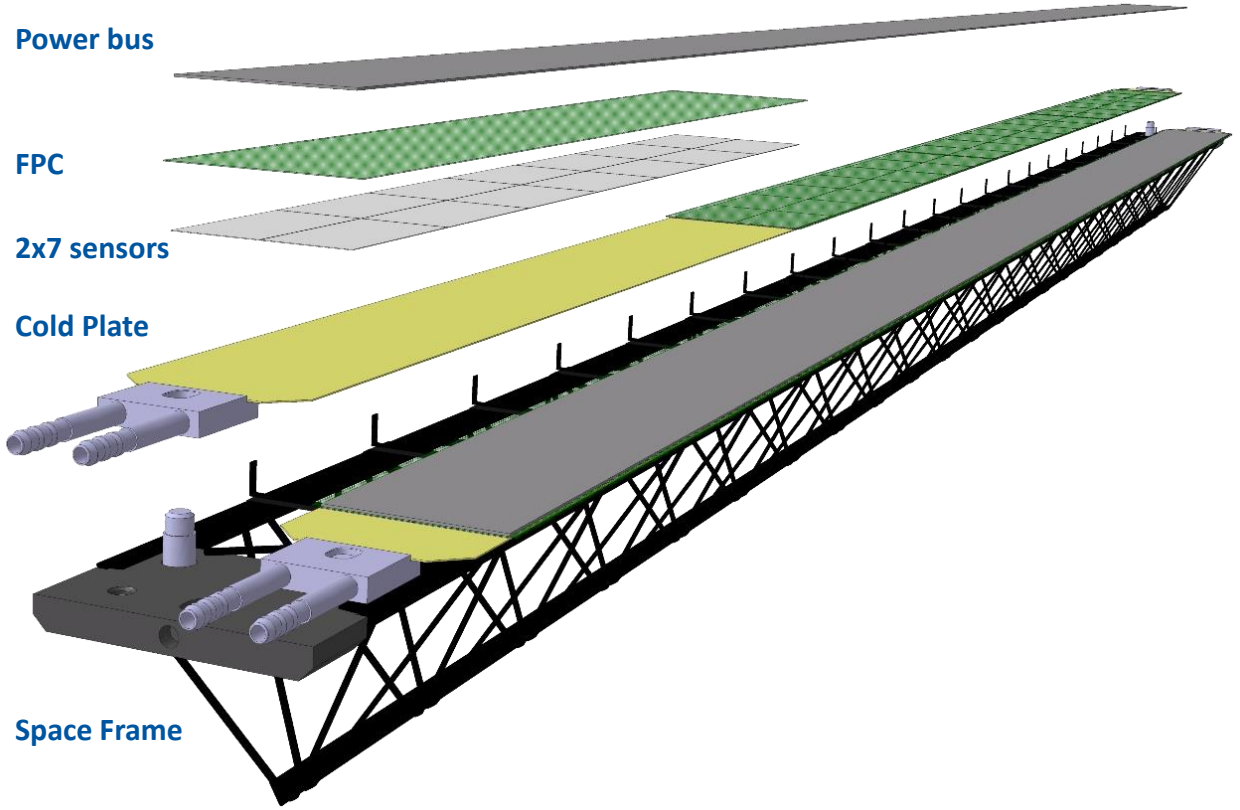


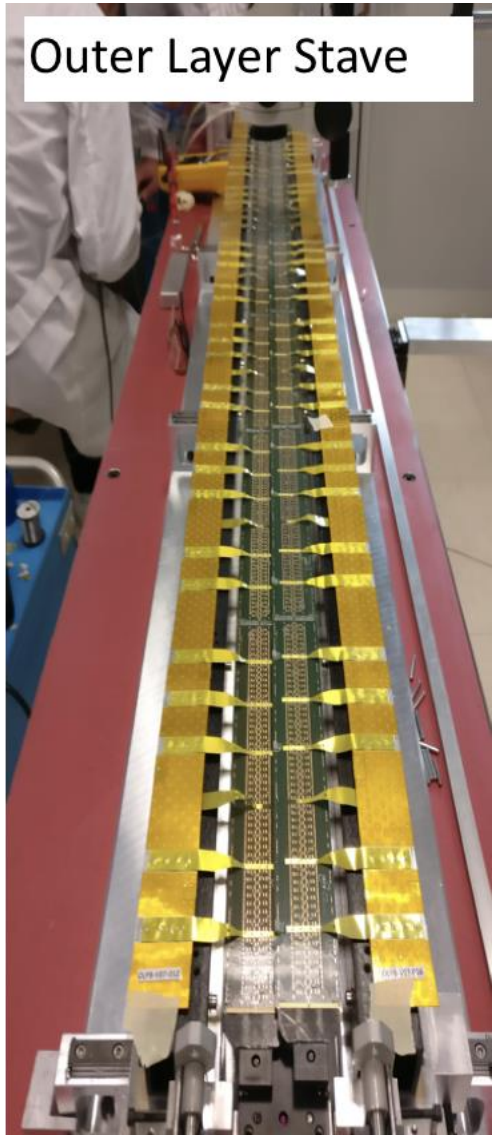
Inner Barrel Stave



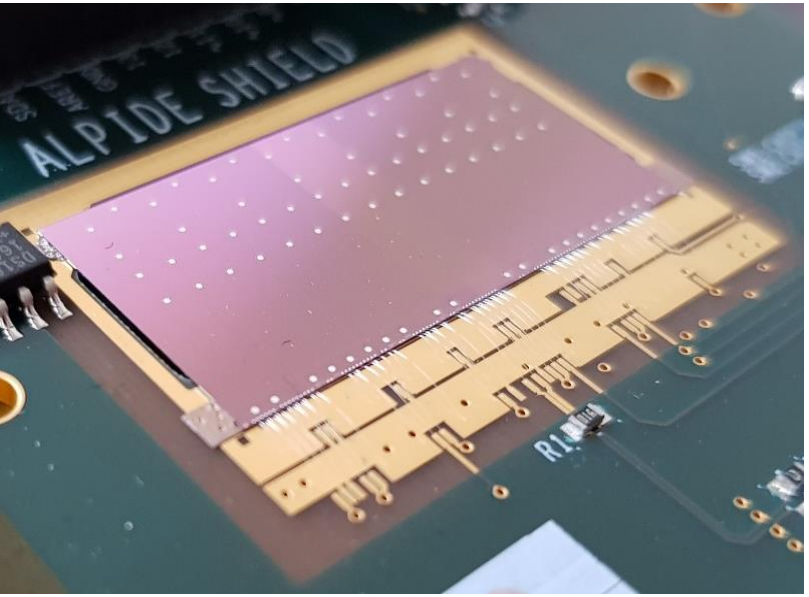


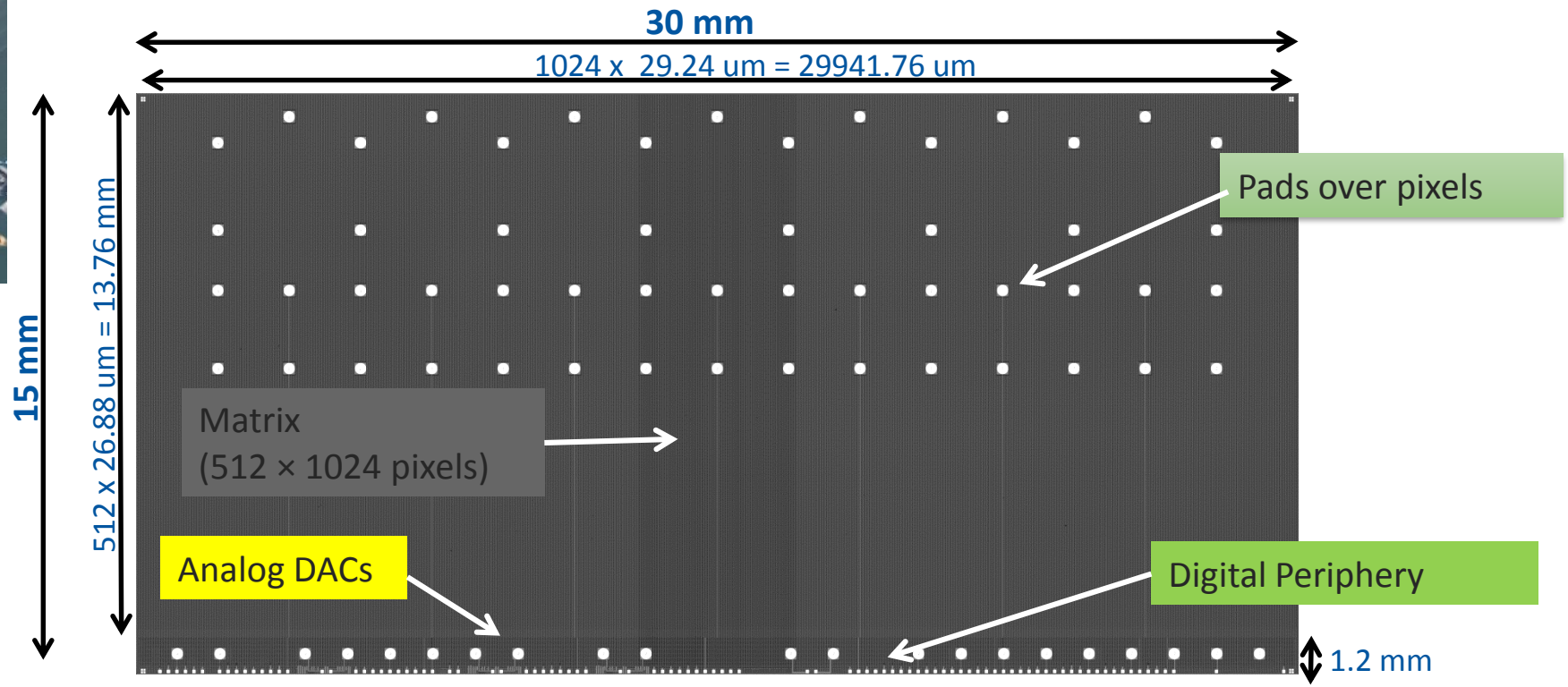
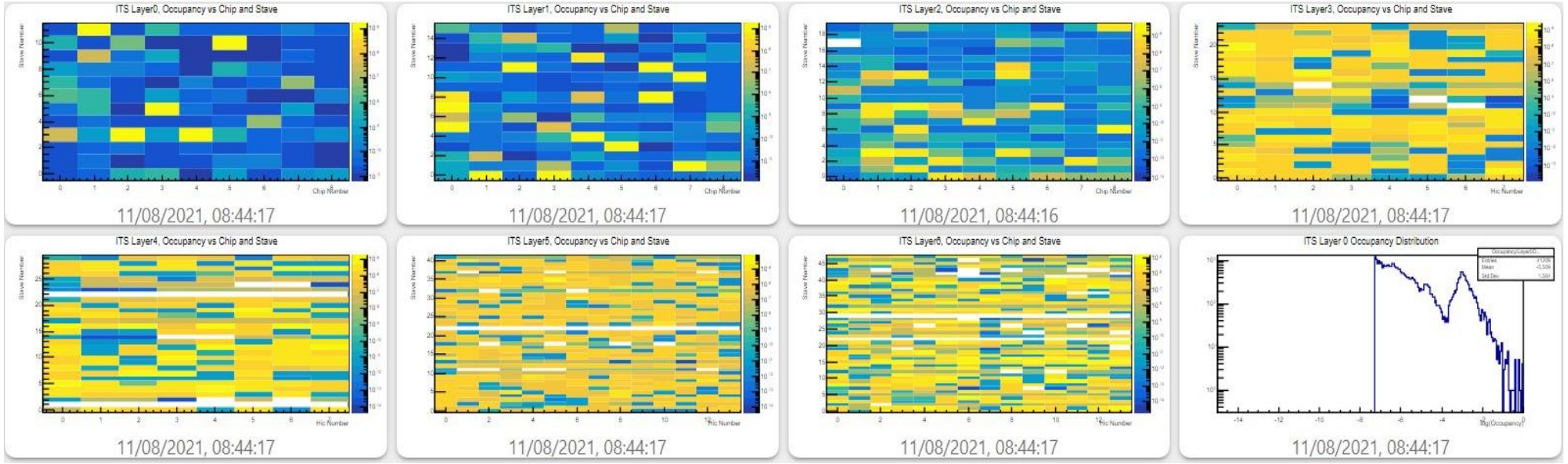
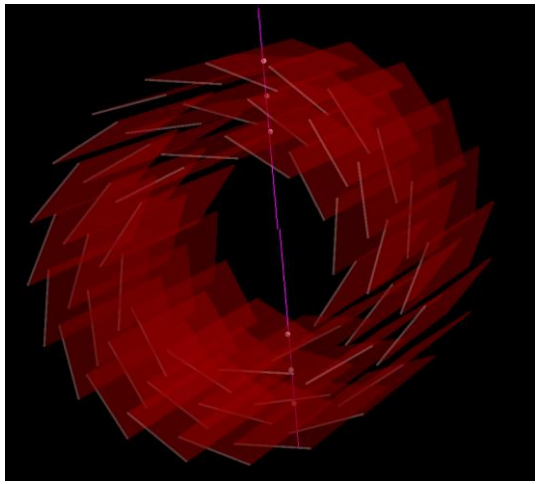
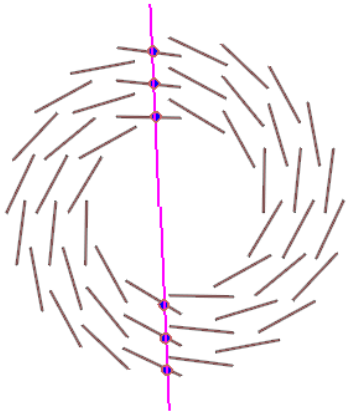
Outer Barrel Stave





ALPIDE Chip


ALPIDE SHIELD


30 mm
1024 x 29.24 um = 29941.76 um
15 mm
512 x 26.88 um = 13.76 mm
Pads over pixels
Matrix
(512 × 1024 pixels)
Analog DACs
Digital Periphery
1.2 mm

Reconstruction workflow