The Prototype Hardware Design and Test of Global Common Module for Global Trigger System of the ATLAS Phase II Upgrade

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I. Summary

The Global Trigger is a new subsystem, which will perform offline-like algorithms on full-granularity calorimeter data. The calorimeter detector subsystems, L0Calo Feature Extractor (FEXs), and Muon Central Trigger Processor Interface (MUCTPI) provide serial data for each bunch crossing to the Multiplexer Processor (MUX) layer. These data are then time-multiplexed and all the data for a given event are transported to a single Global Event Processor (GEP) node that executes the algorithms. The results are then sent to the Central Trigger Processor (CTP) through the CTP Interface. There are two main advantages of the time-multiplexed architecture. First, ordering the data transmission to scan across the detector allows two-dimensional algorithms to be implemented in one dimension, reducing resource usage by an order of magnitude. Second, the event processor is decoupled from the LHC bunch-crossing rate, allowing the use of asynchronous and high-level algorithms that are impossible in the Phase-I hardware trigger.

As shown in the Fig. 1, the hardware implementation of the Global Trigger consists of three primary components: a MUX layer, a GEP layer, and a demultiplexing Global-to-CTP Interface (CTP Interface), all of which use the same hardware implementation - Global Common Module (GCM) to minimize the complexity of the firmware and simplify the system design and long-term maintenance.

The GCM design is an ATCA Front Board with two large FPGAs and one SoC FPGA. The number of processor nodes of each layer are based on the total front-end output channels, maximum input channels of each nodes and the maximum resource available for processing of each node FPGA. Driven mainly by the outputs from the Calorimeter, 72 MUXes and 48 GEPs with up to 72 25 Gb/s inputs/outputs are required.

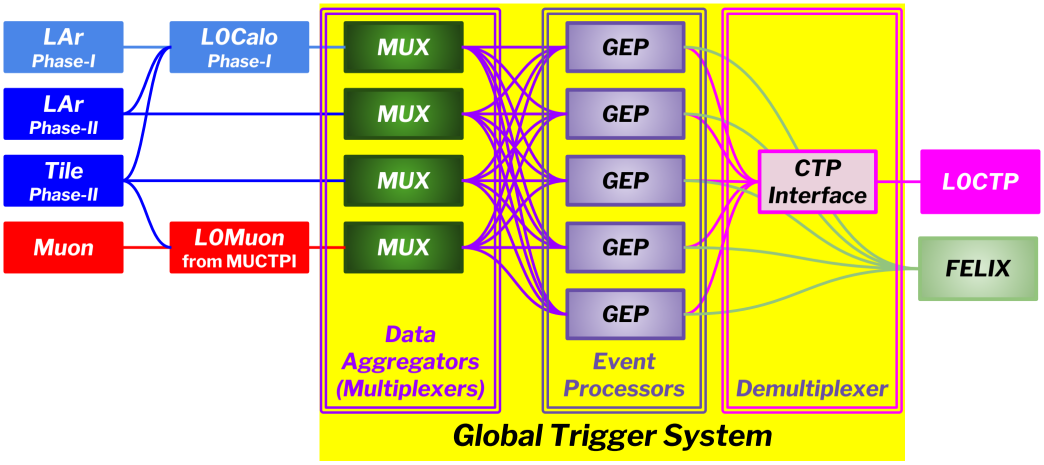

Fig. 1. The functional design of the Global Trigger system.

To meet both the resource requirements and number of 25 Gb/s transceivers, the Xilinx Vertex UltraScale+ FPGA VU13P is selected for the node processors, and a MPSoC FPGA ZU19EG is selected for control and monitoring function. The hardware design block diagram is shown in the Fig. 2. Each node has 8 pairs of FireFly, which is 25Gb/s 12-channel optical module produced by Samtec.

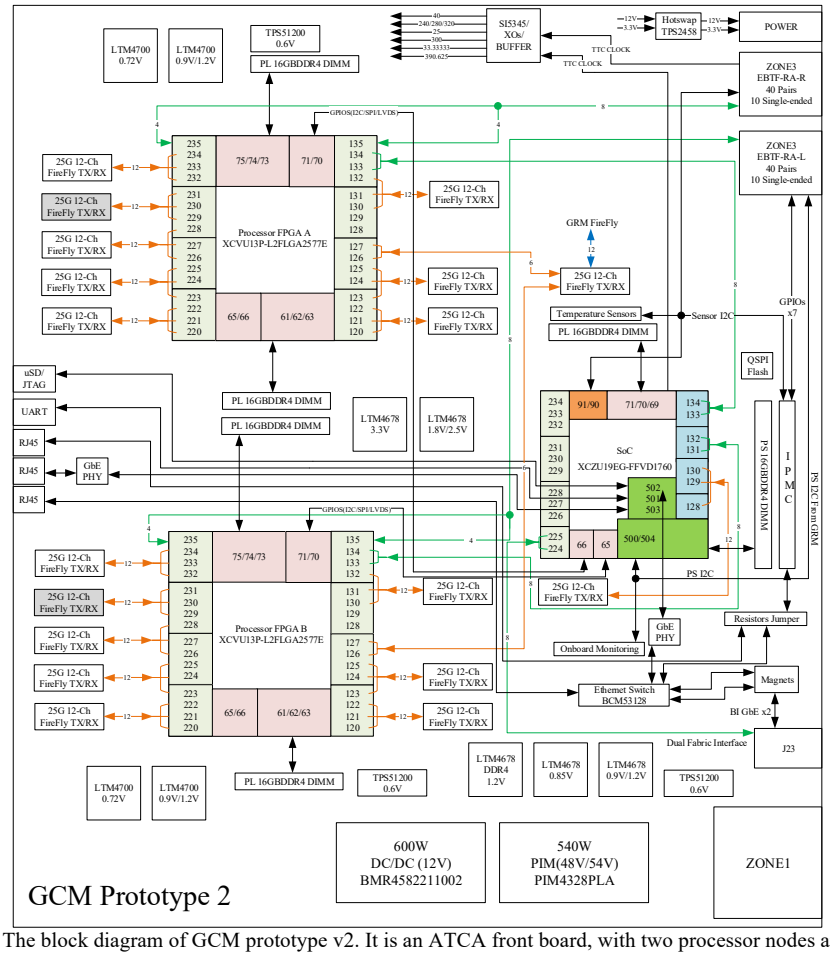

Fig. 2. The block diagram of GCM prototype v2. It is an ATCA front board, with two processor nodes and one SoC.

The hardware was designed in 2020 and is being tested since December 2020. All the major hardware functionalities and critical technologies have been verified such as Zynq UltraScale+ FPGA OS interfaces, monitoring, processor FPGA 25.78125 Gb/s electrical links, 12.8 Gb/s optical links with 14Gb/s FireFly modules, power consumptions and thermal performance. Fig. 3 and Fig. 4 show the performance test of optical links and electrical links of the processor FPGAs at 12.8 Gb/s and 25.78125 Gb/s respectively. More details will be reported in the meeting.

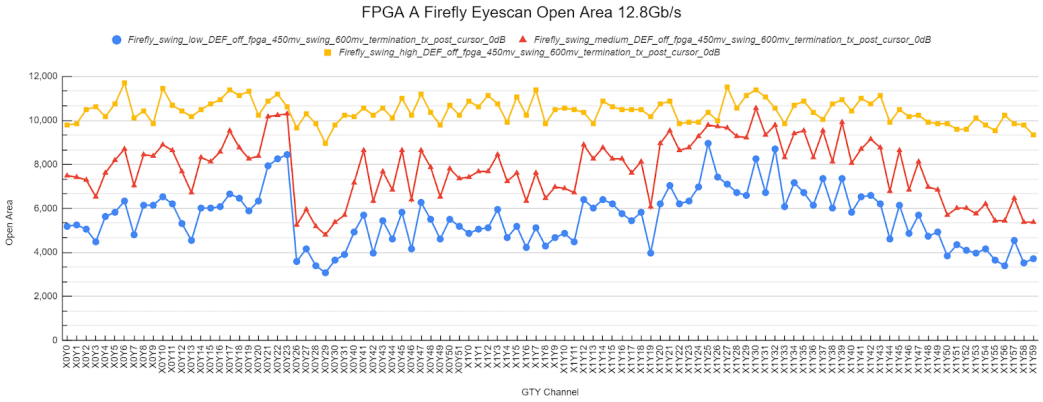

Fig.3 Eye scan results for all the optical links for Processor FPGA and FireFly modules.

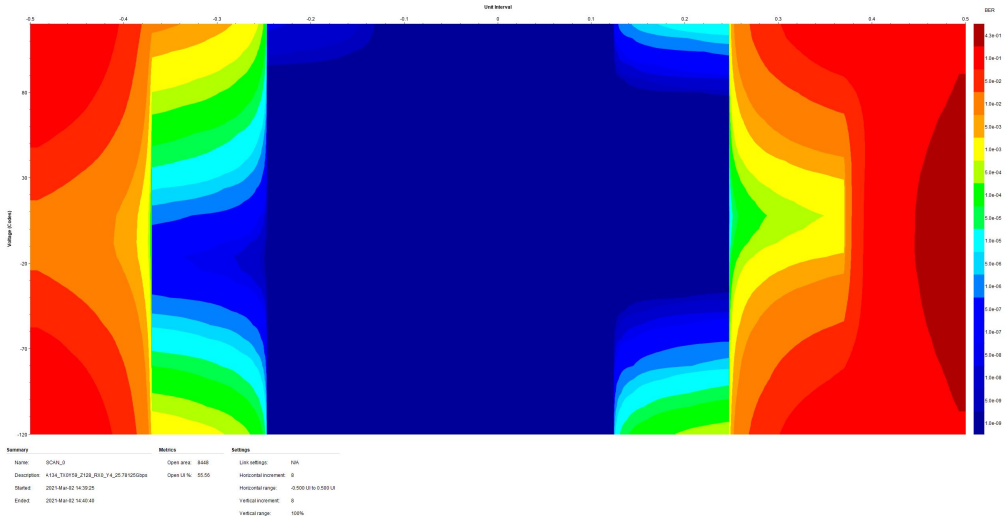

Fig.4 Typical eye diagram of the electrical links for Processor FPGA and at 25.78125 Gb/s.