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The ATLAS Electron Feature Extractor Module: Design, Manufacture and Test

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In Run 3, the ATLAS Level-1 Calorimeter Trigger (L1Calo) will be augmented by an Electron Feature Extractor (eFEX), which will identify isolated electron/photon and tau particles. Each eFEX module accommodates 424 signals at 11.2 Gb/s. Three generations of eFEX have been manufactured, and the design, manufacturing, and testing processes have been optimised. The firmware for the eFEX is managed using a custom system that has since been adopted by ATLAS TDAQ as the standard for the Phase-II upgrade. Presented here are the eFEX design, test results, and lessons learned from prototype and pre-production manufacturing.

Summary (500 words)

In Run 3, the ATLAS level-1 Calorimeter Trigger (L1Calo) will be augmented by new processing modules. Of these, the Electron Feature Extractor (eFEX), will identify isolated energy deposits in the calorimeter characteristic of electron/photon and tau particles, and achieve a higher discriminatory power than the previous trigger by running more complex algorithms on data of a higher granularity (ten E_T values for each tower of 0.1 × 0.1 in eta × phi).

The principle design challenges of the eFEX arise from the nature of the algorithms employed: over-lapping windows of data are processed in parallel, requiring data to be shared between modules. An efficient implementation requires a small number of modules of high bandwidth. Furthermore, sharing data across the module complicates the PCB design: data can be brought to a single FPGA using optical receivers placed close to that device, but longer tracks are necessary to transmit data to multiple FPGAs.

The resultant eFEX design is a 22-layer board with six micro-via layers. It houses 3942 tracks, including 424 pairs carrying signals of 11.2-Gb/s. The PCB material is Isola Itera. Four Processor FPGAs (Xilinx XC7VX550) implement the core of functionality. On the real-time trigger path, they synchronise the data across all inputs, run feature-extraction algorithms, sort the results across the four FPGAs and transmit them downstream, all within a latency of 13.4 ns. A fifth FPGA (XC7VX330T) implements the control and readout interfaces.

The firmware for the four Processor FPGAs is built in a single project using generic parameters and programmable registers to implement the different pinouts, mappings, and functions required. All of the firmware is managed using a custom, script-based, automated workflow, HDL On Git (HOG), which has since been adopted by ATLAS TDAQ as the standard firmware-management system for the Phase-II upgrade. It provides version management and Continuous Integration.

Prototype eFEX modules were built and tested successfully in 2016, but subsequently, the connectivity of the high-speed outputs was changed to take advantage of changes to the trigger system proposed for the Phase-II ATLAS Upgrade. The PCB stack-up was also changed to reduce the voltage drop across the module. A first pre-production run suffered PCB manufacturing problems (eventually resolved), and a second was conducted with a different manufacturer, which was then chosen for the full production run.

These experiences provided an opportunity to optimise the eFEX design flow further, to minimise the likelihood and impact of errors. The flow includes signal-integrity and power simulations, and time-domain reflectometry/transitometry tests. To facilitate the latter, specific tracks are included in the PCB design. These provide a better measure of layer impedances than coupons, due to variations in plating thickness over the panel.

Hardware tests of the eFEX show that the inputs have a bit error rate of less than 10ˆ-15 , and the noise, power, and cooling measurements are within specification. The firmware functionality has been tested as part of a full slice of the ATLAS L1Calo trigger, and the system will be installed in the summer of 2021.

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