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Ultra-low jitter clock distribution for the trigger electronics of the ATLAS New Small Wheel experiment.

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The low radiation levels on the outer rim of the New Small Wheels of the the ATLAS experiment gave the opportunity of utilizing commercial FPGAs for the trigger electronics of the sTGC detectors. The demanding requirements of the Xilinx FPGA transceivers in terms of jitter imposed the development of an ultra-low jitter clock distribution scheme. This scheme includes a custom board placed in the USA15 which distributes 32 clocks over 100 m fiber cables with a jitter of about 700fs. The design techniques for noise reduction and the results are presented.

Summary (500 words)

The LHC at CERN plans to have a series of upgrades to increase its instantaneous luminosity to 7.5×1034 cm−2s−1. The luminosity increase drastically impacts the ATLAS trigger and readout data rates. The innermost station of the ATLAS muon spectrometer, the so-called Small Wheels, will be replaced with a New Small Wheel (NSW) system, consisting of Micromegas (MM) and sTGC detectors, which is expected to be installed in the ATLAS underground cavern during the summer of 2021.
The low radiation levels on the rim of the ATLAS New Small Wheels gave the opportunity of utilizing commercial electronic chips (like Field Programmable Gate Arrays - FPGAs) for the trigger chain of the small-strip Thin Gap Chambers (sTGC) detectors. Those FPGAs require an ultra-low jitter clock for the proper operation of the Gigabit transceivers (4.8 Gb/s serial links). The initial design was based on a radiation tolerant ASIC fabricated at CERN but due to its intrinsic jitter and the high error rate on the transition lines, a different approach had to be chosen. The ASIC was replaced by a custom board named clock distributor based on commercial electronics like jitter cleaners and fanout chips. The new scheme can provide 32 low jitter clocks and achieves a total jitter of about 700 fs over 110 m of fiber cables. The clock distributor board and the whole path were evaluated and extensively tested. In this paper the design techniques for noise reduction and the results are presented.

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