

Hardware Design of the Generic Rear Transition Module for Global Trigger System of the ATLAS Phase II Upgrade

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In the ATLAS Phase-II upgrade, Global Trigger is a new subsystem that will bring event filter-like capability to the Level-0 trigger system. A common hardware platform in ATCA form factor named Global Common Module (GCM) is proposed to be configured as nodes in the Global Trigger. To mitigate the risk and simplify the GCM hardware design, a Generic Rear Transition Module (GRM) is developed. GRM, which is implemented with a Xilinx Versal Prime FPGA and sufficient multi-gigabit transceivers, aims at system control and communication with FELIX, it could also provide additional processing or readout capacity.

Summary (500 words)

The HL-LHC is expected to start operations in the middle of 2027, and to deliver more than ten times the integrated luminosity of the LHC Runs 1-3 combined (up to 4000fb⁻¹). Meeting this requirement poses significant challenges to the ATLAS TDAQ system. In the Trigger and Data Acquisition System upgrade, Global Trigger is a new subsystem, which will perform offline-like algorithms on full-granularity calorimeter data and bring Event Filter-like capability to the Level-0 trigger system.

The Global Trigger consists of three primary components: a MUX layer, a GEP layer, and a demultiplexing Global-to-CTP Interface, all of which use the same hardware implementation to minimize the complexity of the firmware, simplify the system design and improve maintainability. The identical hardware implementation is composed of a Global Common Module (GCM) and an optional Generic Rear Transition Module (GRM). Each pair of GCM and GRM could be configured as two nodes of MUX, GEP, or CTP. The GCM is an ATCA front board, which contains two big processor FPGAs and many multi-gigabit transceivers, used for the major data processing and transmission functions. GRM is an ATCA rear transition module, which contains a Xilinx Versal Prime FPGA and sufficient multi-gigabit transceivers, used for system control and communication with FELIX. Besides, the power consumption of GCM is limited to 350W by the cooling system. It is imposing significant constraints on power consumption, especially when GCM/GRM are used as GEP nodes, which need maximum resources of FPGA logic and transceivers. In this case, GRM is required to provide additional resources for event processing algorithms and data transmission.

To provide more programmable logic resources and transceivers, and achieve a better energy efficiency ratio, the Xilinx Versal Prime FPGA VM1802 is selected for the GRM design. Fig.2 shows the block diagram of GRM. GRM is connected to GCM through Zone3 connectors. Two Si5395 are used for clock cleaners and distributors, the clock source could be configured as the local clocks or remotely clocks from GCM or FELIX with flexibilities. Totally 18 transceivers between GCM and GRM's FPGA are implemented for monitoring, control, and data transmission. Two 12-channel transceivers via FireFly modules are used for communication with FELIX and other possible applications. In addition, there are 40 TX links from Zone3 connectors to expand the readout capability of nodes in the Global Trigger system. All transceivers and FireFly modules support data rate up to 25Gbps. A CERN MMC is used to monitor the health of the board in the ATCA chassis.

The hardware was designed in 2020 and is being tested since February 2021. Now the power rails and the TX links from GCM to GRM have been verified. GTY links from GCM to TX FireFly modules in GRM through Zone3 connectors could work well at 20Gbps. Fig.3 and Fig.4 show the performance of these links at 14Gbps. More progress and details will be reported in the meeting.

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