The NA62 liquid krypton electromagnetic calorimeter fast readout implementation and data taking performances

R. Ammendola, G. Paoluzzi, A. Salamon - INFN Sezione di Roma Tor Vergata
with the NA62 L0Calo detector subgroup

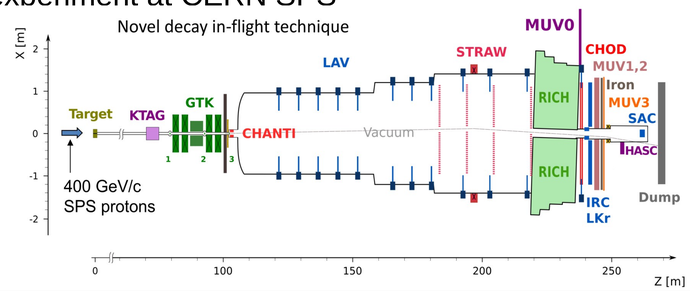
TWEPP2021
20-24 September 2021

Abstract

The NA62 experiment at the CERN SPS aims to measure the branching ratio of the very rare kaon decay $K^+ \to \pi^+ \nu \bar{\nu}$. The calorimeter level 0 trigger identifies clusters in the electromagnetic and hadronic calorimeters. Along with the trigger data sent to the L0 trigger processor, readout data is collected to be sent to L1 software trigger level. We present the novel implementation of the readout data collection and forwarding system in the multiple layers of the calorimetric trigger structure. As soon as the on-field installation and testing will be completed, we will do a performance evaluation of the new system measured in the current data taking session.

The NA62 experiment at CERN SPS

The NA62 experiment aims to measure the very rare kaon decay $K^+ \to \pi^+ \nu \bar{\nu}$, collecting O(100) events with a 10% background to make a stringent test of the Standard Model and deepen the knowledge of the CKM matrix. The $K^+ \to \pi^+ \nu \bar{\nu}$ decay is highly suppressed, well known from the theoretical standpoint and very sensitive to many New Physics models. The Standard Model branching ratio prediction for $K^+ \to \pi^+ \nu \bar{\nu}$ is $(8.4 \pm 1.0) \times 10^{-11}$.



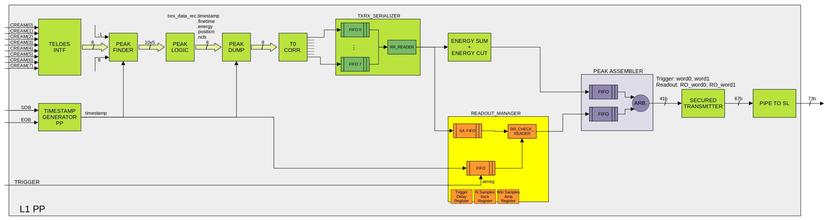
The Level-0 Calorimetric Trigger

The calorimeter level 0 trigger is used to suppress one of the main backgrounds, the $K^+ \to \pi^+ \nu \bar{\nu}$, decay, and to select events with a π^+ in the final state. The calorimeter level 0 trigger identifies clusters in the electromagnetic and hadronic calorimeters. It prepares time-ordered lists of reconstructed clusters together with the arrival timestamp, position, and energy measurements of each cluster. It also provides trigger decisions based on complex combinations of energy and cluster multiplicity. The main parameters of the trigger processor are the high design hit rate (30 MHz) and the required single cluster time resolution (1.5 ns).
The trigger recognizes electromagnetic/hadronic clusters in the calorimeters along with their position, fine-time and energy. The inputs are the Trigger Sum Links (TSL), sums of ADC values, sampled at 40 MHz, that are continuously sent by the CREAM modules. There are 864 TSL for the LKr, 1 for IRC, 1 for SAC, 12 for MUV1 and 6 for MUV2.

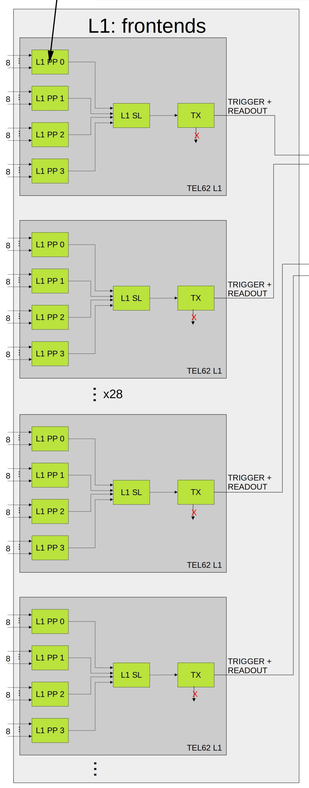
Calorimetric Trigger Processor at a glance: major modifications adding readout capabilities

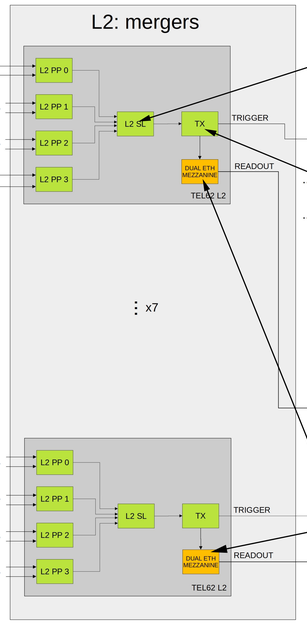
- The calorimeter trigger processor is a parallel system composed of 37 TEL62 boards, 111 mezzanines and 221 programmable devices housed in three 9U crates, performing data taking since 2015.
- Each board mounts 5 Altera Stratix III FPGAs: four, so called Pre-Processing (PP), receive and process data from input mezzanines and one, so called Sync-Link (SL), receives and process data from the PPs and sends them to the output mezzanine.
- An internal transmitter board (TX), mounting a Stratix II FPGA, allows cascading of multiple TEL62 boards.
- The calorimetric trigger is structured as a 3-layer system where each layer has a different number of TEL62:
  - L1: front-end layer (28 boards) where peaks are independently identified in 28 vertical slices of the calorimeter.
  - L2: merger layer (7 boards), where different peaks are horizontally merged when they are close in time and space
  - L3: concentrator layer (1 board), where data is collected and transmitted as trigger primitives to the central L0 Trigger Processor

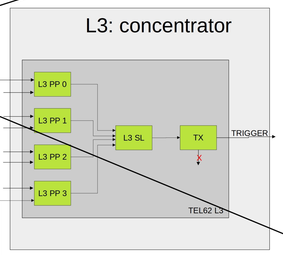
L1 PP Firmware

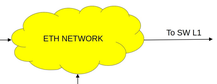


- The general idea is to store readout data as early as possible as it is generated in peak finder logic.
- Trigger signal is used to store timestamps of triggered data.
- Readout data is then selected and forwarded according to a customizable timestamp window.
- Trigger and Readout data needs to be multiplexed in the same communication channels.



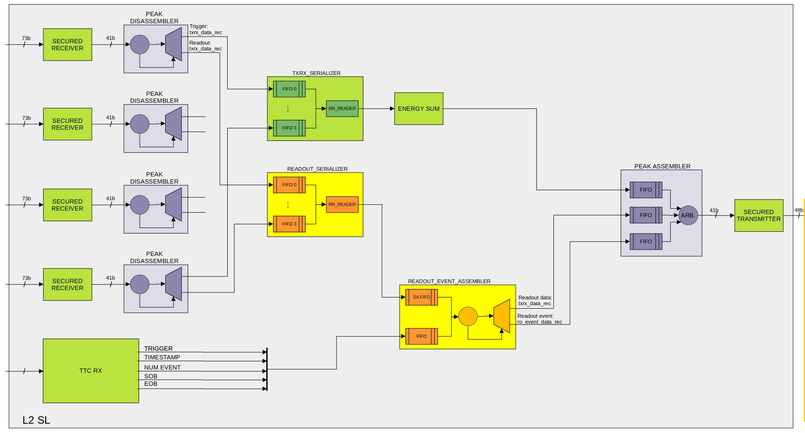






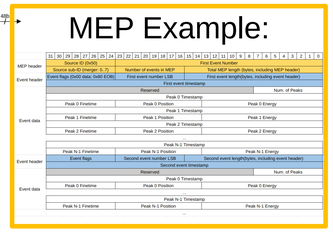
Adding Readout channel towards L1 software trigger level:
- Modifications need to be performed in L1 and L2 PP, SL and TX FPGA firmware.
- A custom designed dual Gigabit Ethernet mezzanine card has been developed to be mounted in L2 merger layer (7 cards in total).
- In the logic diagrams:
  - Yellow boxes indicates new logic blocks
  - Purple boxes indicates existing modified blocks

L2 SL Firmware



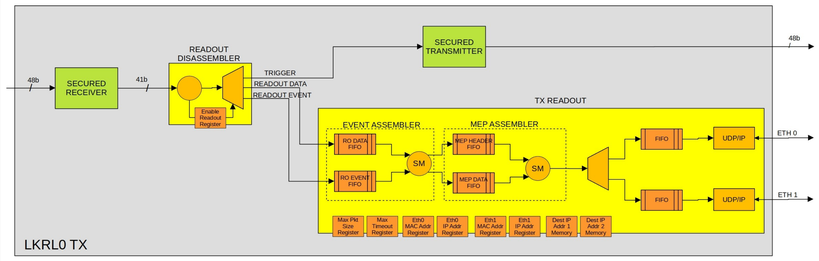
- An event header must be prepared at this level in order to embed information such as event timestamp, number of event, etc..
- Timestamp matching logic is needed in order to create zero-peaks events
- Event data is multiplexed on same communication channel

MEP Example:



Dual Gbit Mezzanine Card

TX Firmware



- Data is de-multiplexed among trigger, readout and readout event data kinds.
- Trigger data path continues to higher level.
- Readout event data is used to assembly a readout event, with 0, 1 or multiple peaks in space.
- Events are grouped in multiple events packets (MEP), using the experiment current TDAQ data format.
- MEPs are sent to PC farm using 2 Ethernet links with UPD/IP protocol.

Conclusions

- Working with existing, aged and running in production hardware needs special care
- Must preserve existing logic and timing
- Limited hardware add-on possibilites
- In the next weeks mezzanine deployment will be completed and performance test will be completed on production environment