

The NA62 liquid krypton electromagnetic calorimeter fast readout implementation and data taking performances

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The NA62 experiment at the CERN SPS aims to measure the branching ratio of the very rare kaon decay $K^+ \rightarrow \pi^+ \nu \bar{\nu}$. The calorimeter level 0 trigger identifies clusters in the electromagnetic and hadronic calorimeters. Along with the trigger data sent to the L0 trigger processor, readout data is collected to be sent to L1 software trigger level. We present the novel implementation of the readout data collection and forwarding system in the multiple layers of the calorimetric trigger structure. We will also present the performance evaluation of the new system that will be measured in the incoming data taking.

Summary (500 words)

The NA62 experiment aims to measure the very rare kaon decay $K^+ \rightarrow \pi^+ \nu \bar{\nu}$, collecting $O(100)$ events with a 10% background to make a stringent test of the Standard Model and deepen the knowledge of the CKM matrix. The $K^+ \rightarrow \pi^+ \nu \bar{\nu}$ decay is highly suppressed, well known from the theoretical standpoint and very sensitive to many New Physics models. The Standard Model branching ratio prediction for $K^+ \rightarrow \pi^+ \nu \bar{\nu}$ is $(8.4 \pm 1.0) \times 10^{-11}$.

The calorimeter level 0 trigger is used to suppress one of the main backgrounds, the $K^+ \rightarrow \pi^+ \pi^0$ decay, and to select events with a π^+ in the final state. The calorimeter level 0 trigger identifies clusters in the electromagnetic and hadronic calorimeters. It prepares time-ordered lists of reconstructed clusters together with the arrival timestamp, position, and energy measurements of each cluster. It also provides trigger decisions based on complex combinations of energy and cluster multiplicity. The main parameters of the trigger processor are the high design hit rate (30 MHz) and the required single cluster time resolution (1.5 ns). The calorimeter trigger processor is a parallel system composed of 37 boards, 111 mezzanines and 221 programmable devices housed in three 9U crates.

Until now, only trigger data was available to L0 trigger processor, while readout data was not used at L1 software trigger layer. The implementation of the readout datapath towards L1 has now been deployed, in order to enhance data acquisition efficiency and refine trigger decision between hardware L0 and software L1 trigger layers.

At the early stage in the first hardware layer, the trigger signal arriving from L0 Trigger processor is used to collect timestamps of the triggered data, calculated with proper delay offset. Readout data from CREAM modules are stored in proper buffers (separated from trigger data line), and data timestamps are matched within a programmable window. Selected data is then forwarded and reduced at the higher levels, using the same data path as the trigger data lines with proper traffic priority rules; this expedient allows using completely the same hardware already deployed, except from a mezzanine card at the second hardware layer, implementing dual Gbit ethernet interface that has been added later. Data packets are thus sent to software trigger layers in order to enhance data selection.

The new fast readout system will be put on-line in the experiment with the beginning of 2021 data taking run. Performance measurement will be carried out, in order to check readout and trigger data integrity with increasing beam intensity.

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