LAr calorimeter R&D for FCC-ee

Readout Electrode Studies

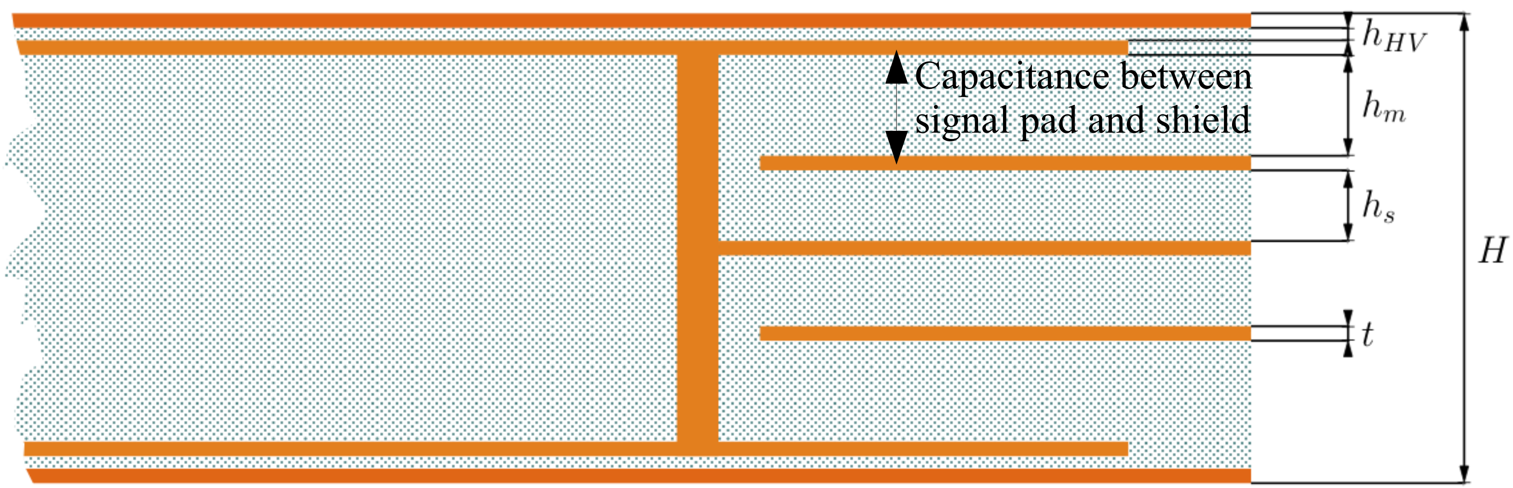
Brieuc François (CERN)
LAr Calo for FCC working meeting
April. 1st, 2021

FUTURE CIRCULAR COLLIDER

CERN

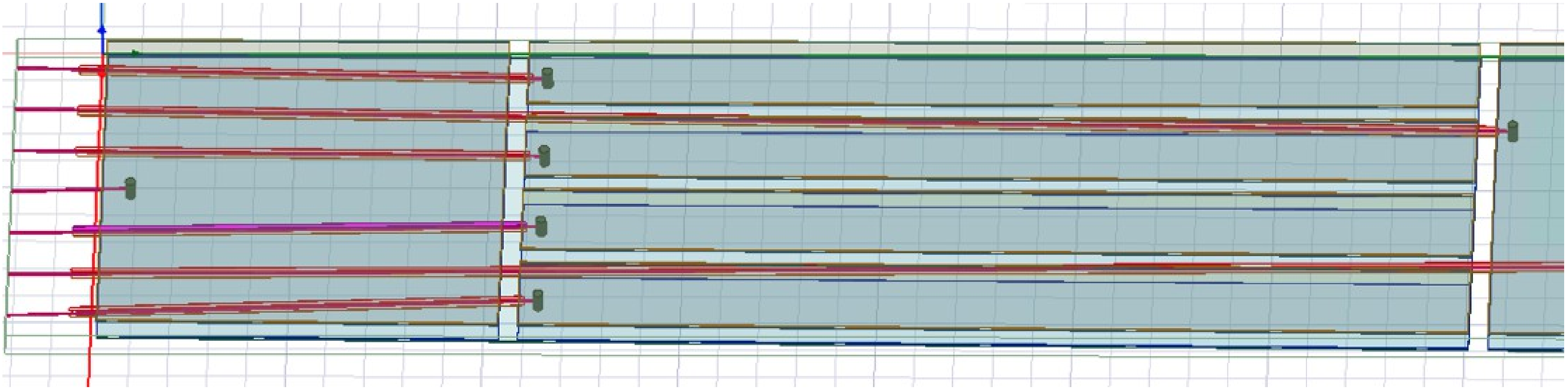
Introduction

- FCC-ee physics program would greatly benefit from measuring low energy (~300 MeV) photons
- Noise term dominates for low energies $$\frac{\sigma_E}{E} = \frac{a}{\sqrt{E}} \oplus \frac{b}{E} \oplus c$$
- A fraction of this noise comes from the signal pad capacitance to ground
  - Important to precisely evaluate these capacitances



ANSYS

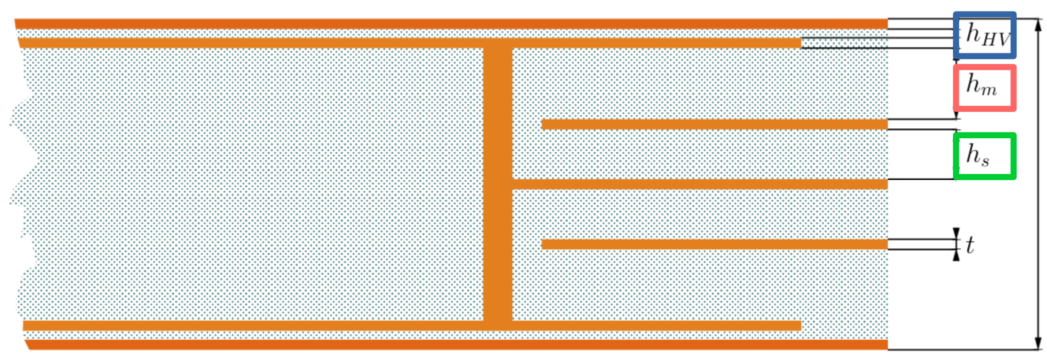
- ANSYS (mutli-physics software) EM Desktop
  - Includes SIWave (signal integrity), Maxwell (finite element solver of Maxwell equations), and much more
  - Plan: derive capacitance from Maxwell, derive S parameters from another tool (or an equivalent circuit)
- The cadence model could be imported into ANSYS Maxwell
  - Different procedure than for ANSYS SIWave (needed a different dataformat)
  - Cadence model was too detailed to be solved in Maxwell
    - All vias have been changed to plain copper cylinder
    - Removed the via at the end of the signal trace (no impact on capacitance)
    - Removed the ground plates



PCB geometrical parameters

- Trace thickness: 35 um
- Trace width: 127 um
- Shield width: 250 um
- Assumptions
  - No E field solver inside copper
    - Tried with, takes longer to compute and does not change the result
  - FR4 as perfect insulator
- FR4 permittivity: 4.4
- Capacitance derivation
  - One volt is applied to a single conductor and zero volts is applied to all other conductors
  - Solve the electrostatic field and get capacitance from energy stored in the electric field

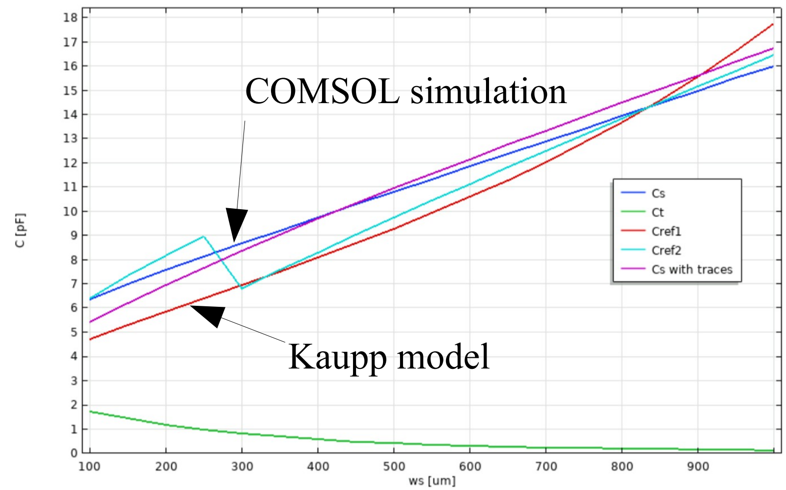
Name	Type	Negative	Material	Dielectric Fill	Thickness	Etch	Rough	Solver	Lower	Upper	Transparency
smt	dielectric		FR4_epoxy		0um			☐	1.285mm	1.285mm	60
top	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	1.25mm	1.285mm	60
dielectric_0	dielectric		FR4_epoxy		100um			☐	1.15mm	1.25mm	60
l2	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	1.115mm	1.15mm	60
dielectric_1	dielectric		FR4_epoxy		250um			☐	0.865mm	1.115mm	60
l3	signal	☑	copper	FR4_epoxy	35um		☐	☐	0.83mm	0.865mm	60
dielectric_2	dielectric		FR4_epoxy		170um			☐	0.66mm	0.83mm	60
l4	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	0.625mm	0.66mm	60
dielectric_3	dielectric		FR4_epoxy		170um			☐	0.455mm	0.625mm	60
l5	signal	☑	copper	FR4_epoxy	35um		☐	☐	0.42mm	0.455mm	60
dielectric_4	dielectric		FR4_epoxy		250um			☐	0.17mm	0.42mm	60
l6	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	0.135mm	0.17mm	60
dielectric_5	dielectric		FR4_epoxy		100um			☐	0.035mm	0.135mm	60
bottom	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	0mm	0.035mm	60
smb	dielectric		FR4_epoxy		0um			☐	0mm	0mm	60

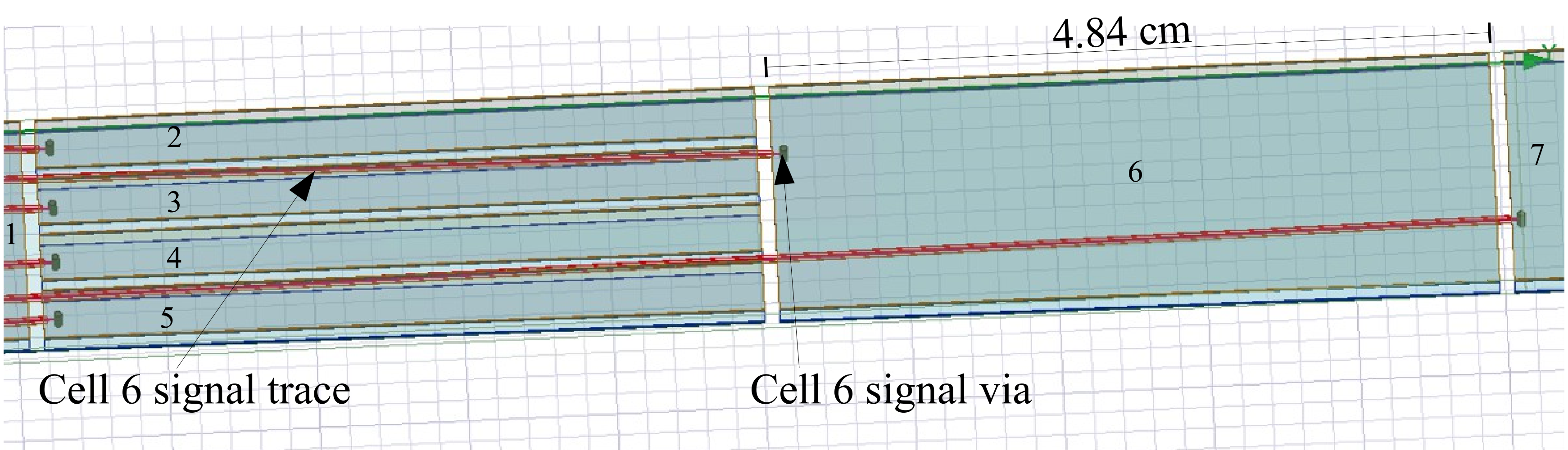


Was 285 in the Calo for FCC-hh paper

Validation

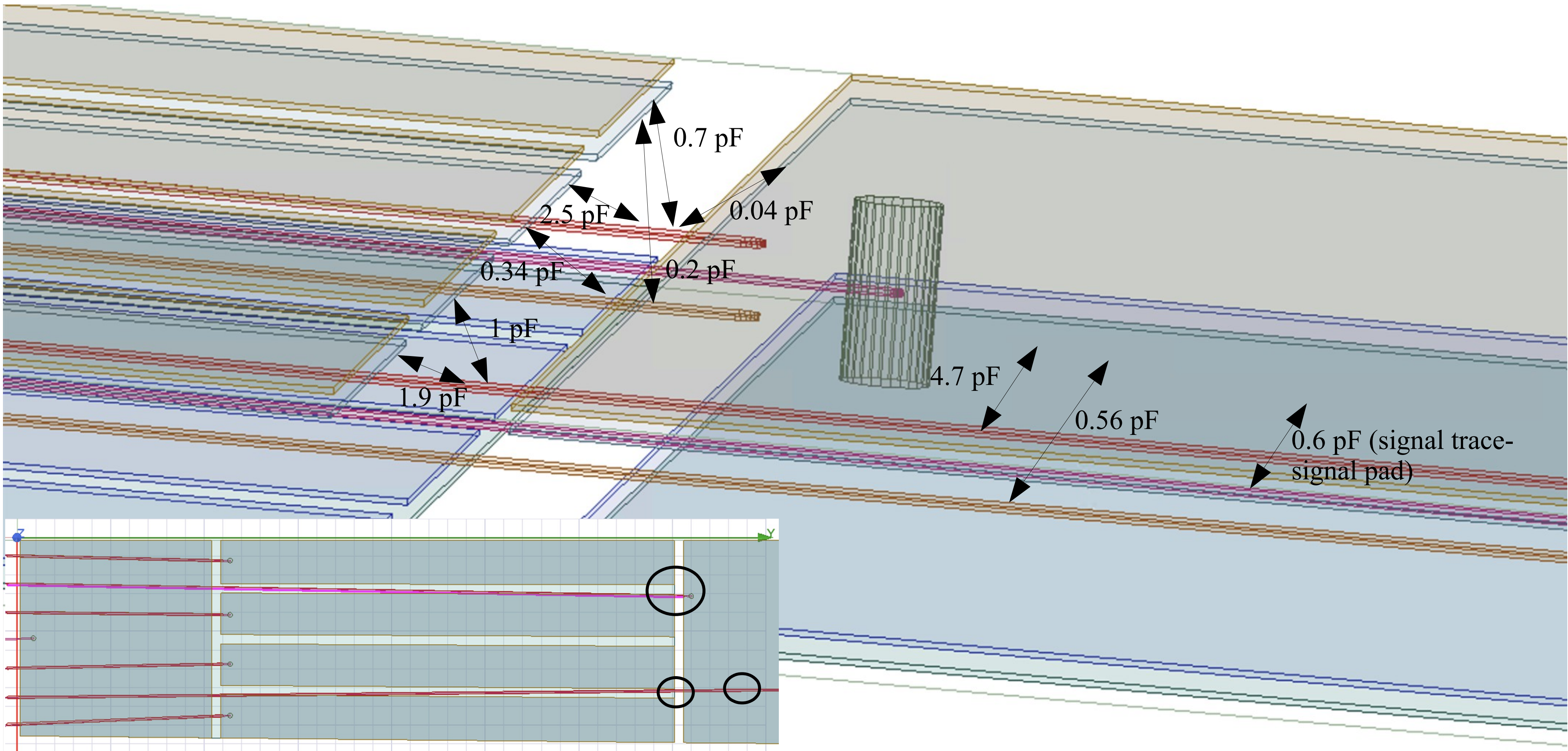
- Derive capacitance for only one shield and one signal pad (cell 6) – setting all other conductors as dielectric
  - Capacitance from Maxwell: 7 pF
  - Capacitance from analytical formula (link): 5.64 pF
    - Seems reasonable
      - COMSOL comparison also showed that the analytical model undershoots the capacitance
      - Asked for 5% accuracy in the Maxwell solver





Shield capacitance

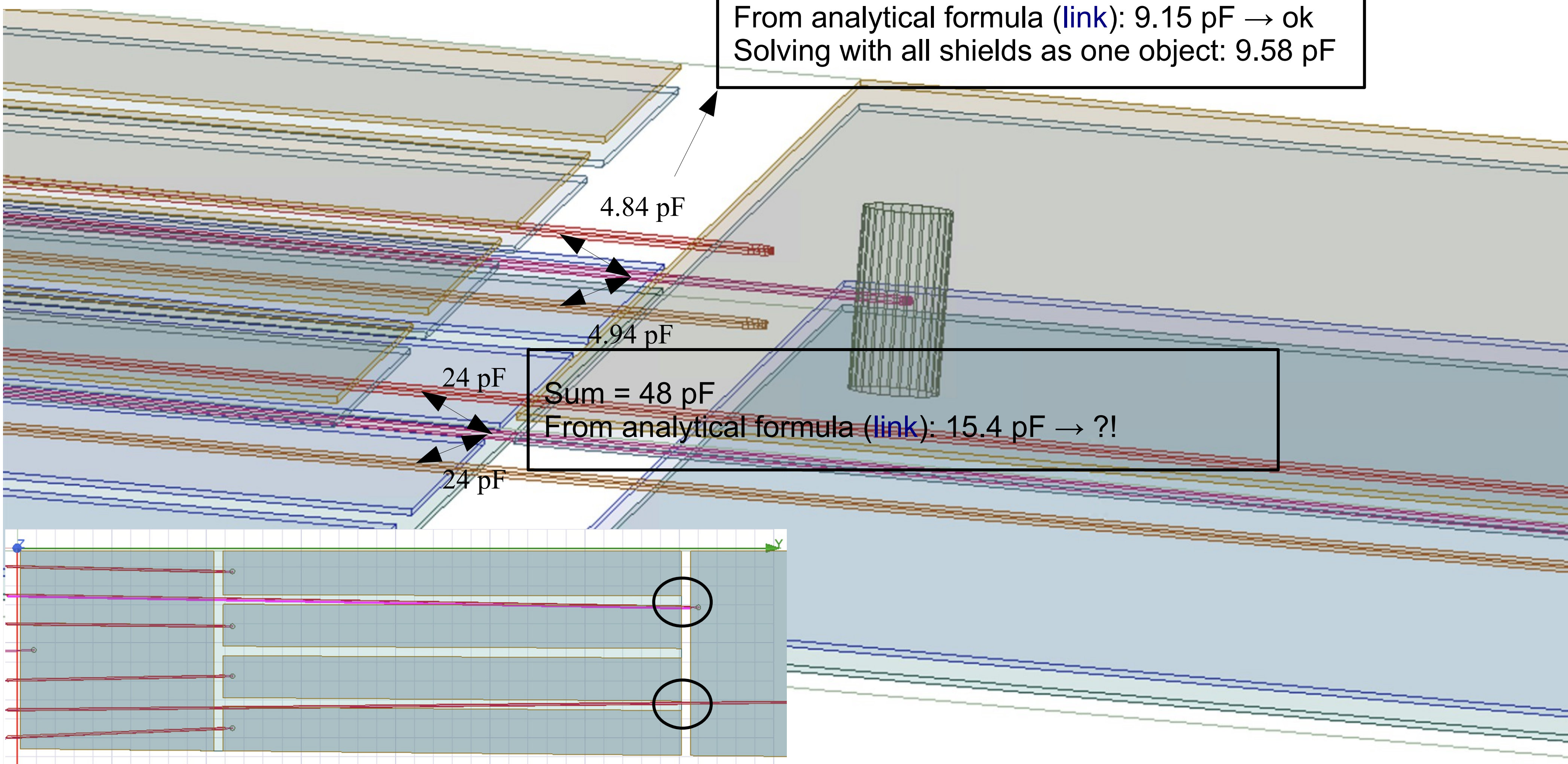
- Signal pad / shield capacitances up to cell 7 – HV plates as floating conductor
  - Running the shield below the pad separation minimizes the noise in the strip cells
  - Capacitance between shield **bottom** and signal pad **top** is O(10%) of the capa(shield **top**, signal pad **top**)



Strip line capacitance

- Technical issue faced
  - Strip-line capacitances

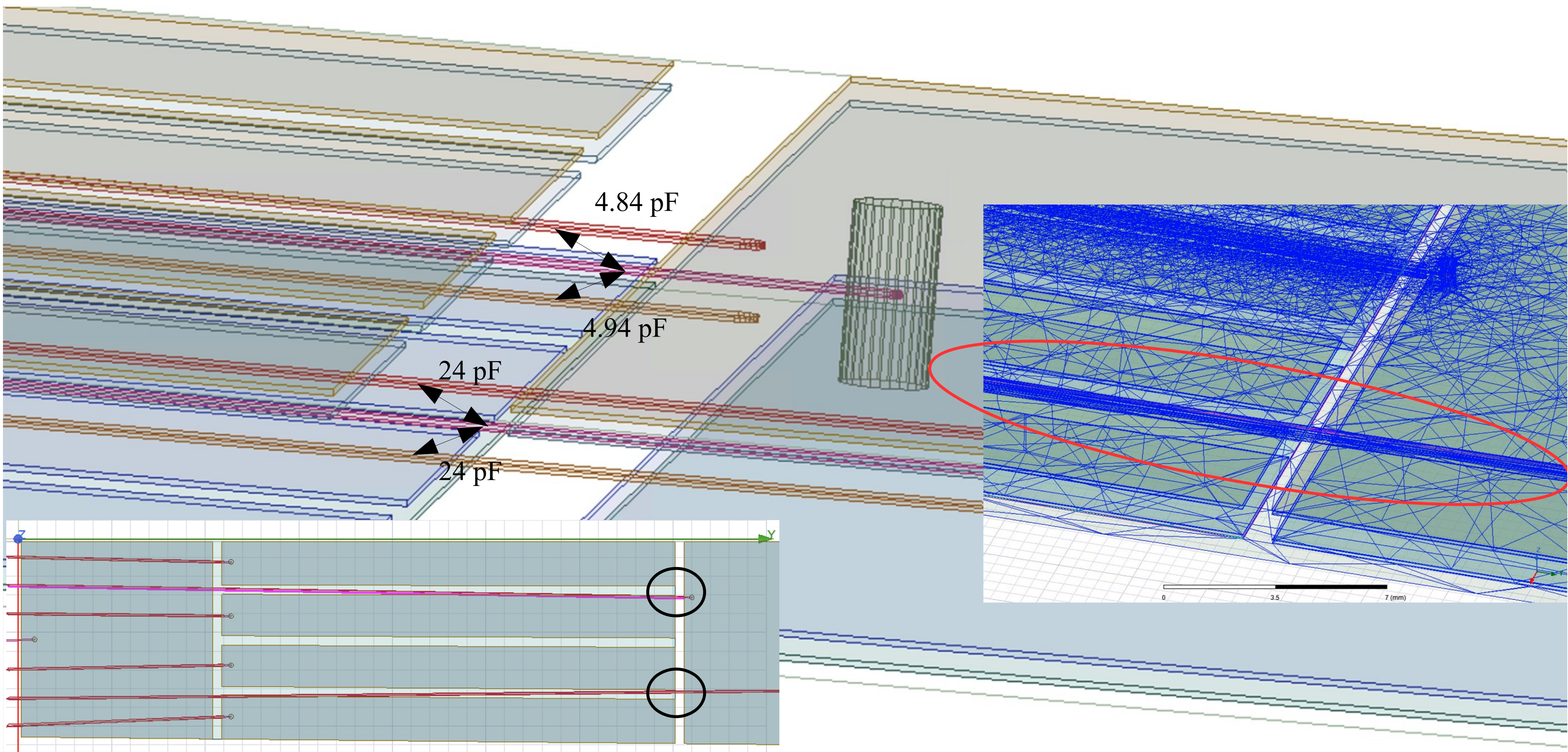
Sum = 9.78 pF
From analytical formula (link): 9.15 pF → ok
Solving with all shields as one object: 9.58 pF



Sum = 48 pF
From analytical formula (link): 15.4 pF → ?!

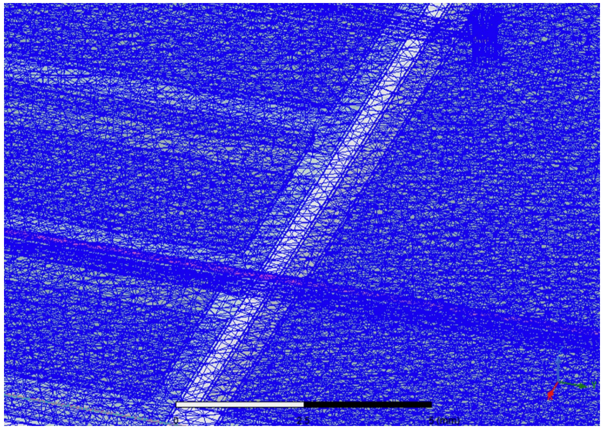
Strip line capacitance

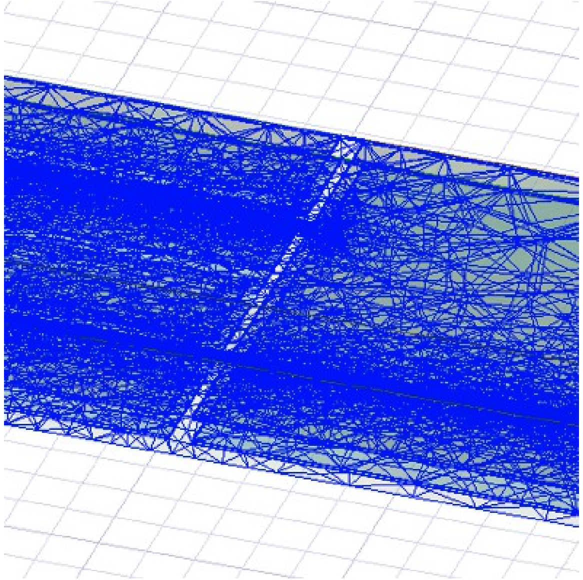
- Mesh is way less dense in the cell 7 region



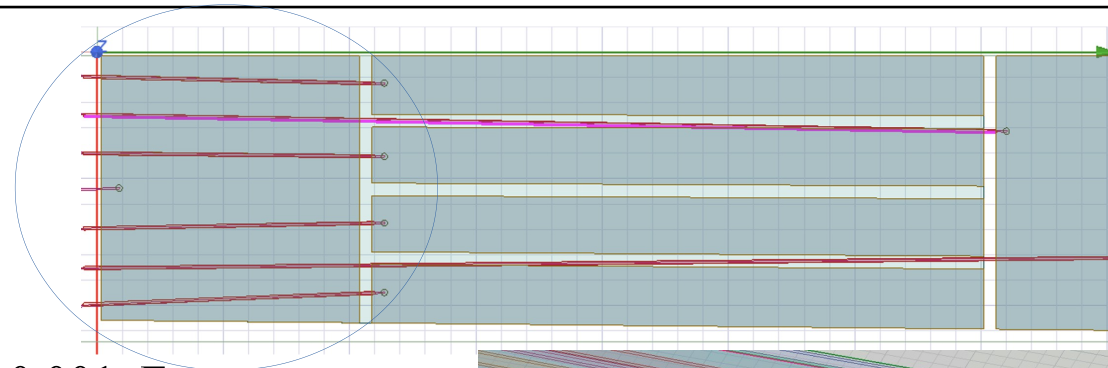
Solving the mesh issue

- Trials to solve the meshing issue
  - Lower relative error to 1% Í
  - Choose another meshing 'strategy' than the default Í
  - Impose maximal segment length in the mesh (0.5 mm)
    - Applied to the whole volume, even far from copper
    - Insufficient memory to solve Í
  - Can create a fictive region (i.e. not included in the Maxwell solver) and impose the segment length only there ð
  - In order to have an object in the capacitance matrix, one has to set a voltage to him, assigning different voltage values to close-by objects seems to increase mesh density between them ð
- Lesson learned: always check the mesh, the criteria on relative error to reach is not sufficient
- New capacitance between the cell 7 shield and signal trace: 7.6 pF (sum = 15.2, analytical formula: 15.4 pF)

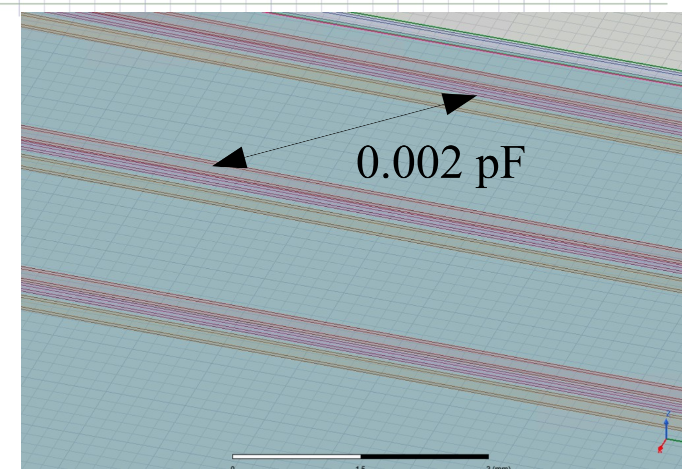




Capacitance extrapolation



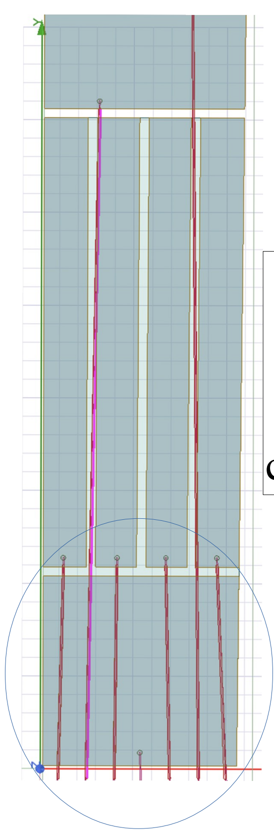
- Cell 1 capacitance with shields
  - Signal pad bottom(top): 14 pF
  - Signal via capacitance is negligible: 0.001pF



- Capacitance between signal trace and adjacent shields is also negligible
- If we assume that the signal trace capacitance to ground can be neglected (match impedance)
  - Can derive the capacitance between signal pad and shield "per length unit" and get the whole capacitance based on cell length and number of shield
  - Will probably have to consider one exception for strip cells where shields run beneath the etch
- Avoids to enter manually all the capacitance from Maxwell (way more flexible)!

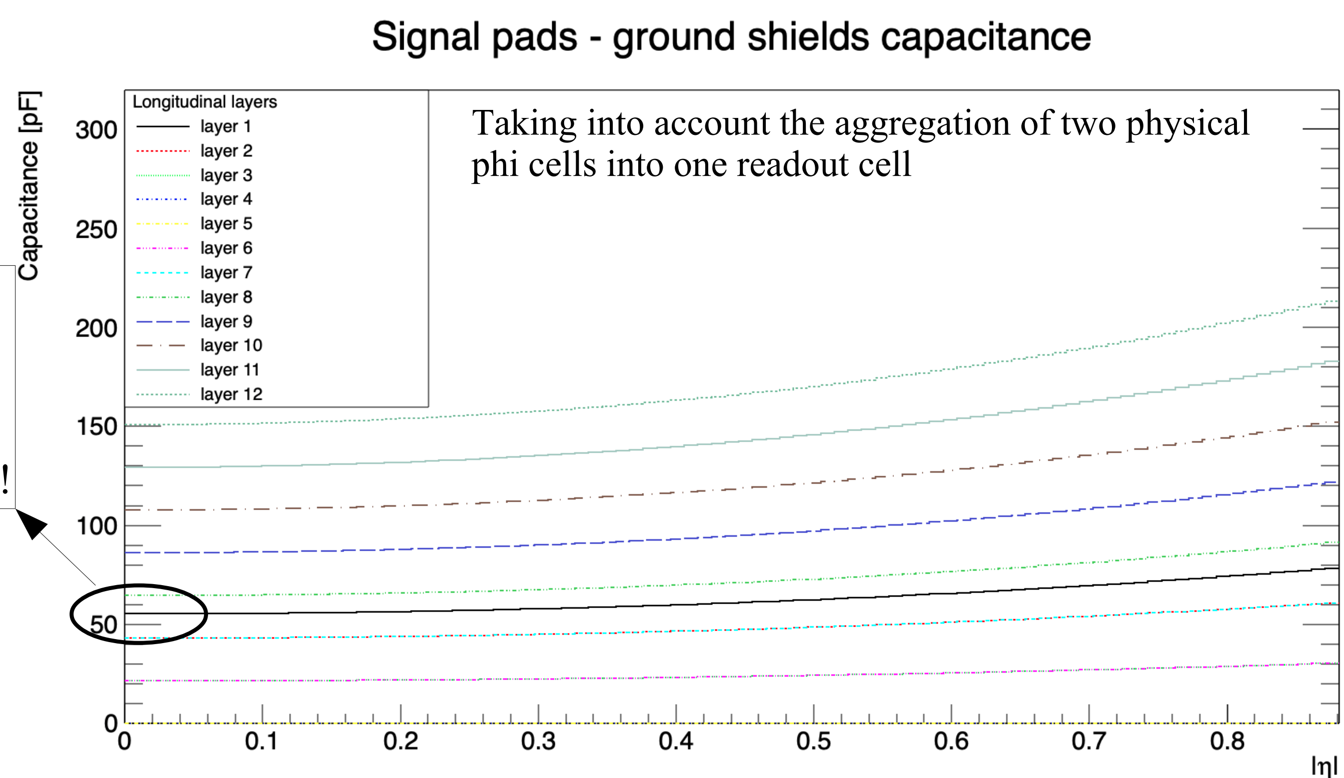
Capacitance extrapolation

- Capacitance of one signal pad to shield (cumulating top and bottom shield contribution) from cell 6: 5.07 pF / 48.43 mm = 0.109 pF/mm
  - Obtained with a good meshing
- Extrapolation to the full detector from capacitance per length unit (thanks Jana!)



14 * 2 * 2 = 56 pF
Very good agreement between Maxwell and the extrapolation of capacitance per length !

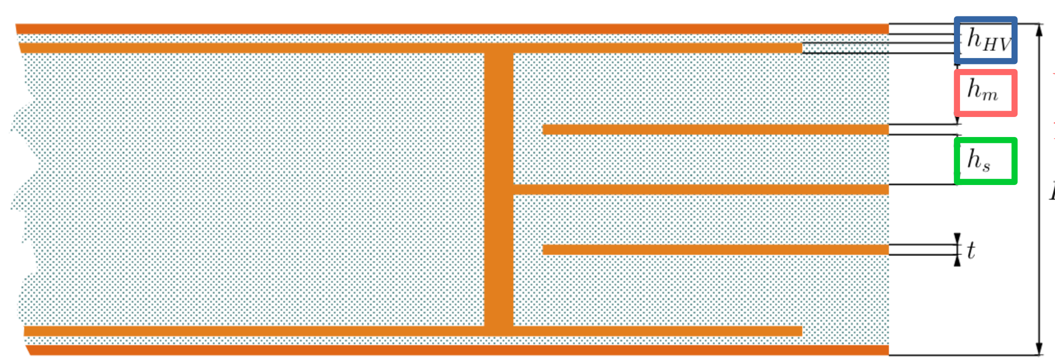
14 pF per pad from Maxwell



PCB thickness

- Decided for now to keep a total PCB thickness of 1.2 mm
  - Re-compute the capacitance per unit length with reduced distance between signal pad and shield (207.5 µm instead of 250 µm)
  - 0.123 pF/mm instead of 0.109 pF/mm

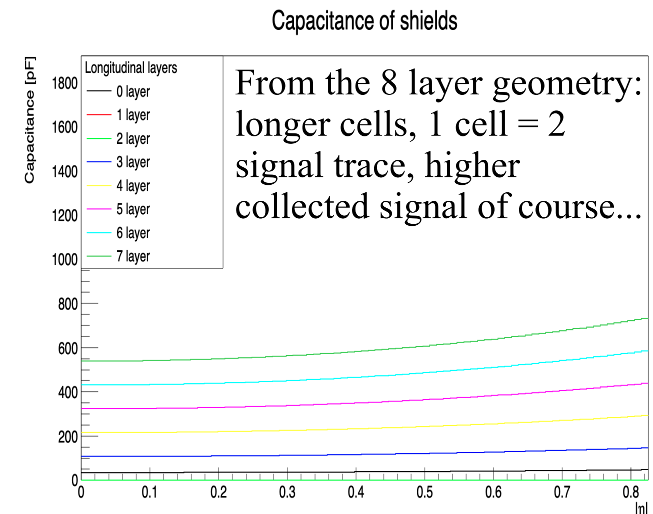
	Name	Type	Negative	Material	Dielectric Fill	Thickness	Etch	Rough	Solver	Lower	Upper	Transparency
	smt	dielectric		FR4_epoxy		0um			☐	1.285mm	1.285mm	60
	top	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	1.25mm	1.285mm	60
	dielectric_0	dielectric		FR4_epoxy		100um			☐	1.15mm	1.25mm	60
	l2	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	1.115mm	1.15mm	60
	dielectric_1	dielectric		FR4_epoxy		250um			☐	0.865mm	1.115mm	60
	l3	signal	☑	copper	FR4_epoxy	35um		☐	☐	0.83mm	0.865mm	60
	dielectric_2	dielectric		FR4_epoxy		170um			☐	0.66mm	0.83mm	60
	l4	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	0.625mm	0.66mm	60
	dielectric_3	dielectric		FR4_epoxy		170um			☐	0.455mm	0.625mm	60
	l5	signal	☑	copper	FR4_epoxy	35um		☐	☐	0.42mm	0.455mm	60
	dielectric_4	dielectric		FR4_epoxy		~~250um~~ → 207.5 um			☐	0.17mm	0.42mm	60
	l6	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	0.135mm	0.17mm	60
	dielectric_5	dielectric		FR4_epoxy		100um			☐	0.035mm	0.135mm	60
	bottom	signal	☐	copper	FR4_epoxy	35um	☐	☐	☐	0mm	0.035mm	60
	smb	dielectric		FR4_epoxy		0um			☐	0mm	0mm	60

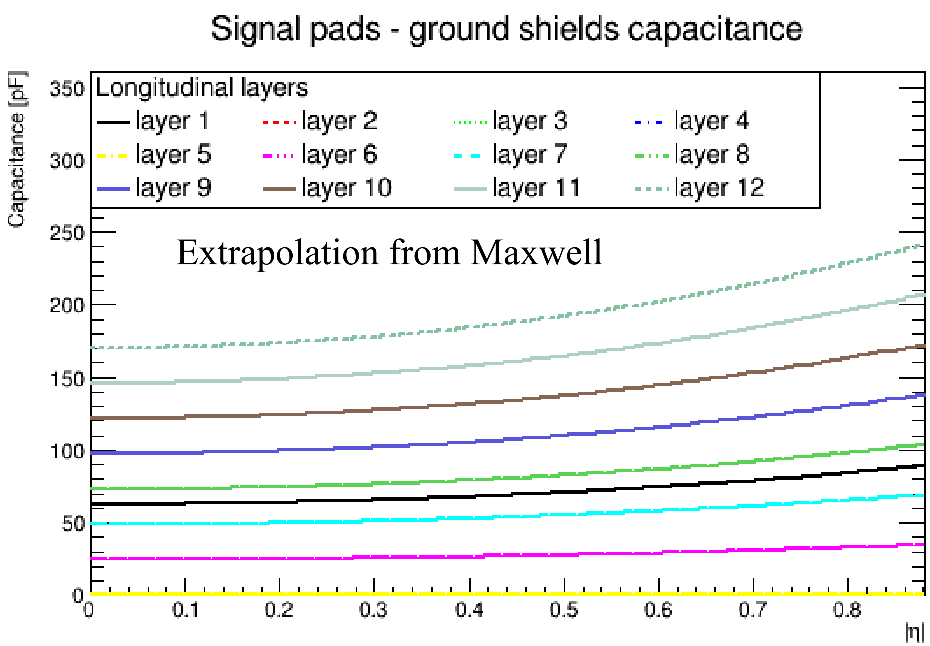


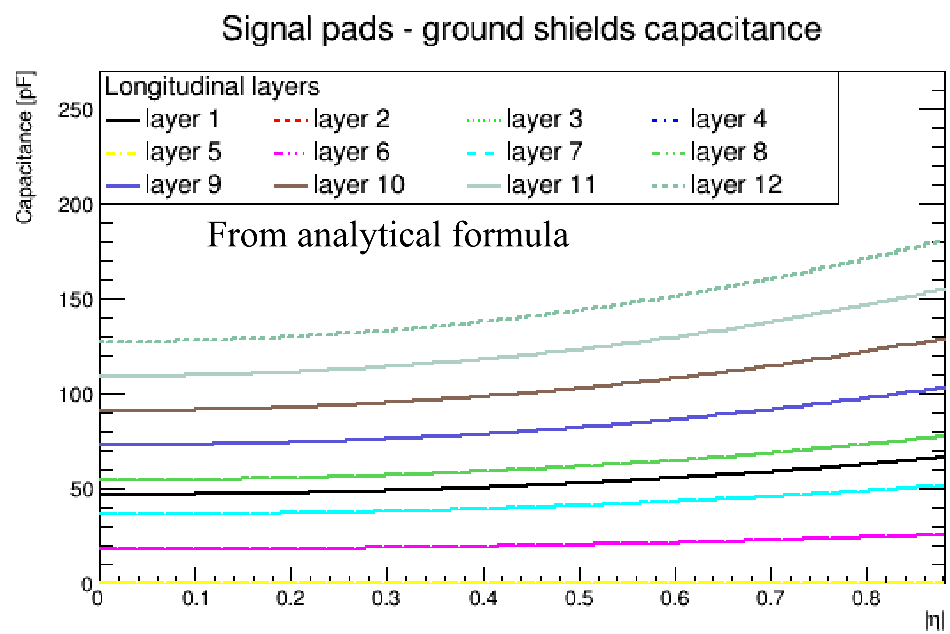
Was 285 in the Calo for FCC-hh paper

'Final' capacitance

- Capacitance with 1.2 mm thick PCB
- Comparison with the analytical formula
  - Maxwell extrapolation leads to ~30% higher capacitances
    - Analytical micro-strip capacitance is underestimated (also observed in the previous COMSOL simulation)
    - Bottom shield also contributes
    - The presence of other conductors has an impact
- Much lower capacitance compared to the previous geometry

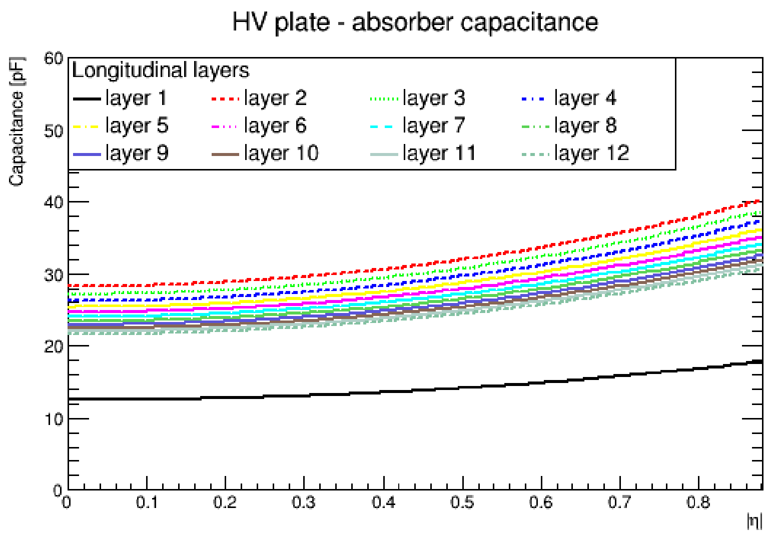






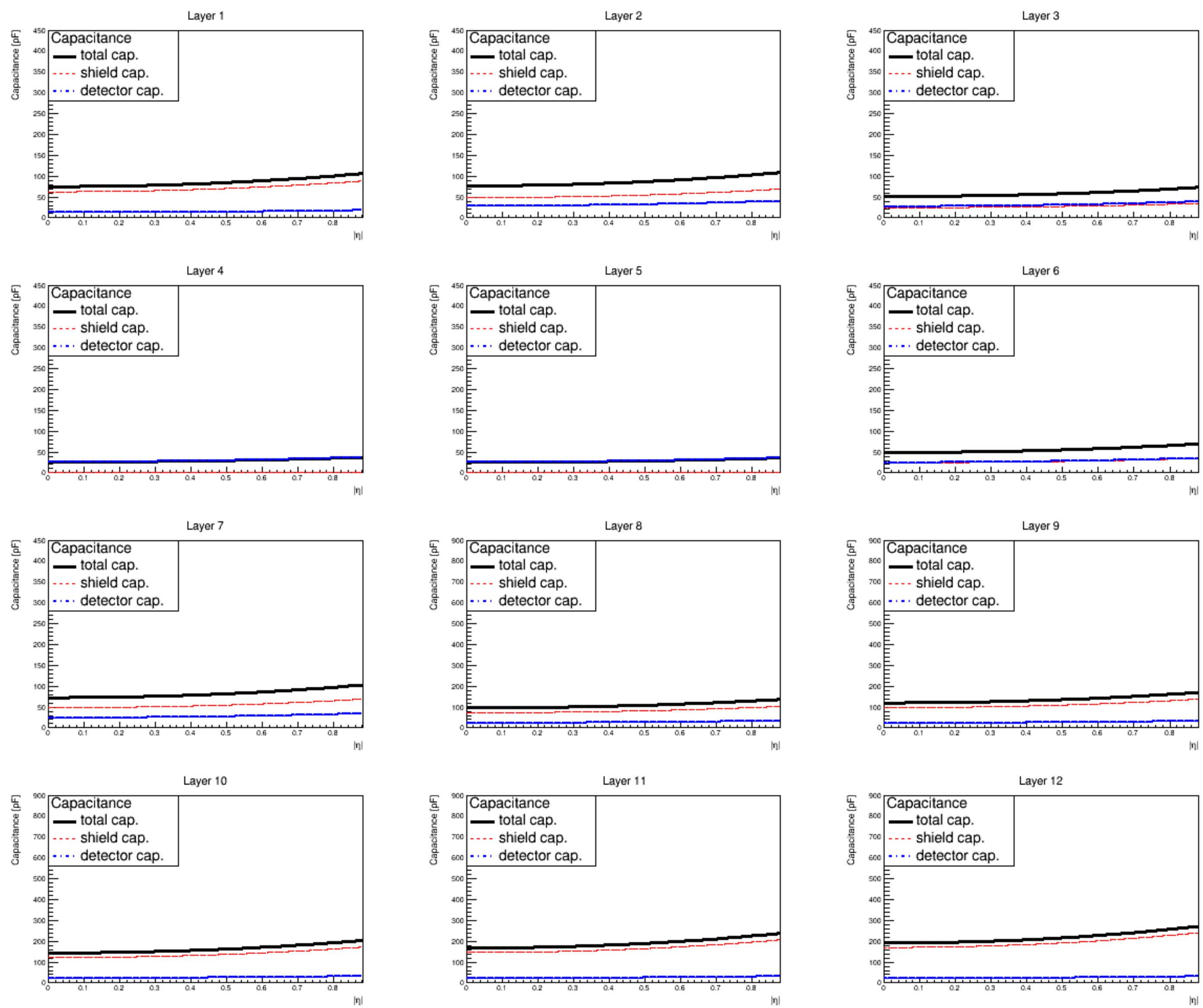
Noise estimation

- Noise estimation
  - $C_{total} = C_{shield} + C_{detector}$
  - $C_{detector}$ due to capacitance between HV plates and grounded absorber ~ 20-40 pF
    - Derived from analytical formula only – capacitance between two plates (less complex environment than for the shields)
    - Decreases with increasing radius (compensating effects: larger LAr gap + bigger surface)



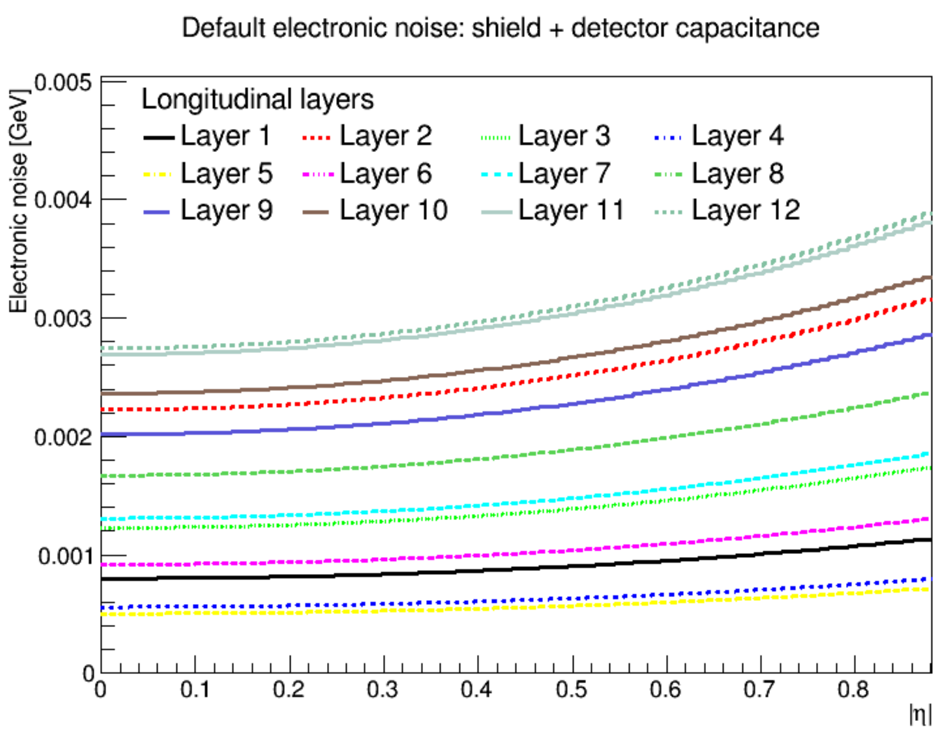
Total capacitance

- Total capacitance
  - 50-300 pF
  - Dominated by shield capacitance except in layer 3 to 6



Noise estimation

- Noise estimation
  - Extrapolation from ATLAS noise/capa
  - 25 MeV for 1400 pF → 0.018 MeV/pF
  - Rescale by the sampling fraction ratio between ATLAS (0.18) and our per layer values
  - Result: 0.5 – 4 MeV noise



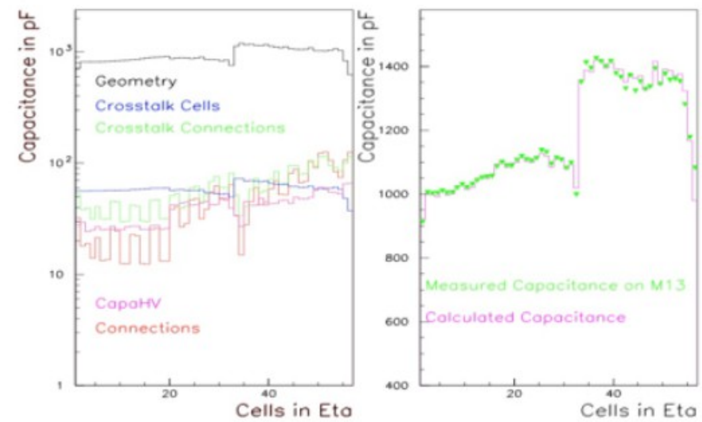
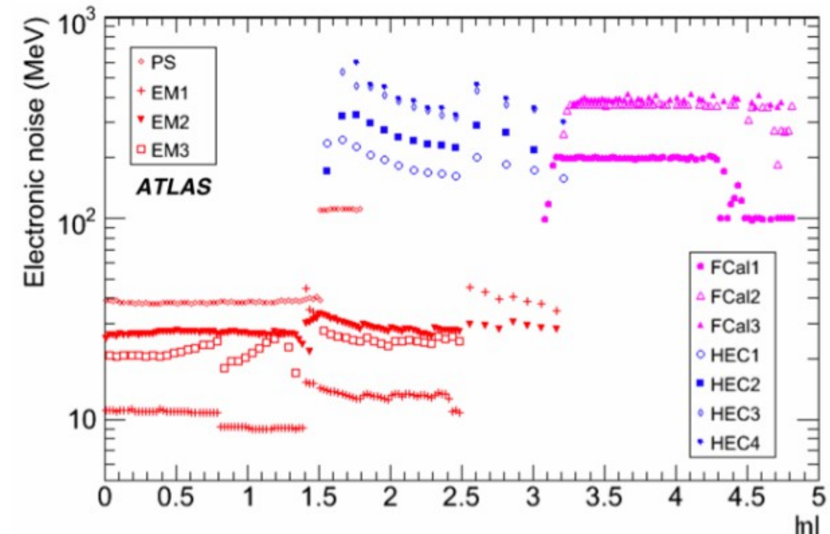


Figure 10: Left: expected constributions to cell capacitances as a function of η. Right: Total expected capacitance as a function of η and comparison with measurements done on M13 module. The agreement is very fair.

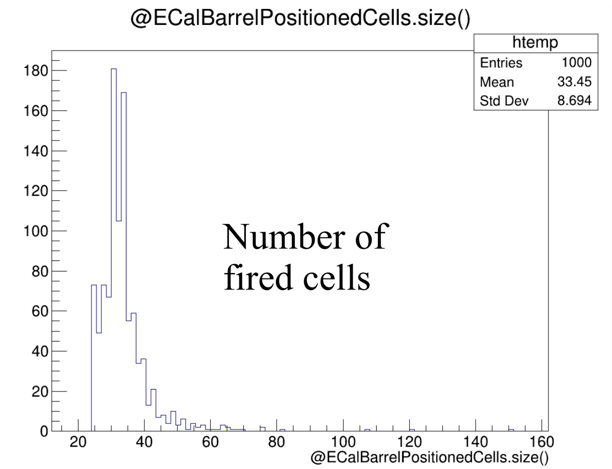
→ ATLAS middle cells (EM2): ε_r x 1nF = 1.4nF

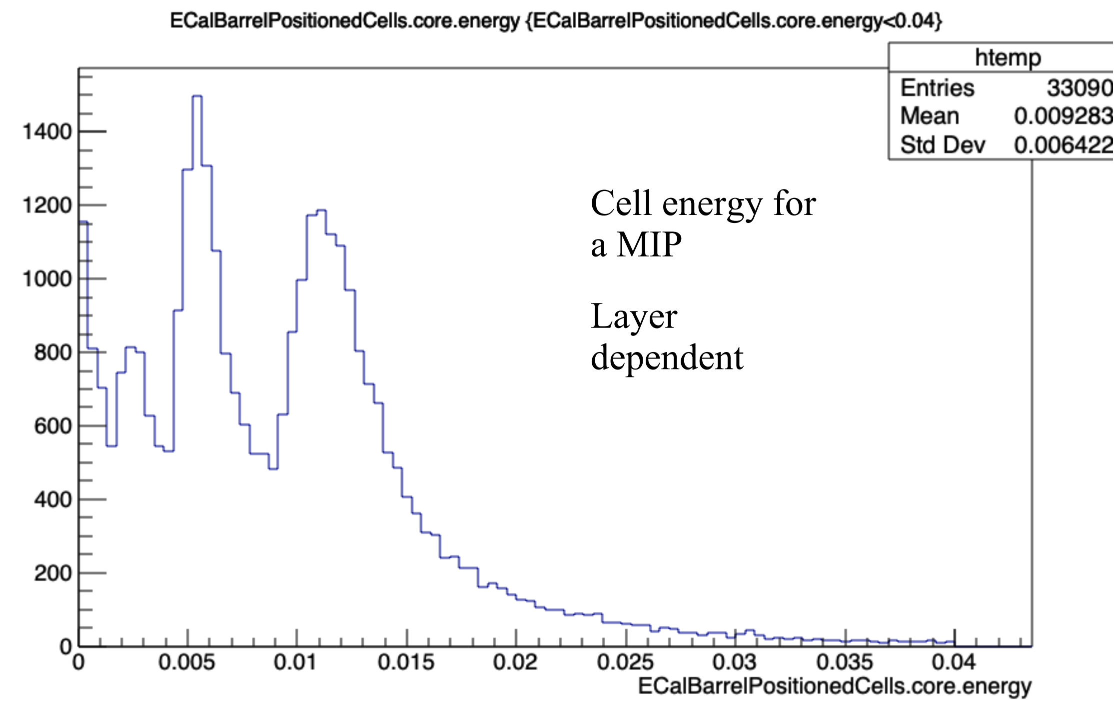


→ ATLAS EM2: 1.4nF → 25MeV noise

MIP energy deposit

- MIP energy deposit per cell
  - No signal attenuation considered, no digitization (energy taken directly from Geant4 deposit and scaled with sampling fraction) – all layers considered together
  - MIP energy deposit seems to be on the edge compared to the noise value BUT
    - Has to be studied layer per layer
    - MIP particle can be identified by some kind of 'tracking'
    - e.g. summing cell energy compatible with track patterns
      - Noise will sum in quadrature





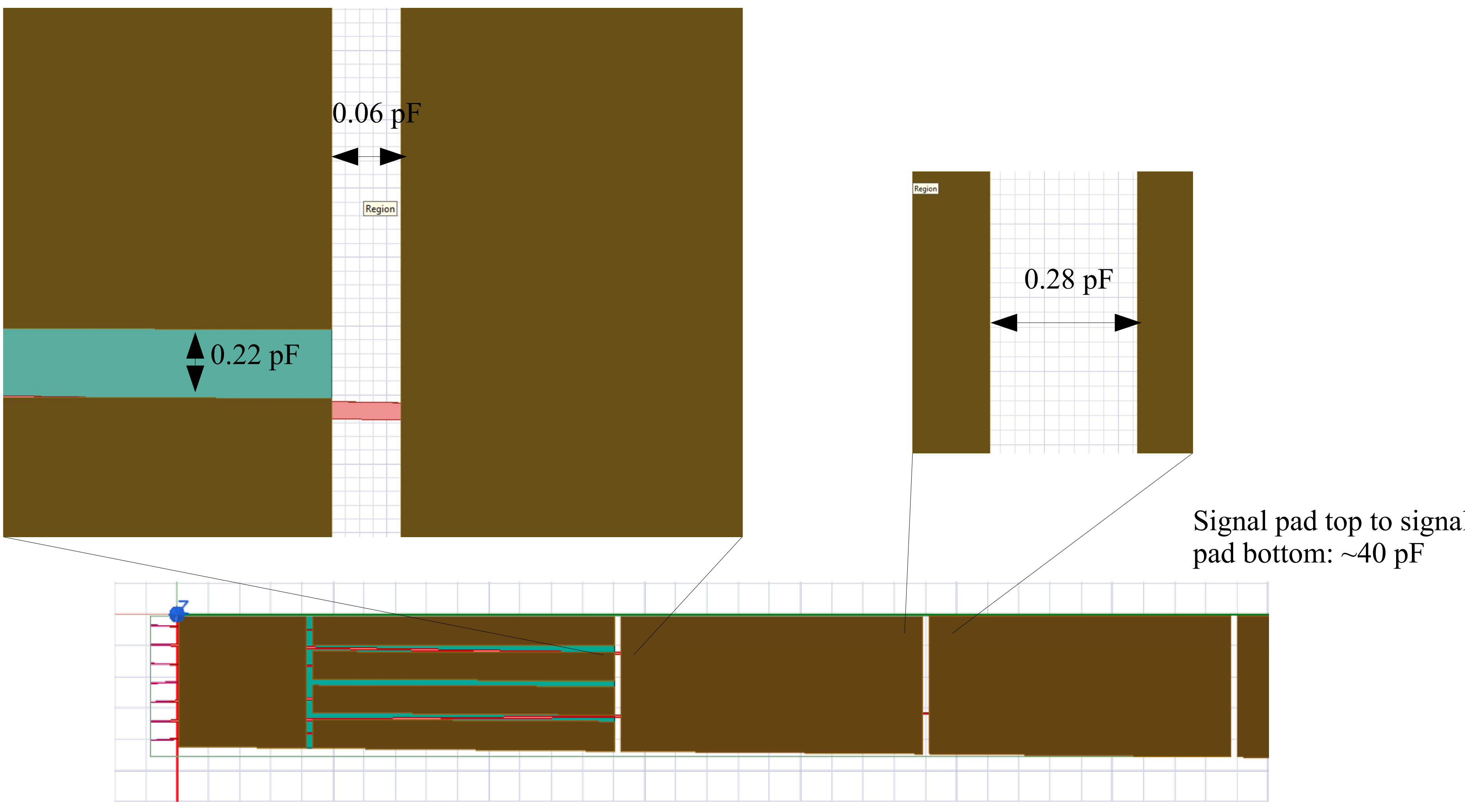
Summary and plans

- Readout electrode capacitance derived from finite-element method simulation (ANSYS Maxwell)
- Derivation of shield capacitance per length and extrapolation to the full detector
- Derivation of capacitance between HV plate and ground absorber (analytical formula)
- Estimation of the noise
- Plans
  - Implement special prescription for the strip layer
  - Port this new noise estimation to FCCSW
  - Investigate signal attenuation
  - Study MIP energy deposit per layer
  - Derive cross talk
    - SIWave is unfortunately not the proper tool in the end, need to use HFSS
  - Find shield width for which cross-talk is 'reasonable'
  - Re-derive capacitance
  - Perform 'final' noise estimation

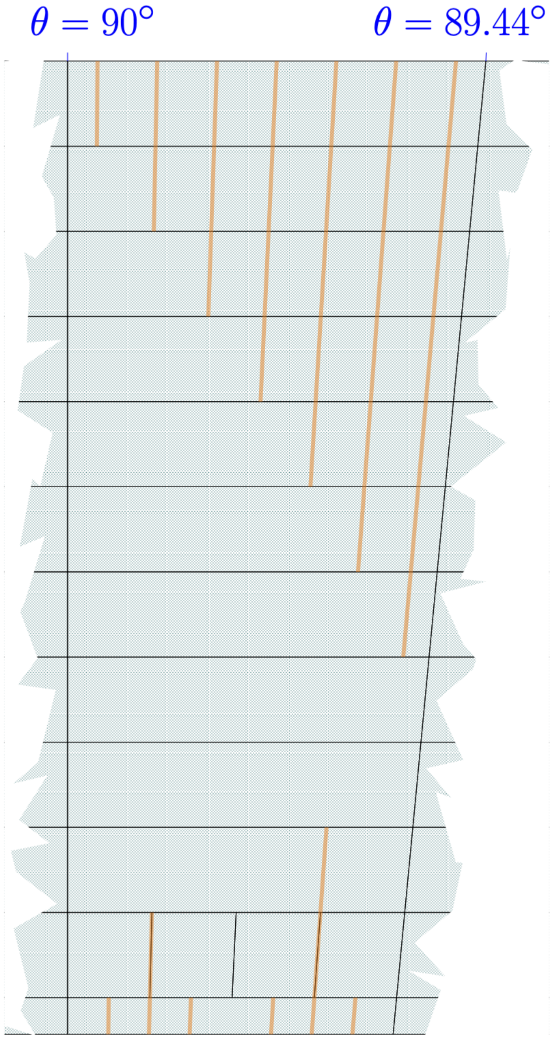
Additional material

Capacitances between signal pads

- 1 mm 'horizontal' spacing between signal pads



Readout electrodes



Readout electrodes