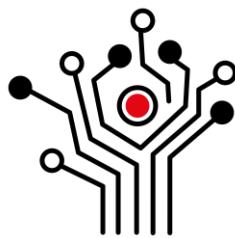


Open-hardware MTCA modules for quantum physics

Grzegorz Kasprowicz



creo TECH
Instruments S.A.



**European
Funds**
Smart Growth



**Republic
of Poland**

European Union
European Regional
Development Fund



Agenda

A quick introduction to ion trap quantum computing;

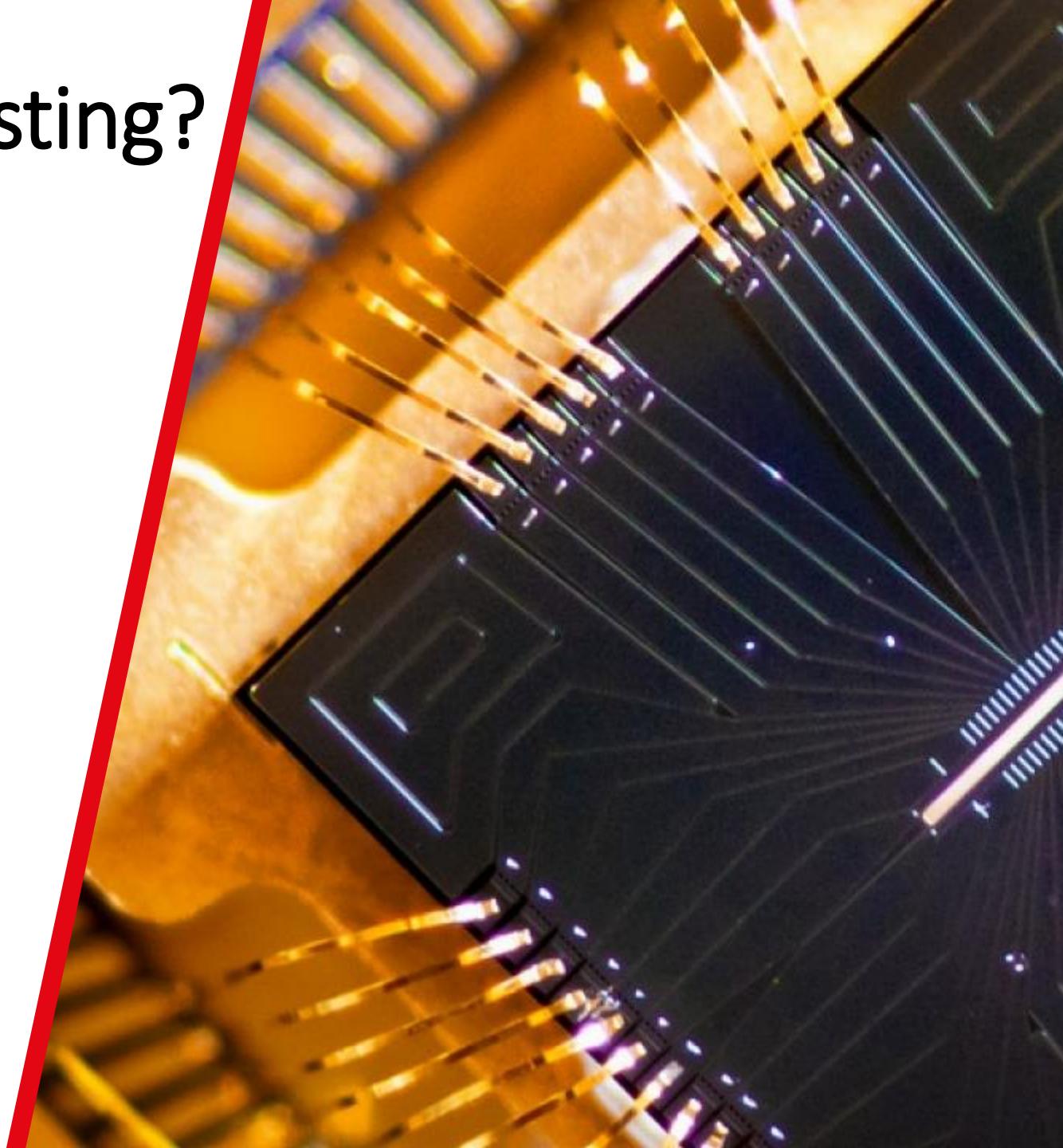
Sinara ecosystem

Presentation of new MTCA-related development

New FMC modules

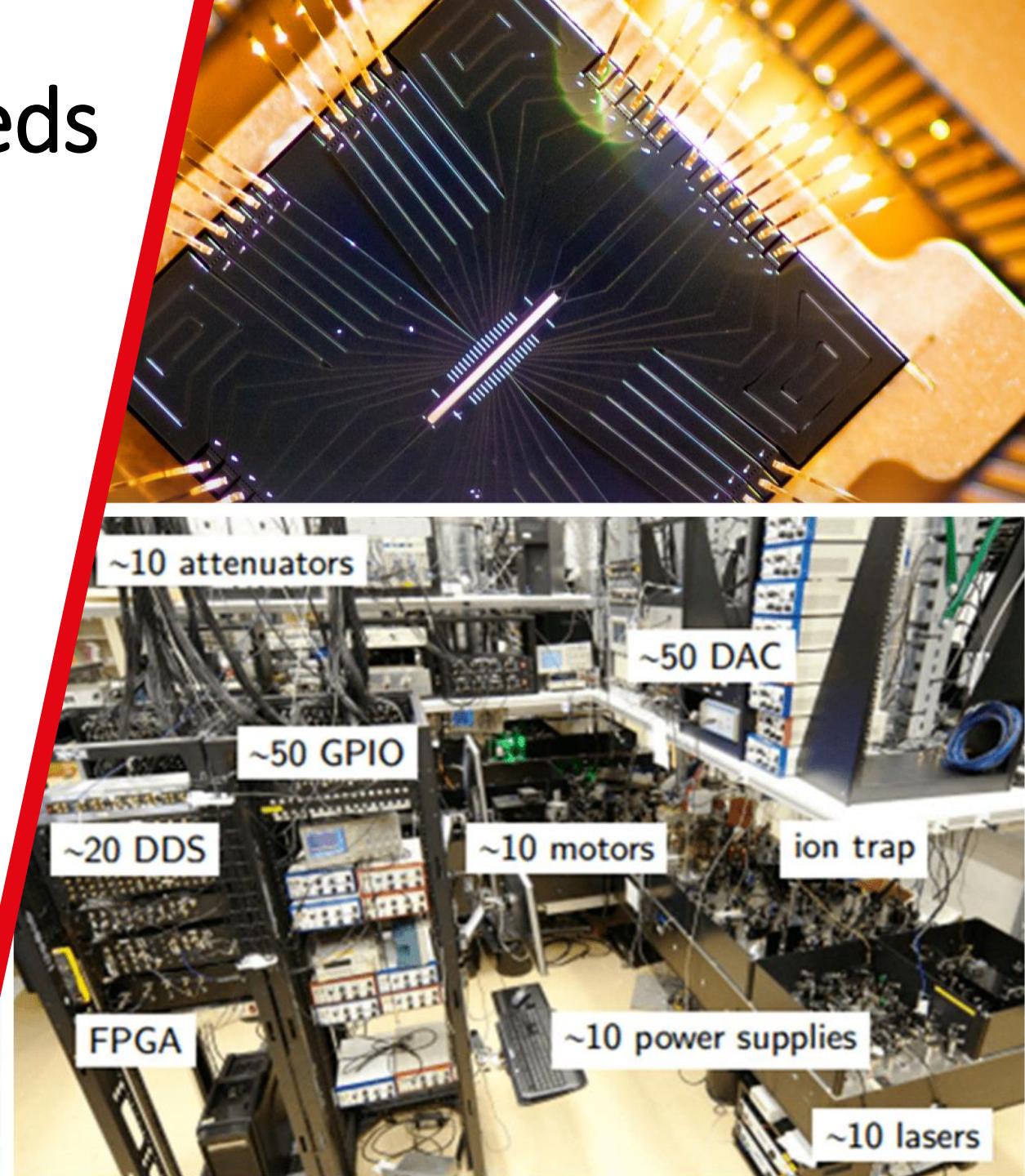
Why are ion traps interesting?

- metrology
- mass spectroscopy
- quantum simulation and sensing
- quantum computing
- qubits are manifested in the internal energy levels of ions and are manipulated through laser and microwave radiation
- long coherence times
- scalability
- e.g. ION Q commercial quantum computer with 11 fully connected qubits, 55 addressable pairs, qubit gate error < 0.03%



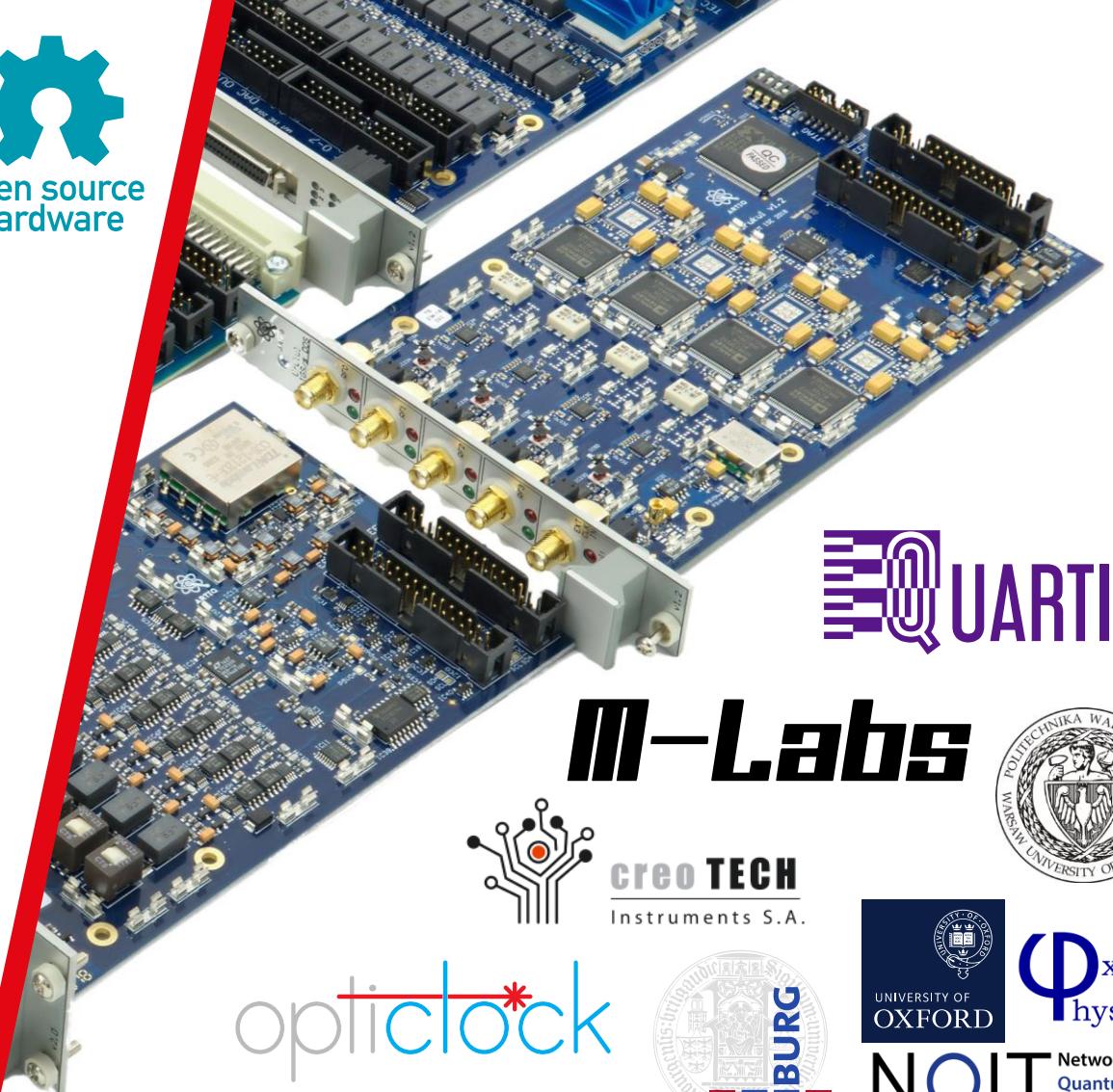
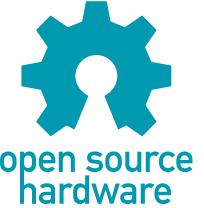
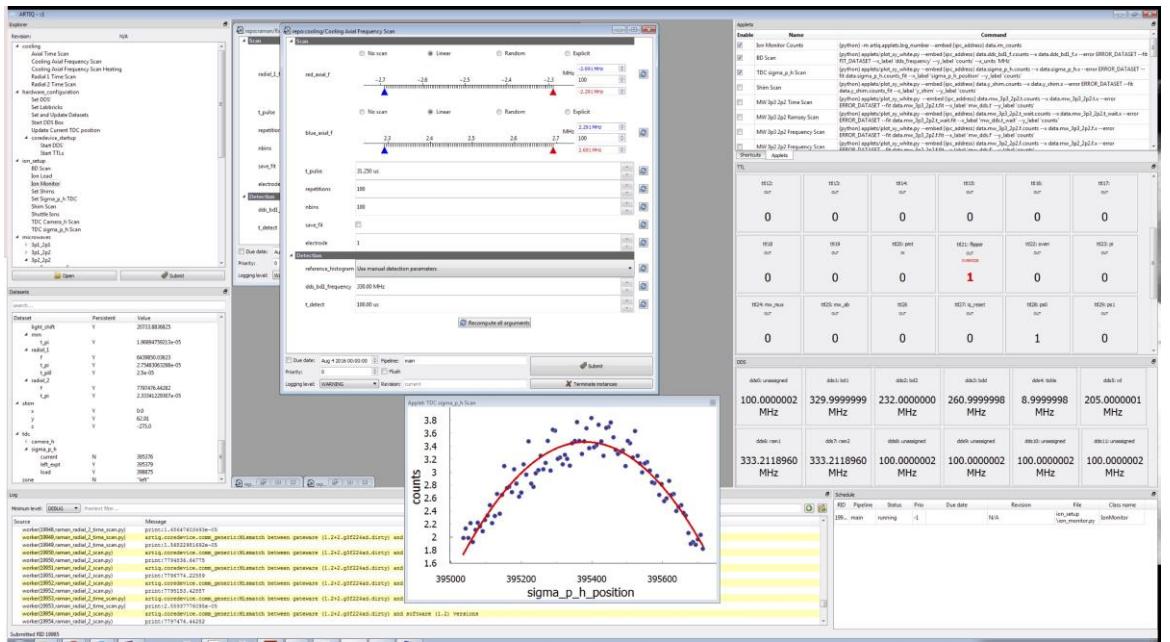
Ion trap experiments - needs

- microsecond response times, sub-ns synchronization
- control system:
 - flexible and modular
 - well tested
 - easy to build and reproduce
- multi-channel processing
- ultra-low noise (order of nV) DAC
- laser intensity servos
- laser frequency stabilization
- fast ion state readout and modification



Sinara project

- Bottom-up initiative of the ion trap community
- Modular control and measurement hardware ecosystem, tailored to the needs of ion-trap experiments
- Open source HW
- Compatibility with ARTIQ open software



QUARTIQ

M-Labs



creo TECH
Instruments S.A.



Oxford
Physics

UNI
FREIBURG

UNIVERSITY OF
MARYLAND

JOINT
QUANTUM
INSTITUTE

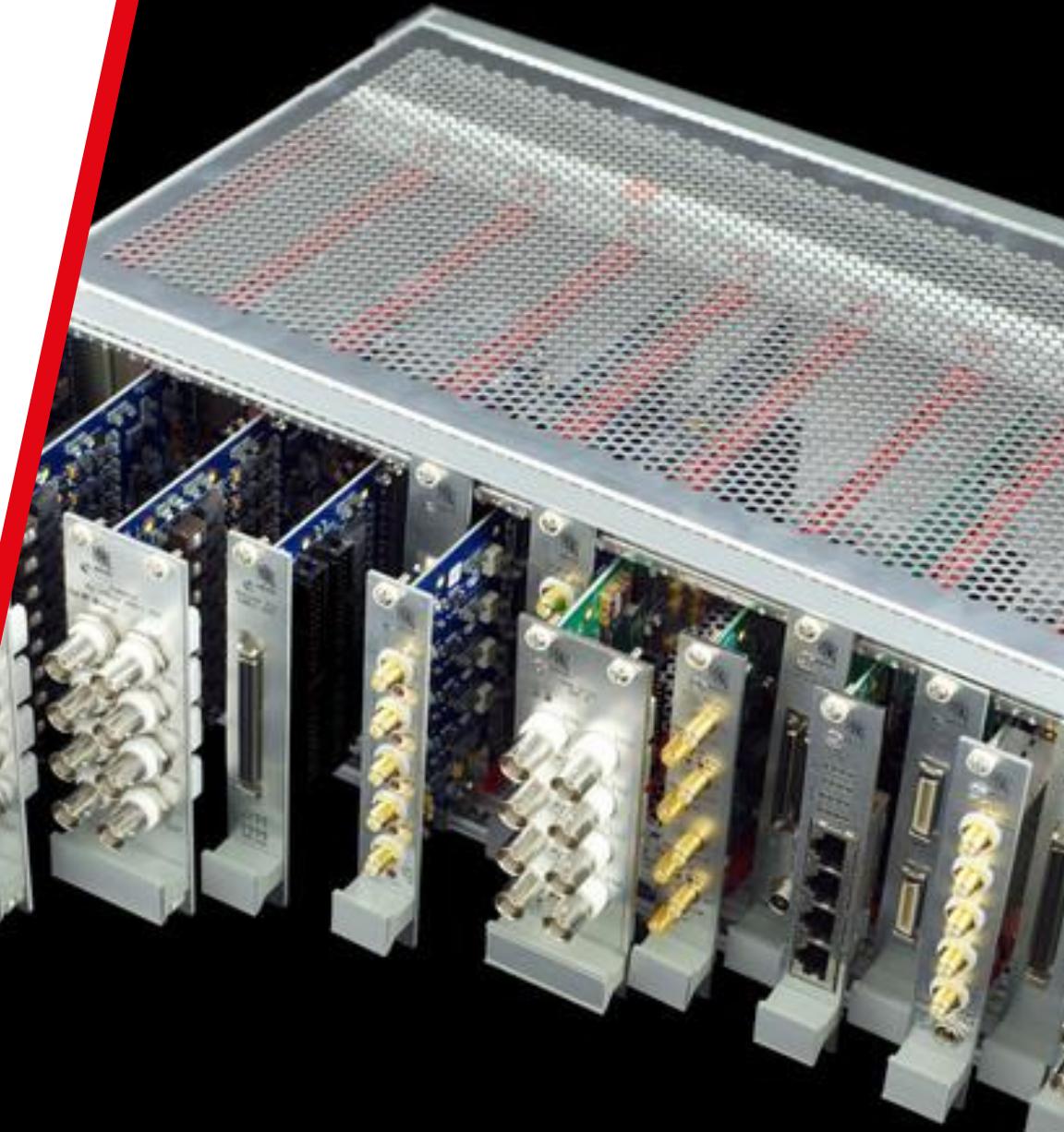
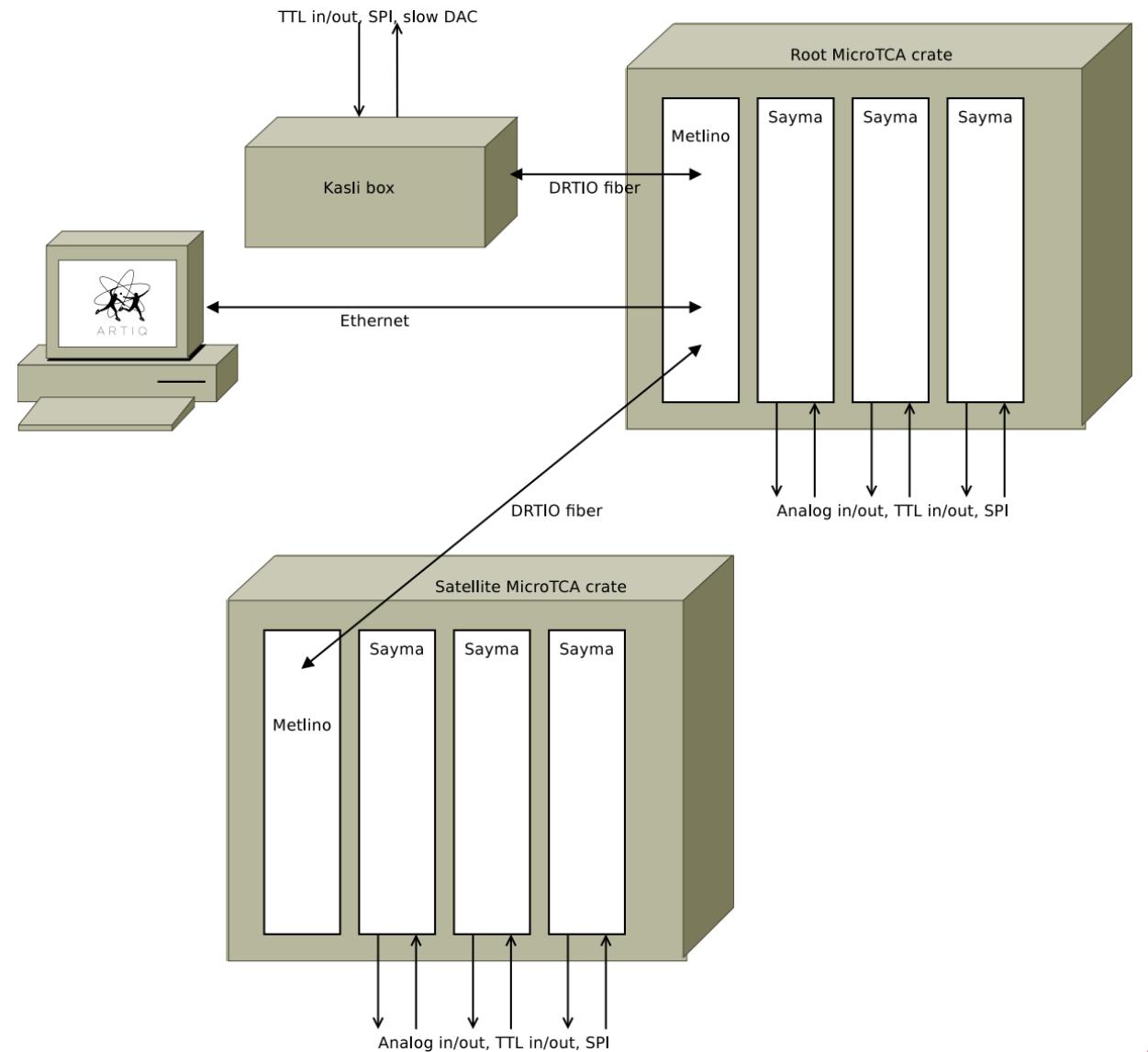
PTB
Physikalisch-Technische Bundesanstalt
Braunschweig und Berlin

Leibniz
Universität
Hannover

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Sinara control system



- **Kasli** Artix-7 100T FPGA deterministic real time controller (sub-ns precision)

- TTL or LVDS **I/O** EEMs

- **Urukul** DDS-based frequency synthesizer with sub-Hz resolution, phase steps and amplitude control

- **Sampler** low-noise ADC with 1.5MSPS sample rate and +10mV to +10V input range

- **Zotino** DAC with ultra-low noise and good stability

- **Grabber** camera interface

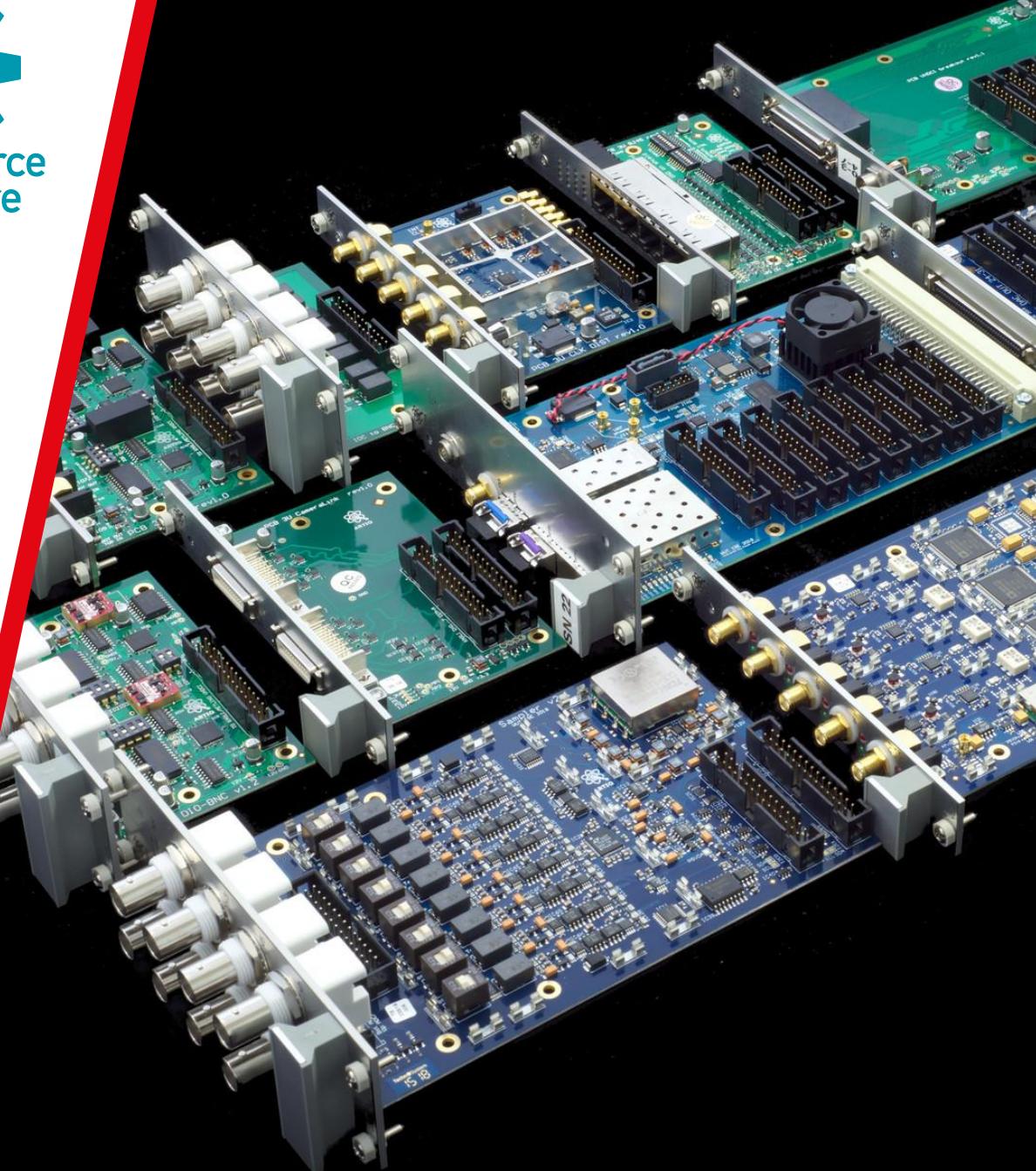
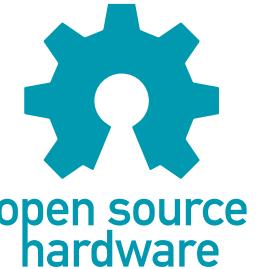
- **Clocker** clock distribution with low jitter <100fs

- **Thermostat** temperature controller

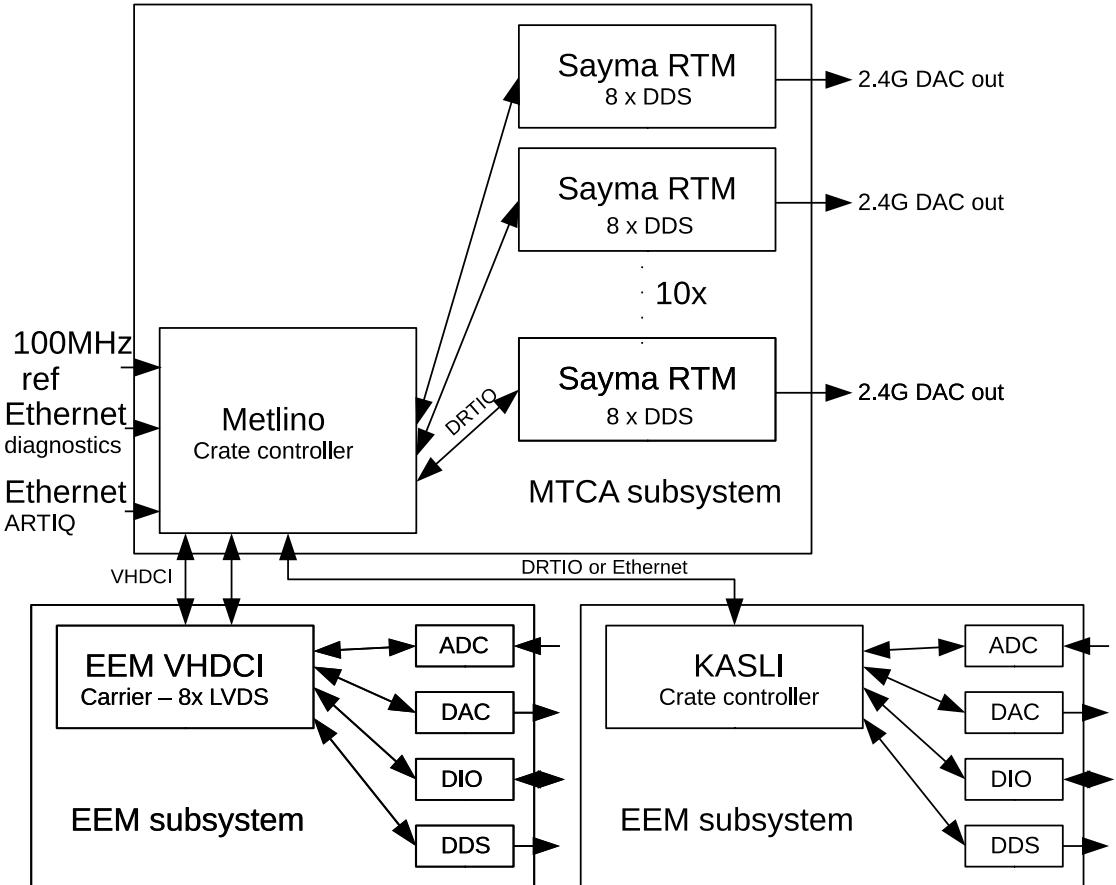
- **Booster** 8 channel RF amplifier for AOM

- **Sayma** AMC and RTM SAWG in MTCA format

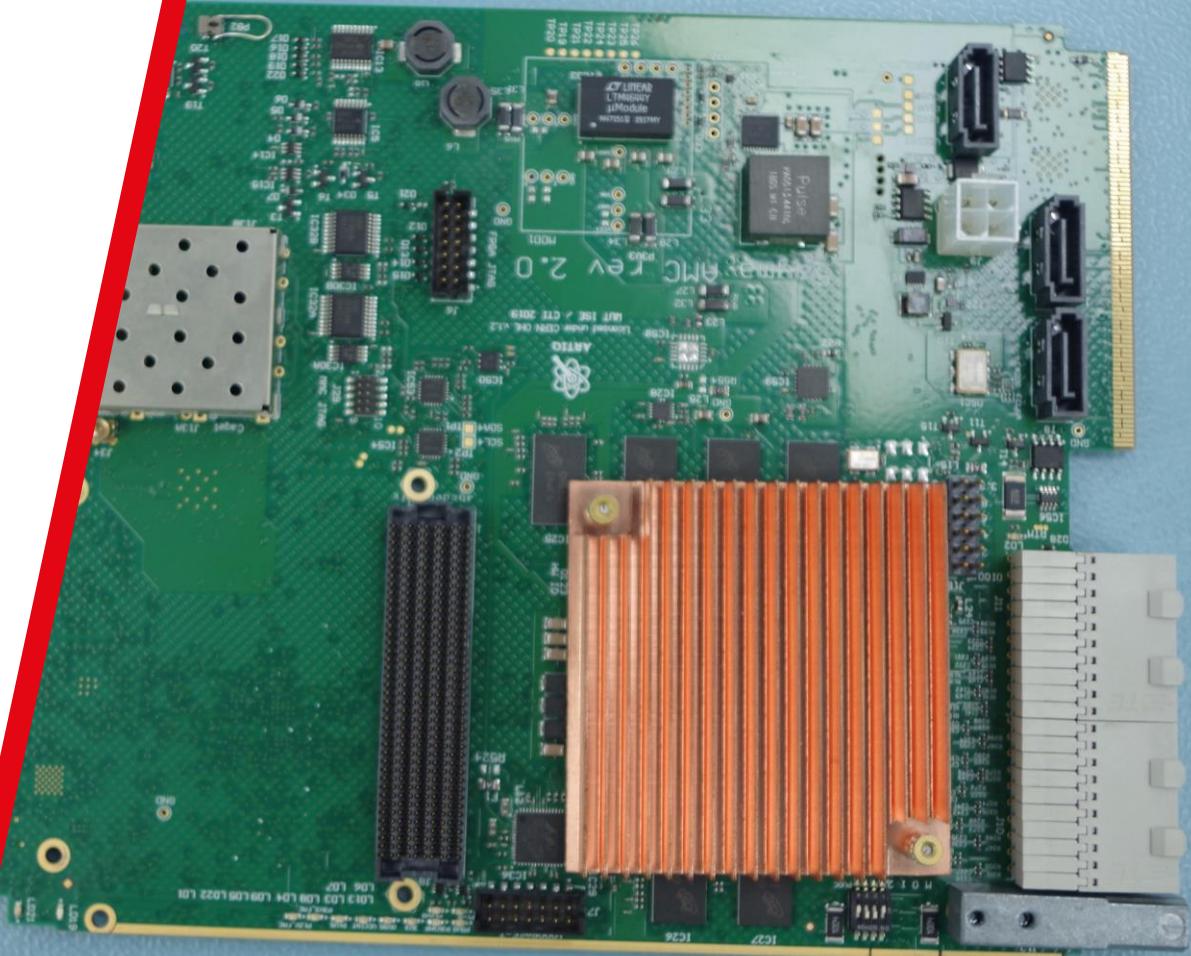
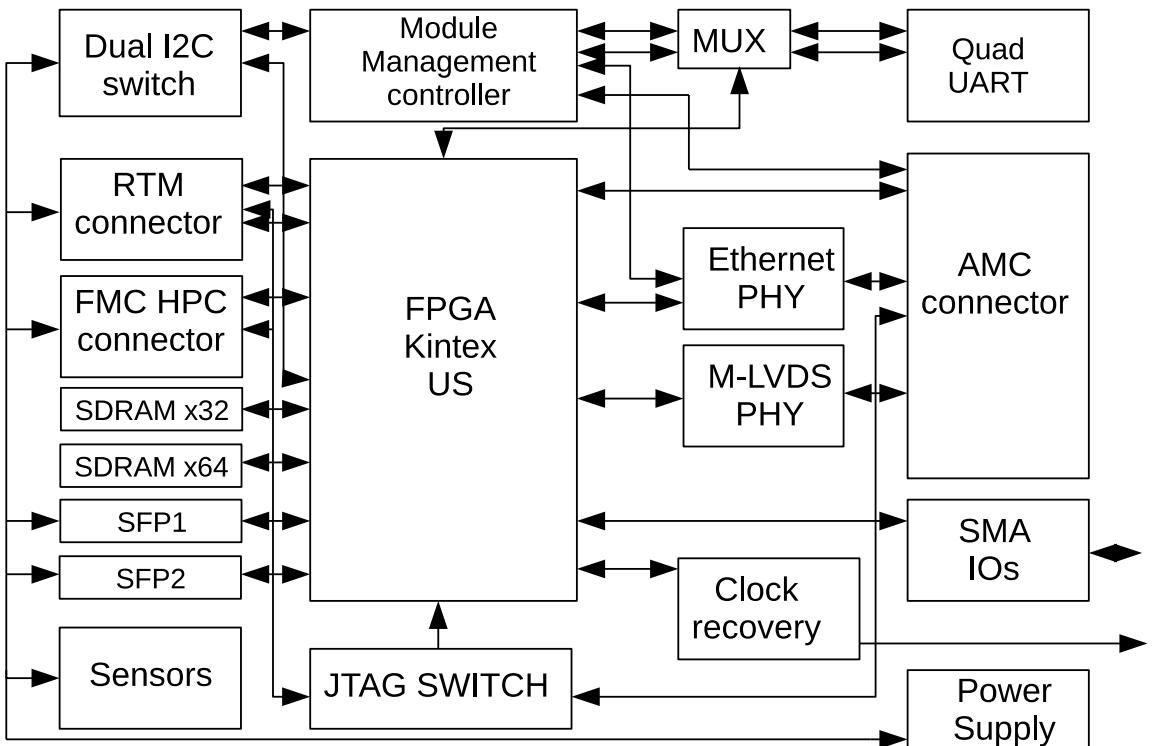
- **56** modules and growing...



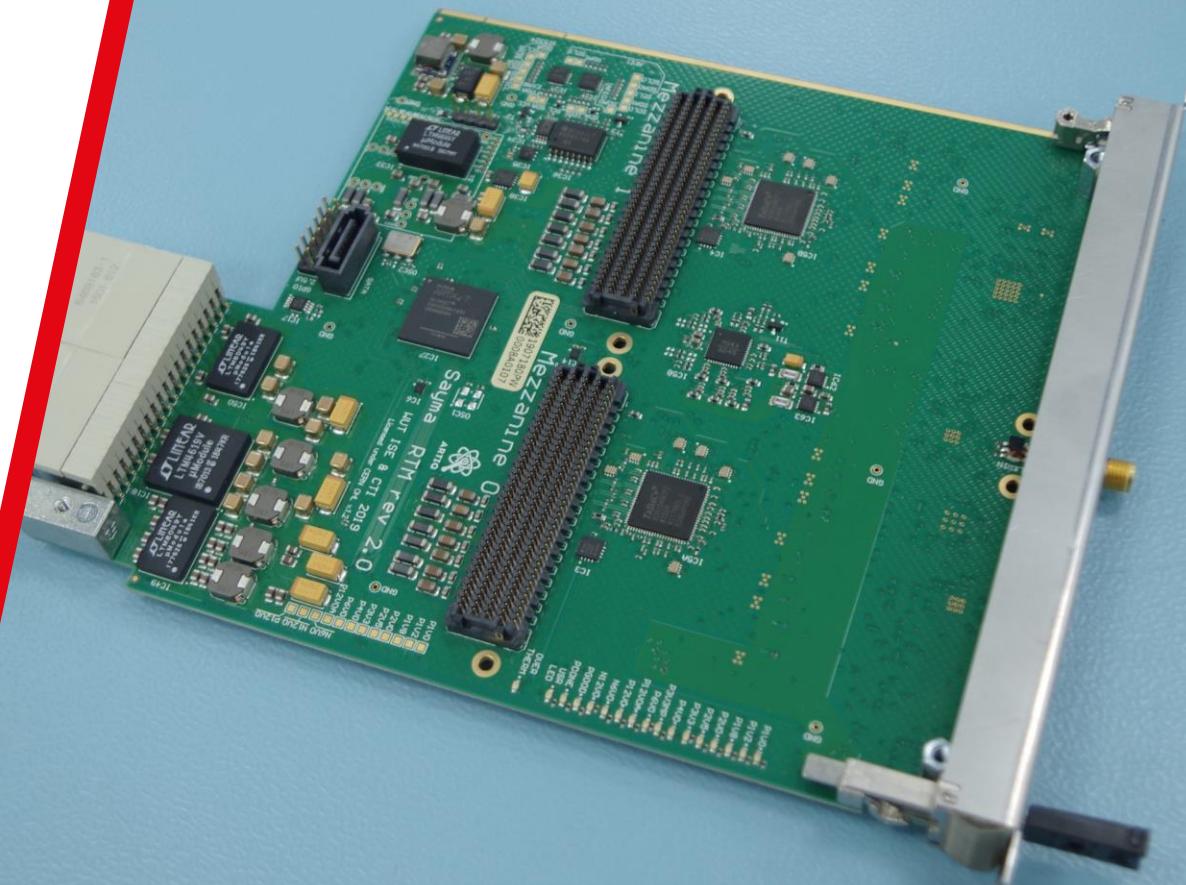
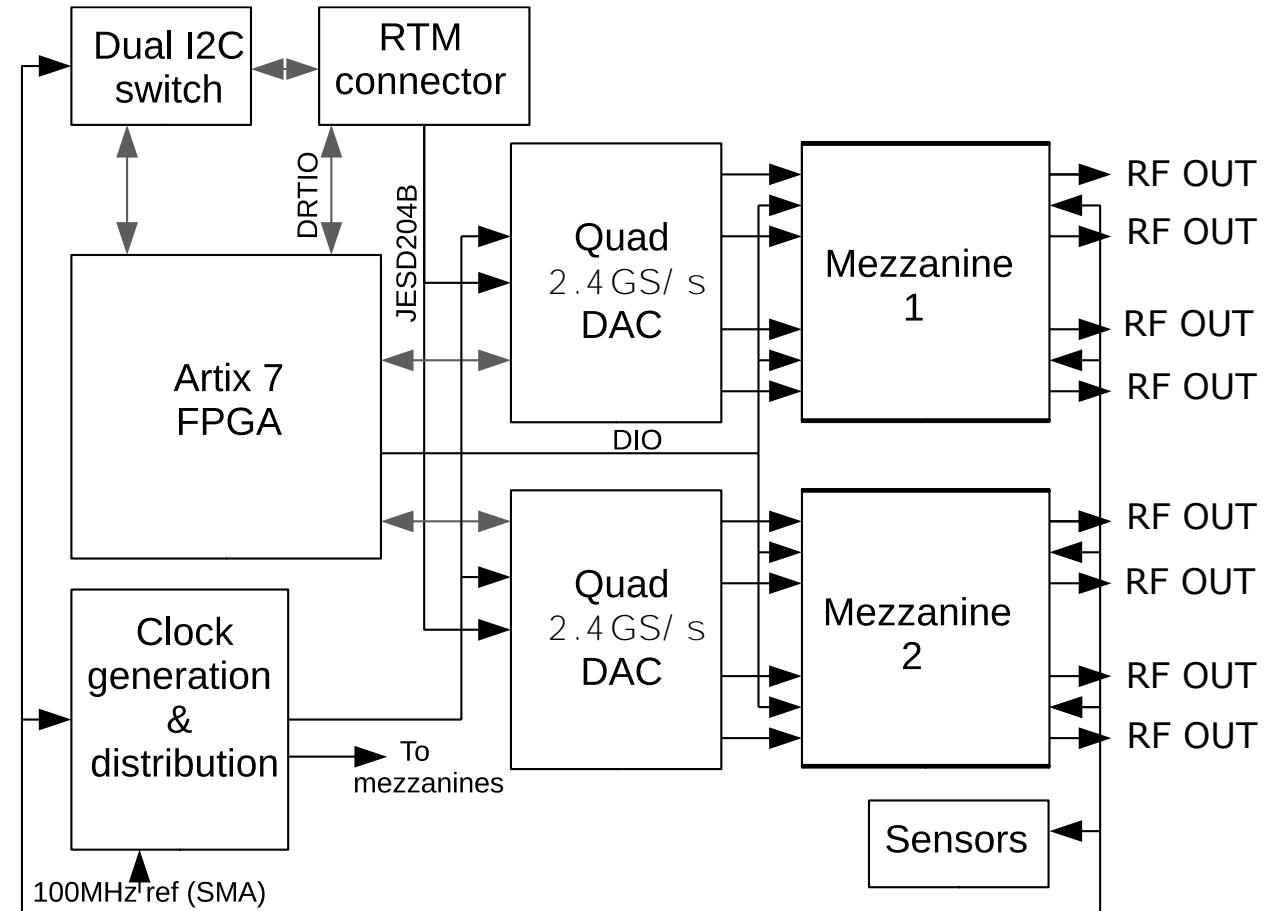
Sinara Ecosystem



Sayma AMC – AWG controller



Sayma RTM – 8 CH 2.4GS/s AWG



Metlino

Sits on top of standard NAT MCH

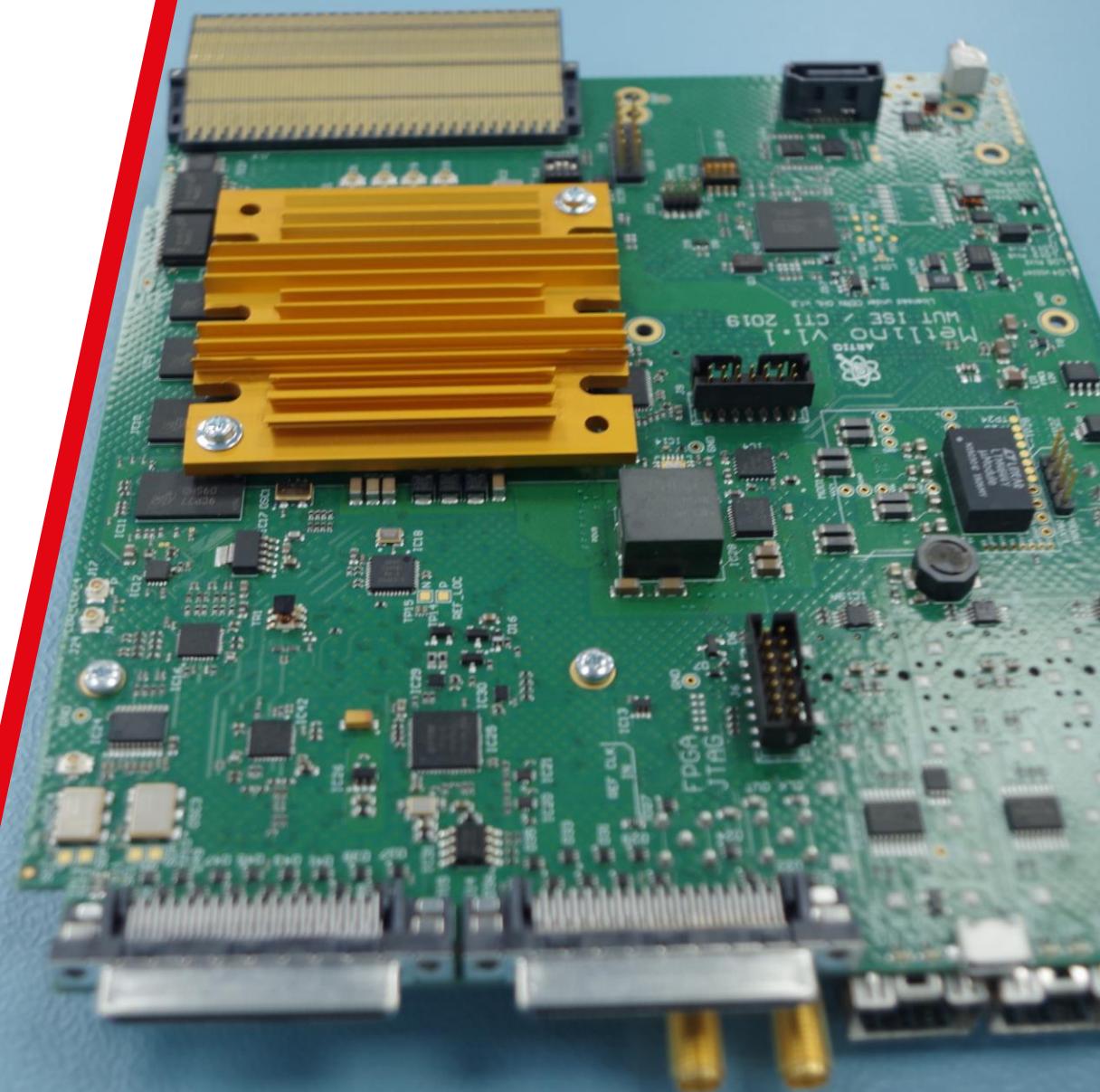
Based on UltraScale FPGA

DRTIO master/slave

Controls:

- other MTCA crates using DRTIO
- EEM boards using LVDS links

FMC connector for future extensions



RF-SoC

8 channel complete readout system for
SC qubits / AWG

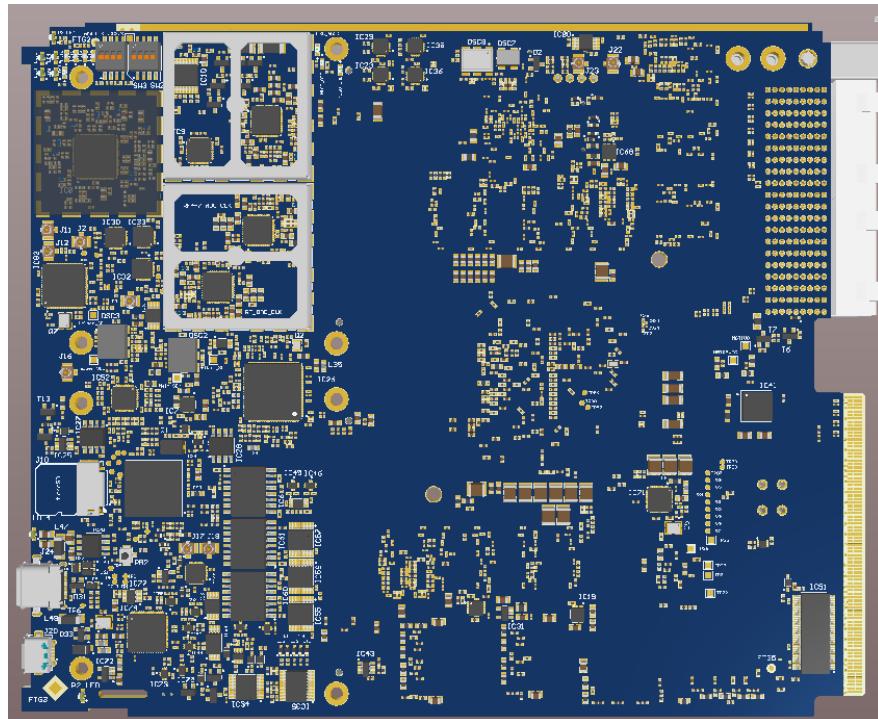
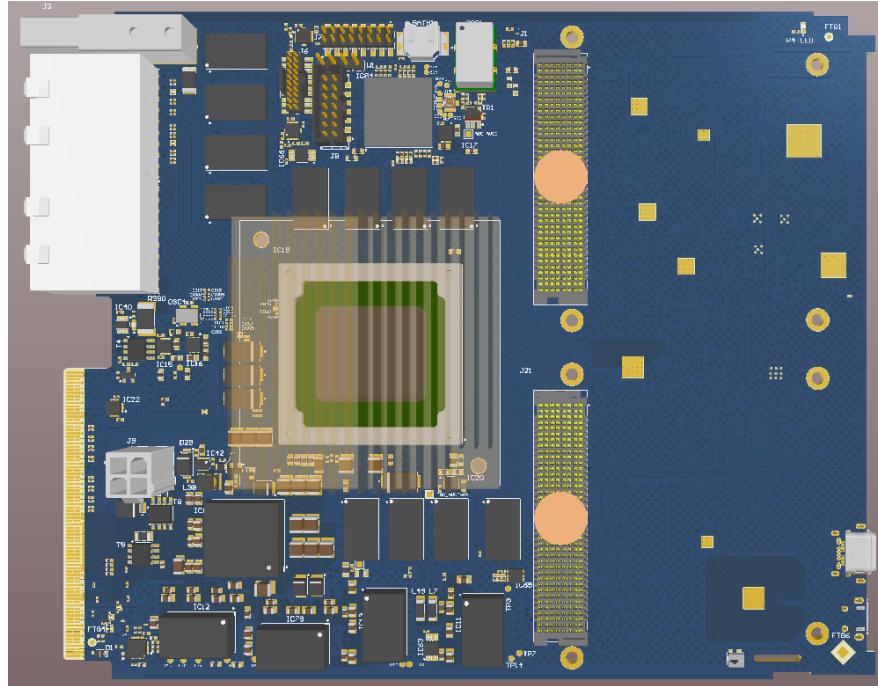
Universal AFE modules for various
physics (ion-traps, SC qubits)

Based on RFSOC

Dedicated timing FPGA

Current status: 2-nd PCB review

Developed at the WUT & Technosystem
within NCBIR project



AMC FMC CARRIER - AFC

New revision of well known AFC

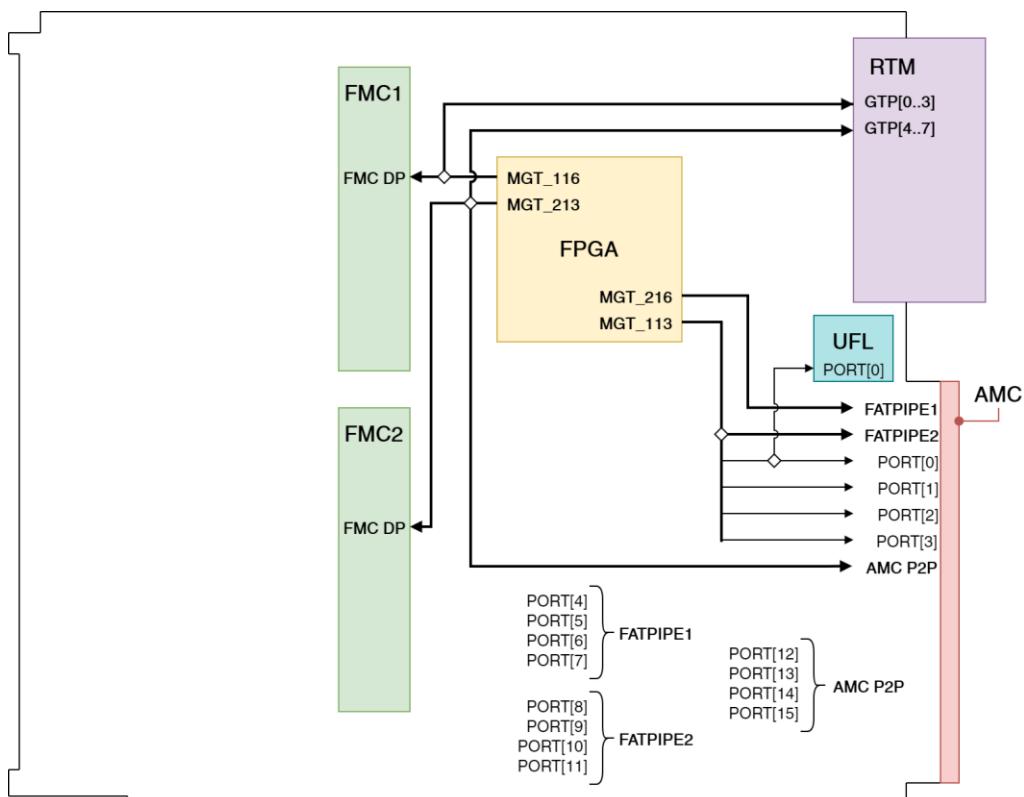
Multi channel TDC and readout system for QC

Flexible clock circuit (WR, DRTIO support)

Common development between LNLS, WUT

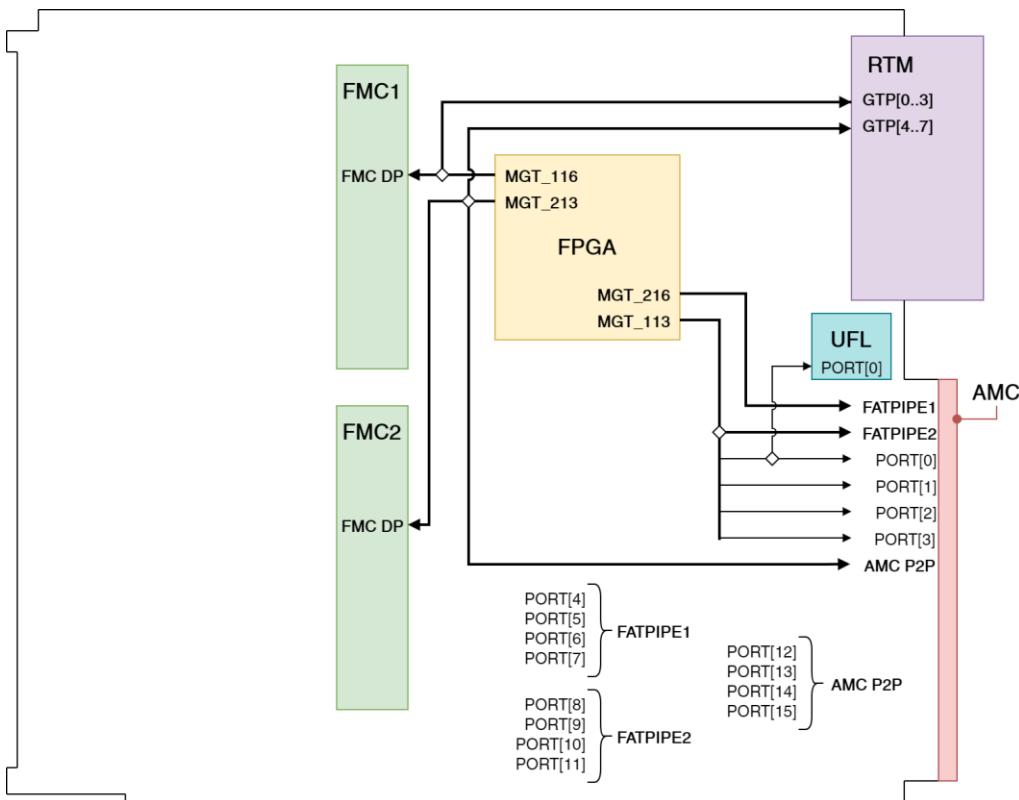
and CTI

Optional RTM SFP-QSFP



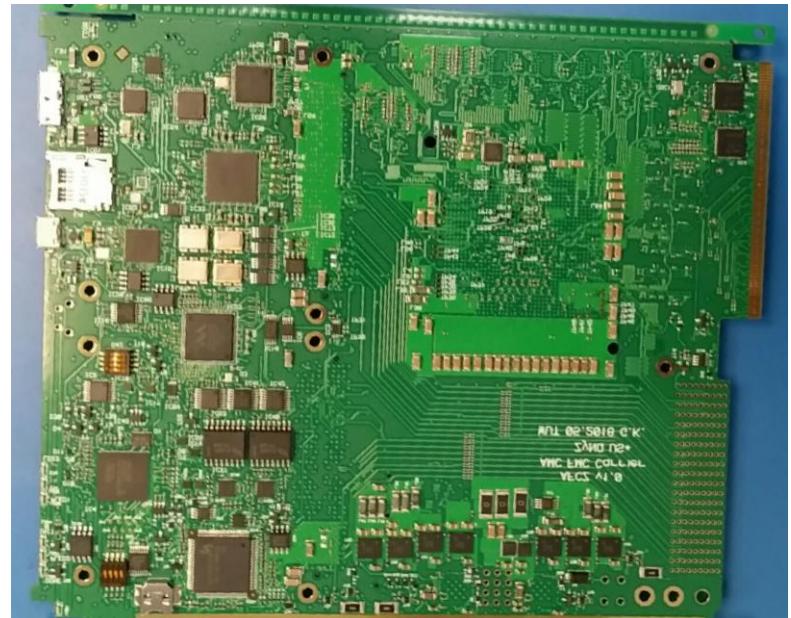
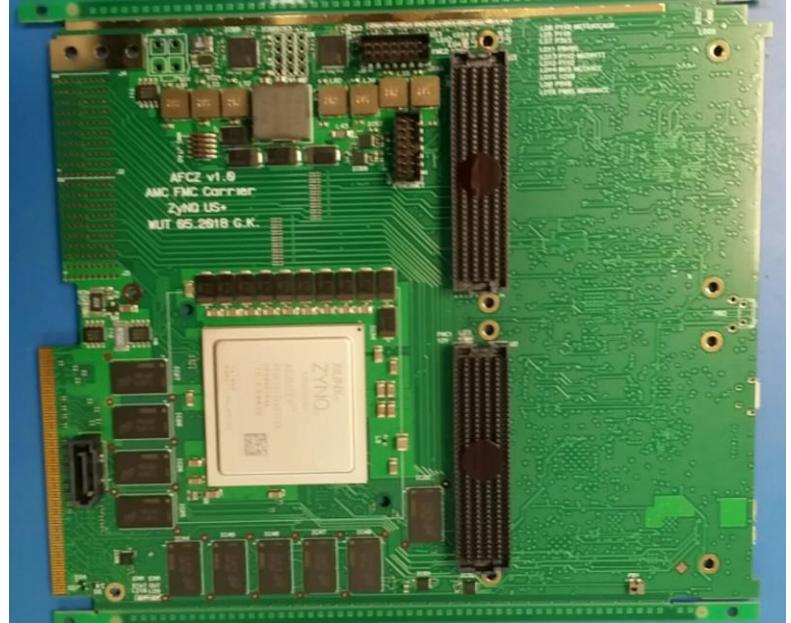
AMC FMC CARRIER – AFCK v2

New revision of well known AFCK – based on UltraScale
FPGA; architecture unified with AFC
Multi channel TDC and readout system for QC
Flexible clock circuit (WR, DRTIO support)
Common development between LNLS, WUT and CTI
Optional RTM SFP-QSFP



AFCZ

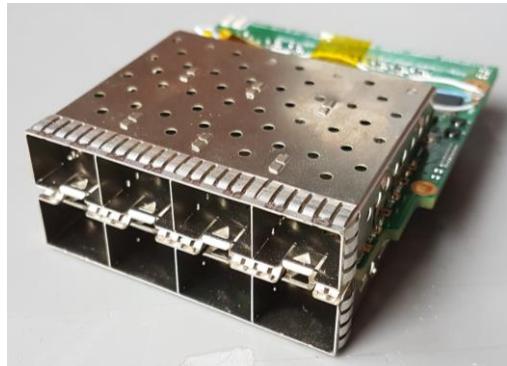
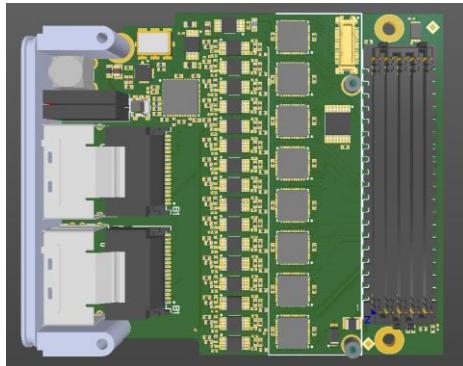
AMC FMC Carrier with ZynQ US+
Optional RTM SFP-QSFP
Optimized for high speed serial converters
2-nd revision developed together with
CERN for LLRF / WR applications; currently
tested at CERN



New FMC modules

Several FMC modules were developed to complement the carrier boards:

- 16-channel ADC + CFD + TDC
- 16 channel 125MS/s, 14-bit DAC for ion shuttling + dedicated AFE
- SFP FMC with 4 or 8 cages



- **48 channel 2.4GS/s AWG**
 - Dedicated to ion-trap applications
 - AFE boards with RF gain control and precise ADC
 - All channels synced within a fraction of ns using DRTIO
 - Developed for US Army Research Lab/Oxford by WUT, CTI and Mlabs
-
- Ongoing integration effort of Sinara ecosystem and CERN Distributed IO Tier – CPCIS backplane instead of ribbon cables
 - Sinara is used in over 100 Q experiments around the world, over 2k units sold
 - Sinara is currently applied to control CERN AEgIS experiment (anti-matter trap)

