

The OpenIPMC project

Development of a portable FOSS IPMC software and design of an HW platform for its operation

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16th CERN xTCA Interest Group Meeting

Elements of the project and their aim

- IPMC software (OpenIPMC)
 - Open Source SW → No license problems (e.g. students), flexibility
 - Multiplatform → Freedom to choose MCU, future-proofing (arch.)
 - PICMG-compliant → Compatibility (so far restricted to the HEP use case)
 - See our presentation in 15th xTCA IG (<https://indico.cern.ch/event/897461/>)
- IPMC DIMM hardware module (OpenIPMC-HW)
 - Open Source HW → Future-proofing (any group can re-use the design)
 - LAPP pinning → Compatible with CERN IPMC layout v4
 - Rather simple PCB → Can be fabricated by many PBC manufacturers
 - Well-supported MCU
- Firmware for the DIMM module (OpenIPMC-FW)
 - Open Source SW → No license problems (e.g. students), flexibility
 - Eclipse-based SDK → Popular, easy to use and install, supports Linux
 - Support for different ATCA boards

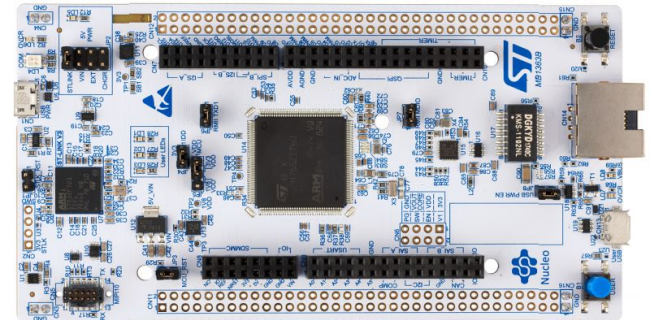
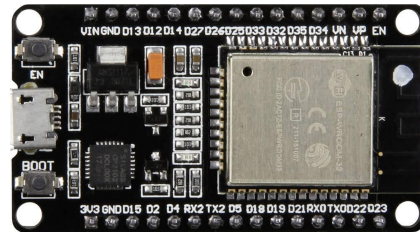
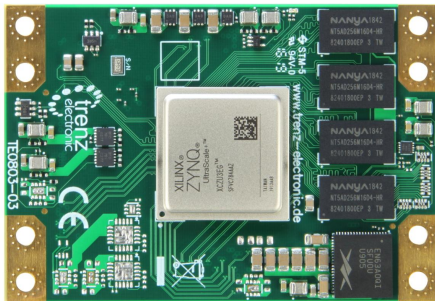
Brief recap on the OpenIPMC software

OpenIPMC

- IPMC software implementing PICMG-compliant IPMI functions
 - Power negotiation and hot-swap (M-states, handle, etc.)
 - Instantiate board sensor records, declare them to ShM, read-out and publish data
 - Focus on simplicity: optional functions can be added to the project by the user
- Platform-independent design, written in C
 - Can quickly port the project to different architectures (e.g. ZynqMP, ESP32, STM32)
- Based on FreeRTOS operating system
 - Can run independent “tasks” in parallel (w/ prioritization)
 - Flexible software development, thanks to task decoupling
 - Supported by many SoC manufacturers (TI, NXP, ST, Xilinx, Microsemi...)
- OpenIPMC is free and open source software
 - Can be easily customized to fit a new board, and modified to be debugged
 - No need to sign NDAs for contributors, curious newcomers and students

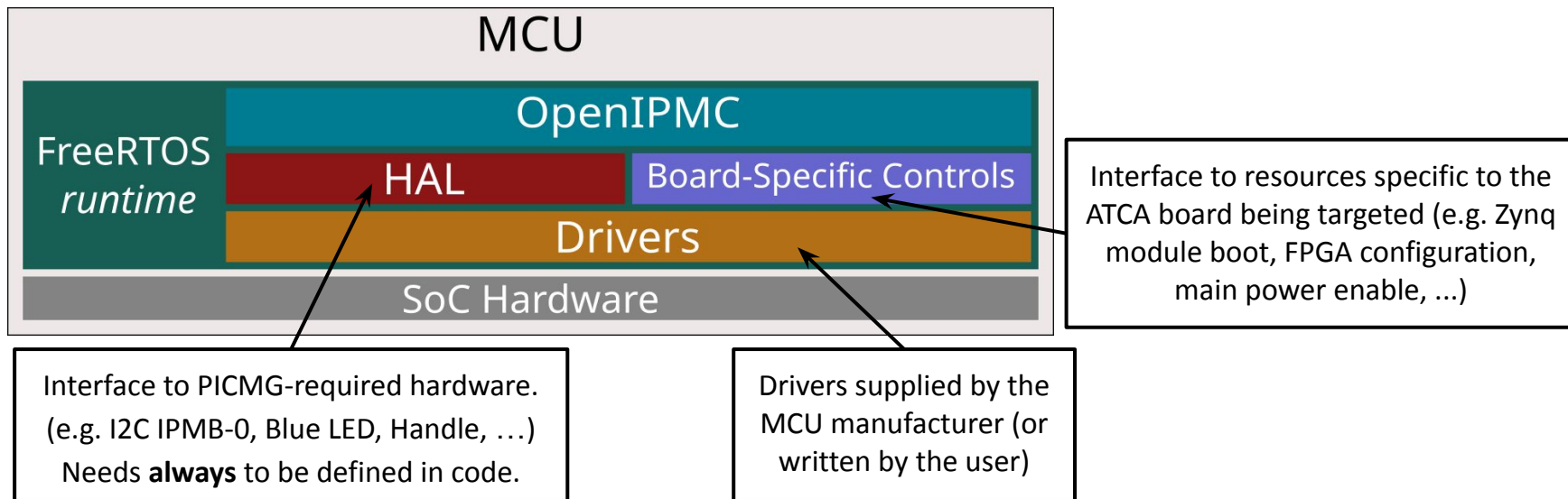
Evolution of OpenIPMC support on different devices

- First platform: Cortex-R5 cores on Zynq US+
 - IPMC (R5) and Linux (A53) running in the same device
 - Targeting the ATCA-ZynqMP management module by KIT (proposed for Serenity-A2577)
- Portability exercise: ESP32 microcontroller
 - Not a “serious” device, but very different arch from Zynq, cheap and very flexible
- First mainstream MCU: STM32 microcontroller
 - Successful porting opened the way to design of the DIMM module



How OpenIPMC interfaces to the hardware

- Two interfaces between OpenIPMC hardware-agnostic code and hardware drivers
 - **Hardware Abstraction Layer** → interface to hardware driver used for IPMI functions (IPMB, blue led..)
 - **Board-specific controls** → customize board-specific behavior (how to turn on power, read sensors..)
- Note that other FreeRTOS tasks (not shown in pic) can run aside of the OpenIPMC stack



OpenIPMC-HW

Choice of the microcontroller

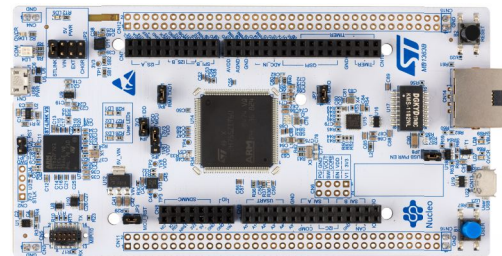
The OpenIPMC software runs on top of FreeRTOS

- Software shown to be easily portable on new MCUs (~3 wks)
- Plenty of MCU manufacturers to choose from



We chose **STM32H745XIH6** by STMicroelectronics

- Number of I2C/SPI hardware peripherals → 4 / 6
- Number of GPIOs/UART/USART → up to 168 / 4 / 4
- Availability of a free toolchain → STM32CubeIDE
- Availability of an evaluation board → NUCLEO-H745ZI-Q (cost: 23 CHF)
- Our experience with other STM32 MCUs → STM32F103C8T6 (e.g. “Blue pill” board)
- Performance margin for future upgrades → 480 MHz Cortex-M7+240 MHz Cortex-M4
- Large SRAM/Flash memories → 1024 kiB / 2048 kiB
- Expected reliability of the manufacturer → STMicroelectronics is a leader in MCUs
- Cost → 17.45 \$ per piece



STM32 NUCLEO-H745ZI-Q

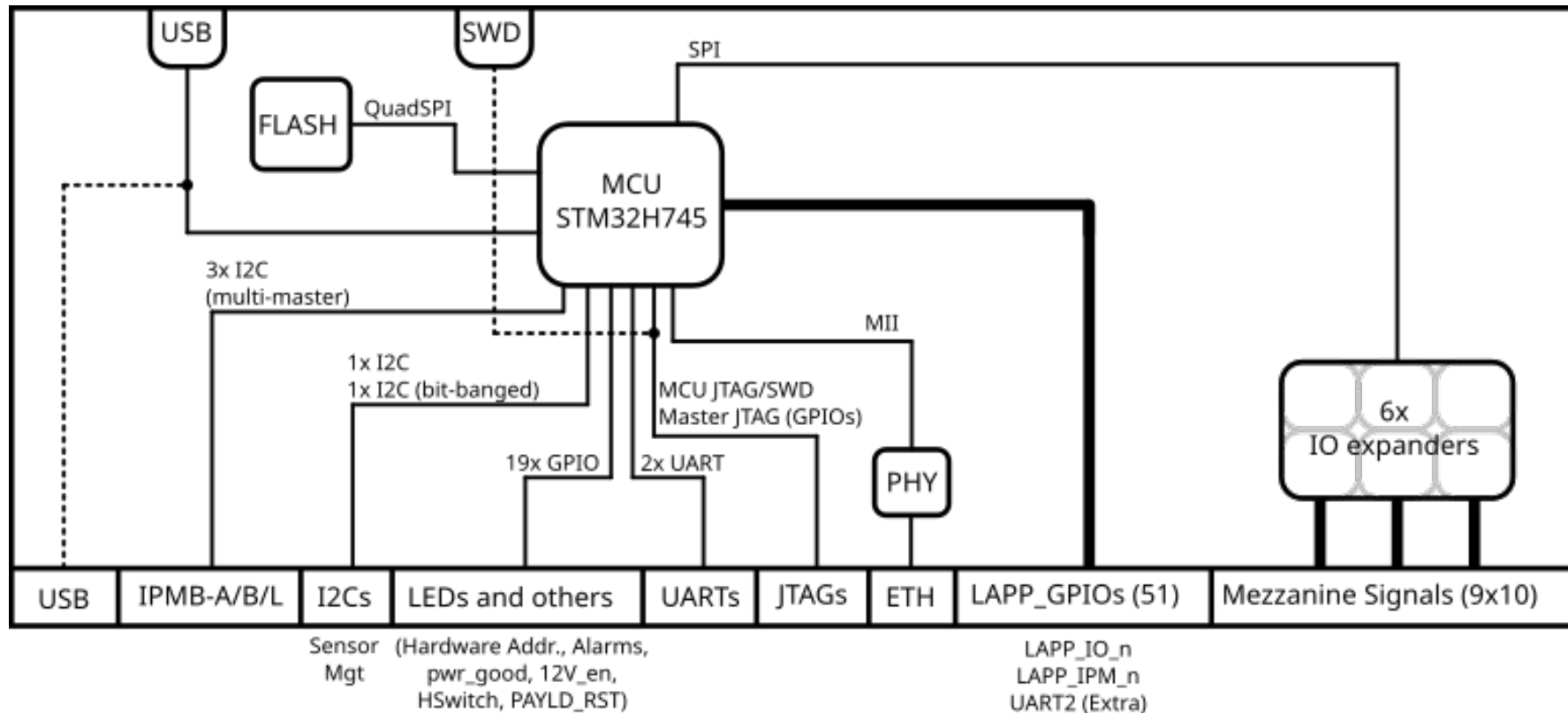
What we get in addition

- High speed USB device/host/OTG → USB programming & terminal
- Efficient SMPS to power the core → better thermals
- External memory support → store config/firmwares/etc
- Lots of other features we will not use (e.g. HDMI driver)

Full documentation on ST site

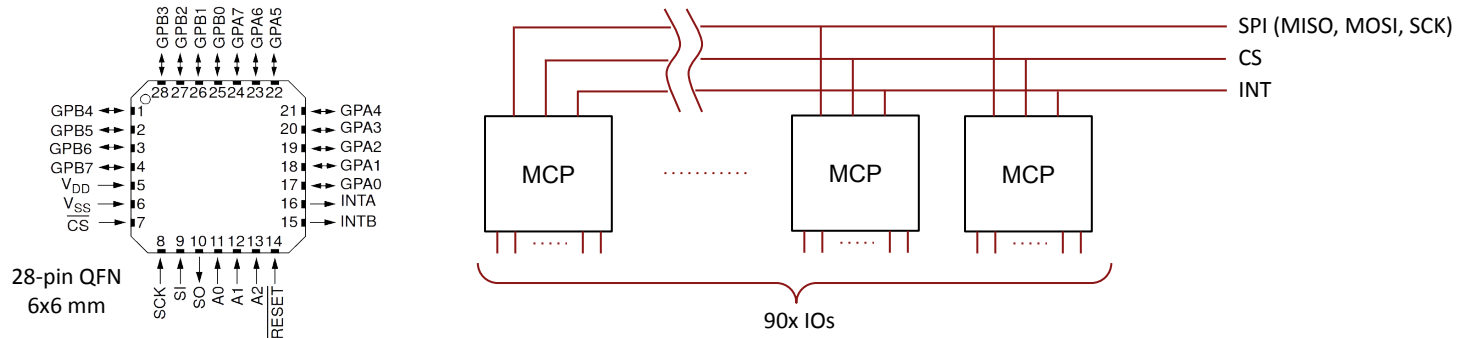
<https://www.st.com/en/microcontrollers-microprocessors/stm32h745-755.html#documentation>

OpenIPMC-HW layout: schematic



AMC IO expanders

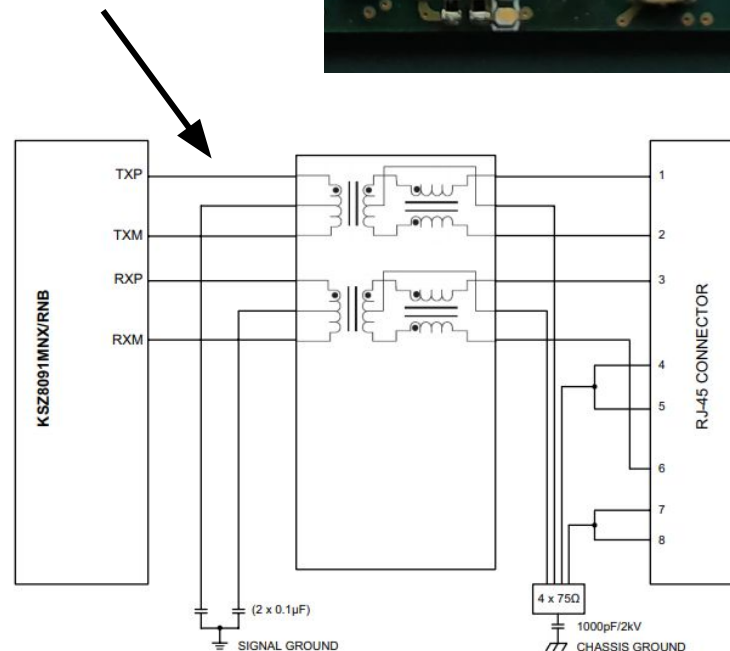
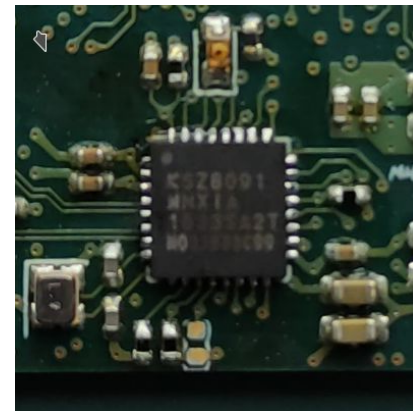
- CERN/LAPP IPMC specifies a set of 10 control signals for each AMC mezzanine
 - Up to 9 mezzanines are supported → **90 GPIOs needed!!!**
- We use six Microchip MCP23S17 16-bit I/O expanders, controlled via a single SPI bus at 10 MHz
 - Only one SPI bus + shared Chip Select (CS) to control all the expanders
 - Expander address in SPI protocol header, address is set via package pull-ups /downs
 - One GPIO from MCU used to catch the interrupt signals from the expanders (open collector mode)
- Dedicated driver was developed to control all Expanders in a transparent way



Ethernet PHY

- Micrel/Microchip KSZ8091MNX

- Same as other IPMCs
 - Compatibility with **tx/rx bias scheme** used in existing in ATCA boards
 - Well tested PHY, known to be reliable
- 10/100 Mbit with auto MDI/MDI-X
- MII interface @ 25 MHz
 - Separate 25 MHz crystal for the PHY on the IPMC
- MDC/MDIO for configuration
- Other features we don't use
 - TDR for fault detection & ranging, ...



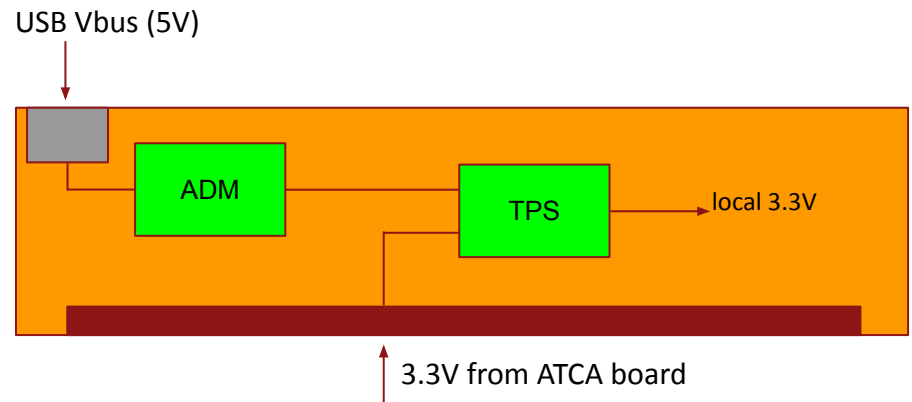
USB interface

- Intended for use in two functions
 - Quick access to the IPMC Command Line Interface
 - Firmware update via a simple USB cable
- Command Line Interface via USB VCP driver
 - VCP is part of the USB standard
 - Supported natively by ST development tools
- Hardware update via USB DFU protocol
 - DFU is part of the USB standard
 - Supported natively by the ROM bootloader in the MCU



3.3V power OR-ing switch

- We want to make possible to program the module in-hand via USB
 - Two Possible Power Sources and risk of reverse powering
- Source hierarchy
 - DIMM Edge connector (3.3V) → primary source
 - On-board USB (5V) + 3.3V LDO → secondary source
 - Source conflict resolution → use a COTS ORing switch for USB applications
- Texas Instruments TPS2115A
 - Automatic power ORing with 2 inputs
 - 3x3mm SON-8 package
- Analog Devices ADM7172
 - 3.3V LDO, max 2A
 - 8-LFCSP package

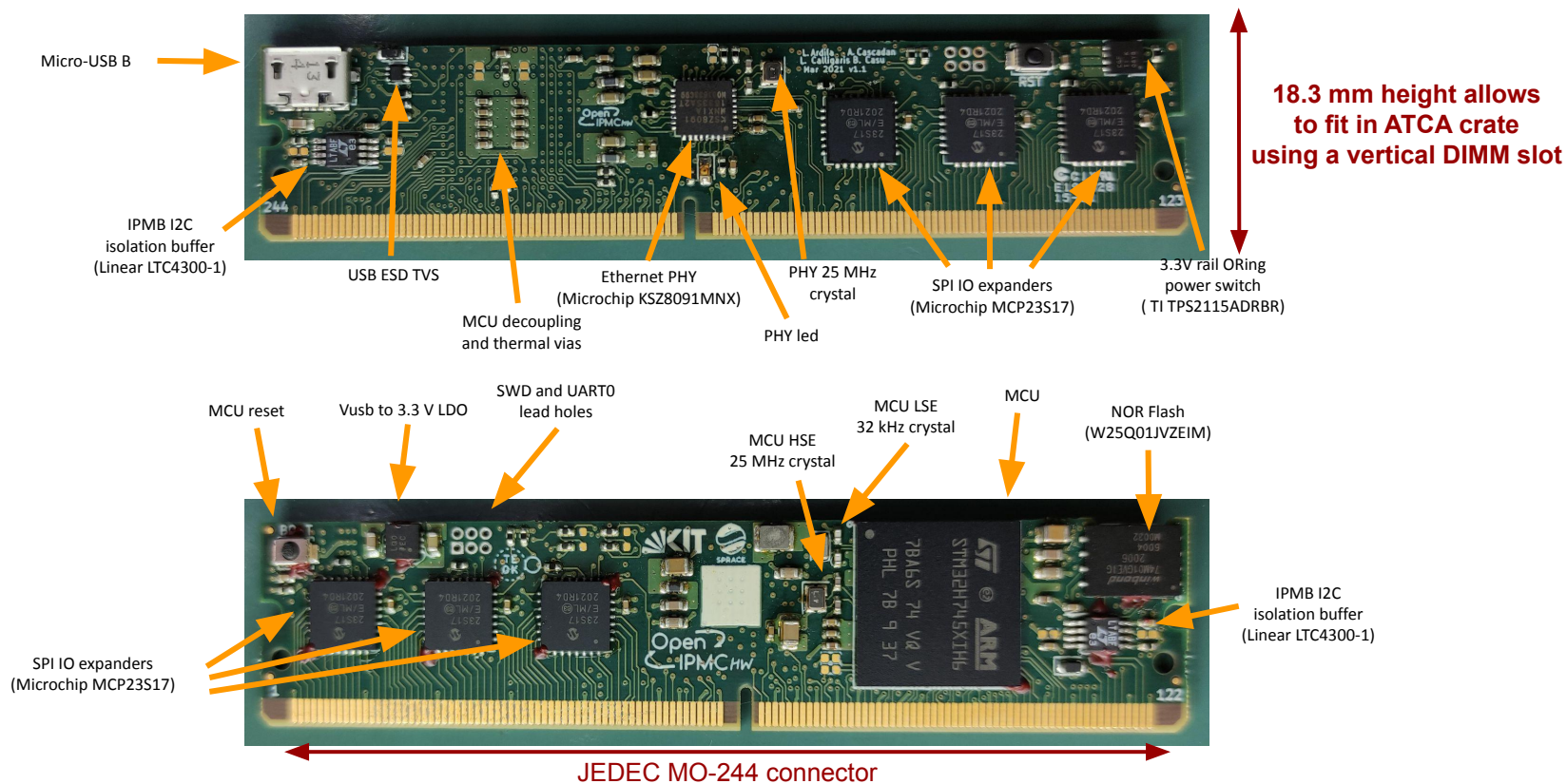


External flash

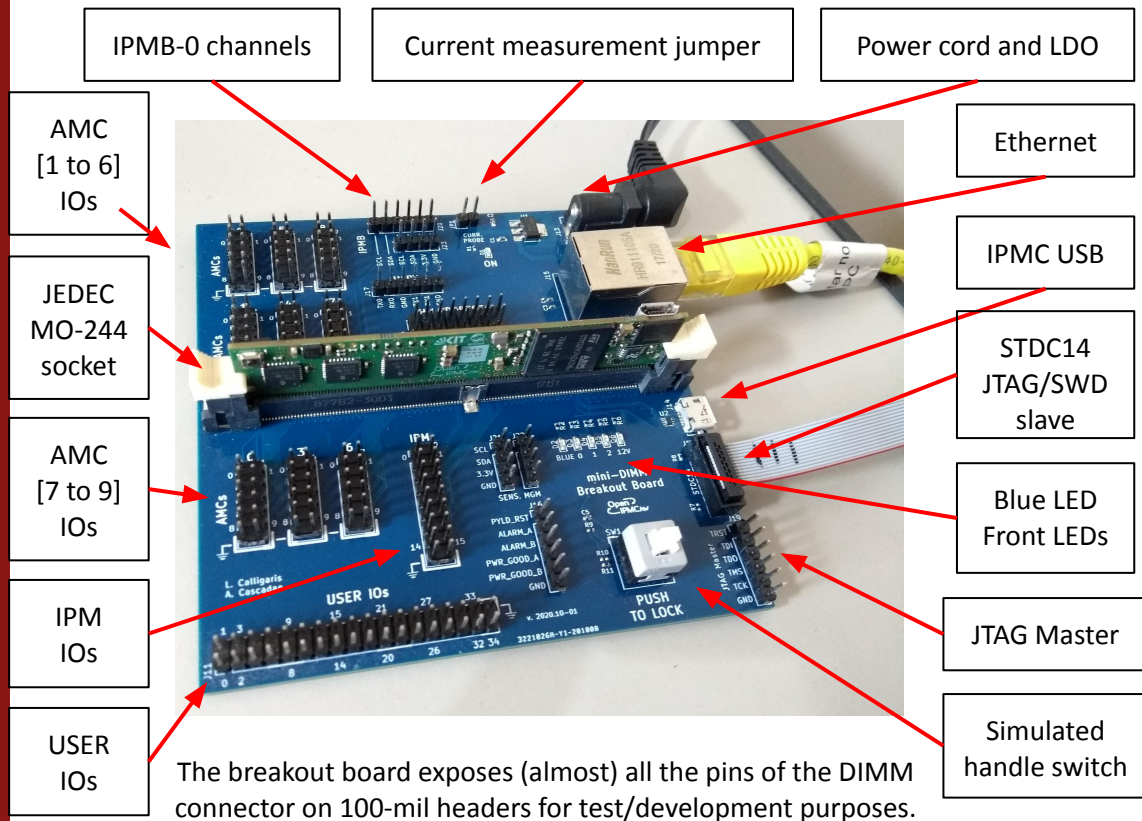
- The MCU supports external QSPI flash
- We added one to the DIMM to
 - Store configuration
 - Aid in firmware upgrade binary gymnastics
 - Store a failsafe “golden image”
- Our chosen part is Winbond W74M01GVZEIG
 - WSON-8 package
 - 1 Gbit = 128 MiB with 4kiB erasable blocks
 - Cheap (7.33 USD)
 - Currently severely impacted by chip shortage
 - Pin-compatible alternative parts from Micron
 - MT25QL01G BBB1EW9 (but costs twice as much)



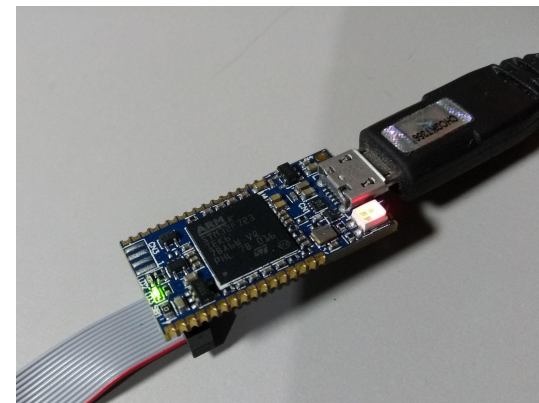
OpenIPMC-HW layout: picture



Breakout Board used for development & programming



We plan to make a small update adding the breakout for 12V_EN



STLink-V3MINI JTAG/SWD debugger
Cost: around 10 USD

The breakout board is very inexpensive:

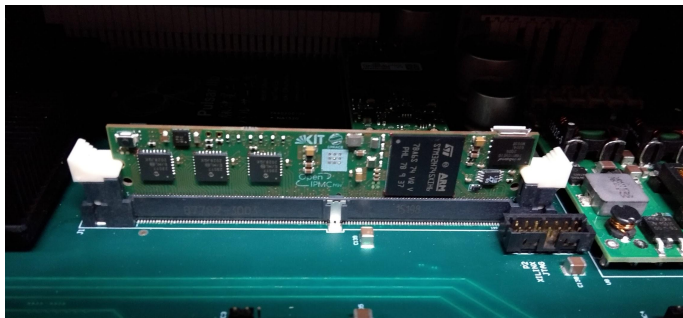
- 10 PCB + shipping = 26 USD
- Dimm connector = 17 USD
- The other components are cheaper

OpenIPMC-HW on ATCA boards

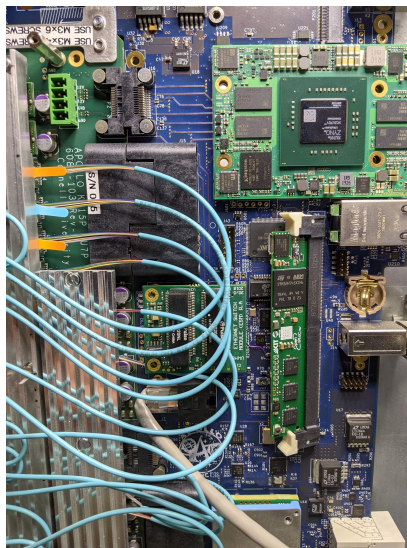
Test setups

- OpenIPMC-HW is currently being tested in 3 ATCA boards
 - Pulsar-IIb, at SPRACE (São Paulo)
 - Serenity, at KIT (Germany) and CERN
 - Apollo, at Boston University

For each target board, the OpenIPMC-FW code is forked and adapted to the specific hardware. We took care to make this process easy for users.



Pulsar-IIb @ SPRACE



Apollo @ BU



Serenity @ KIT

Sensor readings

```
#
# clia sensordata 8c
Pigeon Point Shelf Manager Command Line Interpreter

HotSwap Sensor → 8c: LUN: 0, Sensor # 1 ("Hot Swap Carrier")
                    Type: Discrete (0x6f), "Hot Swap" (0xf0)
                    Belongs to entity (0xa0, 0x60): FRU # 0
                    Status: 0xc0
                    All event messages enabled from this sensor
                    Sensor scanning enabled
                    Initial update completed
                    Sensor reading: 0x00
                    Current State Mask 0x0010

IPMB Sensor → 8c: LUN: 0, Sensor # 2 ("IPMB-0 Sensor")
                 Type: Discrete (0x6f), "IPMB Link" (0xf1)
                 Belongs to entity (0xa0, 0x60): FRU # 0
                 Status: 0xc0
                 All event messages enabled from this sensor
                 Sensor scanning enabled
                 Initial update completed
                 Sensor reading: 0x88
                 Current State Mask 0x0008

Temperature form PIM400 → 8c: LUN: 0, Sensor # 3 ("TEMP PIM400")
                           Type: Threshold (0x01), "Temperature" (0x01)
                           Belongs to entity (0xa0, 0x60): FRU # 0
                           Status: 0xc0
                           All event messages enabled from this sensor
                           Sensor scanning enabled
                           Initial update completed
                           Raw data: 42 (0x2a)
                           Processed data: 32.320000 degrees C
                           Current State Mask: 0x00
```

```
8c: LUN: 0, Sensor # 4 ("CURRENT PIM400") ← Current on PIM400
    Type: Threshold (0x01), "Current" (0x03)
    Belongs to entity (0xa0, 0x60): FRU # 0
    Status: 0xc0
    All event messages enabled from this sensor
    Sensor scanning enabled
    Initial update completed
    Raw data: 3 (0x03)
    Processed data: 0.282000 Amps
    Current State Mask: 0x00

8c: LUN: 0, Sensor # 5 ("-48V_A PIM400") ← Voltage on -48 line
    Type: Threshold (0x01), "Voltage" (0x02) ← (Channels A and B)
    Belongs to entity (0xa0, 0x60): FRU # 0
    Status: 0xc0
    All event messages enabled from this sensor
    Sensor scanning enabled
    Initial update completed
    Raw data: 162 (0xa2)
    Processed data: 52.650000 Volts
    Current State Mask: 0x00

8c: LUN: 0, Sensor # 6 ("-48V_B PIM400")
    Type: Threshold (0x01), "Voltage" (0x02)
    Belongs to entity (0xa0, 0x60): FRU # 0
    Status: 0xc0
    All event messages enabled from this sensor
    Sensor scanning enabled
    Initial update completed
    Raw data: 162 (0xa2)
    Processed data: 52.650000 Volts
    Current State Mask: 0x00

#
```

Sensor reading test: Shelf Manager CLI is printing the sensor readings of Serenity @ KIT.

Sensor readout test at CMS TIF



credits: Giacomo Fedi

An OpenIPMC-HW was left reading out sensors on the PIM400 of its hosting Serenity board at TIF. The values were fed into the TIF Carbon server and plotted with Grafana. Data readout was stable.

Polaris PICMG standards compliance tests

- Verification of compliance with PICMG standard requires many tests
 - Needs an automated system allowing to perform tests in batches
- We are using an ATCA compliance testing sw by Polaris Networks
 - Kindly provided by the CERN EP-ESE group at bldg 14. Thanks!
- OpenIPMC-HW was put to test with the CERN Polaris setup
 - The results (below) have been fundamental in orienting our improvements
 - We will keep to use this tool to orient our improvements

PASSED	FAILED	SKIPPED	TOTAL
56 (56%)	17	26	99

Summary and outlook

- Following the development of OpenIPMC, we designed an IPMC module
 - Mini-DIMM form factor, pin-, function- and mechanically-compatible w/ CERN IPMC
 - Based on a powerful STM32H745 microcontroller
 - Board design and firmware released under open source license
- We now develop for three target boards: Pulsar-IIb, Serenity and Apollo
 - Firmware can be customized for each target board rather easily
 - Tests for the implemented IPMI and non IPMI functions have been successful
- Testing for compliance with the Polaris Network tester is very encouraging
 - 56% of the tests successful, most of failures due to still missing features (multi records,..)
 - We are aiming to smooth these issues soon
- We are looking into extending features to include HPM.1, HPM.2 and HPM.3 standards

Repositories on Gitlab

OpenIPMC (IPMC software)

- gitlab.com/openipmc/openipmc

OpenIPMC-FW (DIMM firmware)

- gitlab.com/openipmc/openipmc-fw



OpenIPMC-HW (DIMM board design)

- gitlab.com/openipmc/openipmc-hw

Breakout baseboard

- gitlab.com/openipmc/openipmc-hw_debug-base



Open 
 IPMC

Questions?

Backup Slides

Command Line Interface: Telnet & UART

- CLI: allows extra control and debug capabilities beyond IPMI protocol (via Telnet or UART)
- Telnet: allows remote connection to IPMC or to any device on board if associated to a UART port

```
File Edit View Search Terminal Help
cascadan@ipecluster2:~$
cascadan@ipecluster2:~$
cascadan@ipecluster2:~$
cascadan@ipecluster2:~$
cascadan@ipecluster2:~$
cascadan@ipecluster2:~$
cascadan@ipecluster2:~$
cascadan@ipecluster2:~$
cascadan@ipecluster2:~$
cascadan@ipecluster2:~$ telnet 192.168.10.30
Trying 192.168.10.30...
Connected to 192.168.10.30.
Escape character is '^]'.

>> info
OpenIPMC-HW
Firmware commit: db7e6708

Target Board: OpenIPMC-HW
IPMB-0 Addr: 0x8c

>>
>> debug-ipmi
IPMB-0 rcvd: 8c 10 64 20 34 2d 03 7c
Get Sensor Reading
IPMB-0 sent: 20 14 cc 8c 34 2d 00 2a c0 00 00 29

IPMB-0 rcvd: 8c 10 64 20 38 2d 03 78
Get Sensor Reading
IPMB-0 sent: 20 14 cc 8c 38 2d 00 2b c0 00 00 24

Key ESC
msg: Command abort
>>

File Edit View Search Terminal Help
Welcome to minicom 2.7

OPTIONS: I18n
Compiled on Nov 15 2018, 20:18:47.
Port /dev/ttyACM0, 19:50:56

Press CTRL-A Z for help on special keys

>> info
OpenIPMC-HW
Firmware commit: db7e6708

Target Board: OpenIPMC-HW
IPMB-0 Addr: 0x8c

>>
>> debug-ipmi
IPMB-0 rcvd: 8c 10 64 20 34 2d 03 7c
Get Sensor Reading
IPMB-0 sent: 20 14 cc 8c 34 2d 00 2a c0 00 00 29

IPMB-0 rcvd: 8c 10 64 20 38 2d 03 78
Get Sensor Reading
IPMB-0 sent: 20 14 cc 8c 38 2d 00 2b c0 00 00 24

Key ESC
msg: Command abort
>>

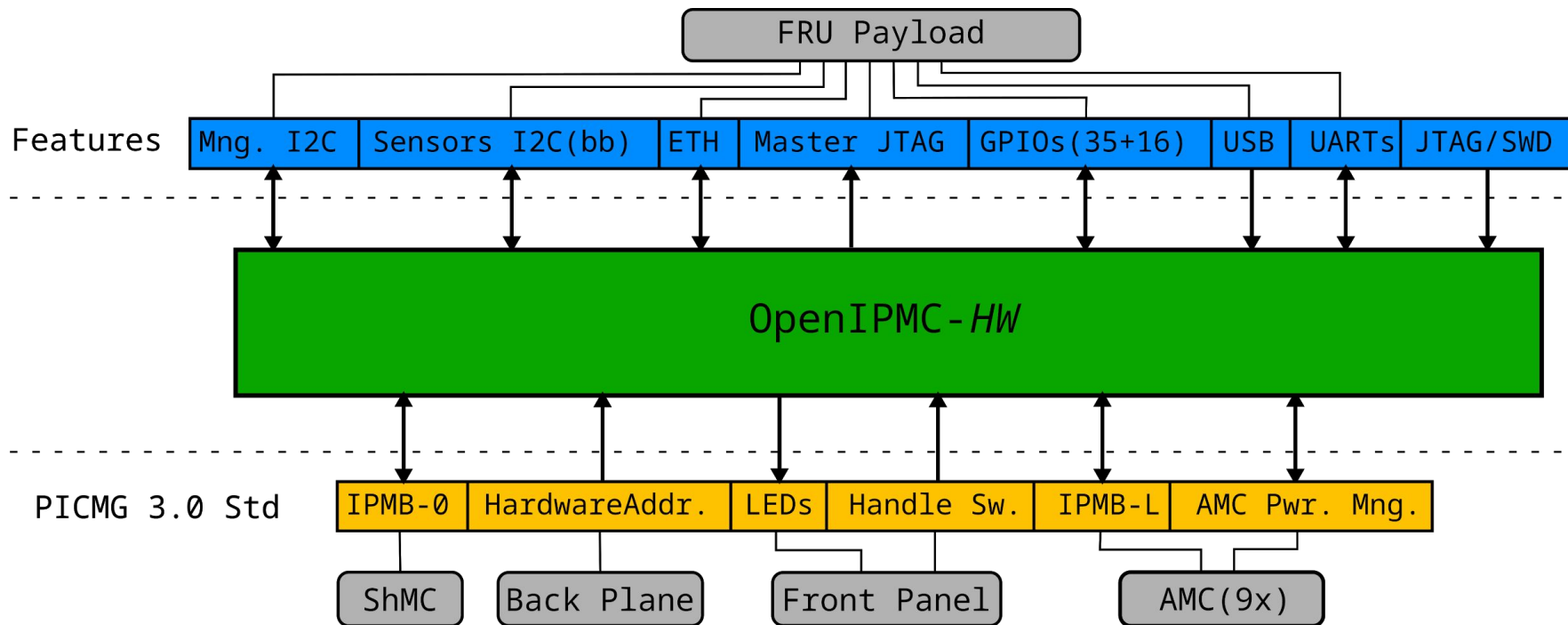
CTRL-A Z for help | 115200 8N1 | NOR | Minicom 2.7 | VT102 | Offline | ttyACM0
```

Telnet

DIMM-UARTO (via Minicom)

The CLI can r/w simultaneously over two separate channels

OpenIPMC-HW DIMM connections



Note: among the GPIOs some pins can be configured as UARTs, following the SoC Interest group layout

STM32H745XI Microcontroller: specs

- Cores

- 1x ARM Cortex-M7 (480 MHz max)
- 1x ARM Cortex-M4 (240 MHz max)

- Package

- 265-TFBGA
- 14x14mm
- 0.8mm pitch

- Memory

- 2x 1 Mbyte Flash
- 64 I + 128 D Kbytes TCM (M7 only)
- 864 Kbytes SRAM

- Power

- Input 1.62 to 3.6 V
- Integrated SMPS+LDO

- IOs

- 168x GPIOs
- 4x I²C
- 6x SPI
- 8x UART
- Ethernet MAC
- USB host/device/OTG
- Quad-SPI

- Others

- LCD-TFT
- JPEG Codec
- ADCs
- DACs
- OpAmps
- Graphical Accelerator

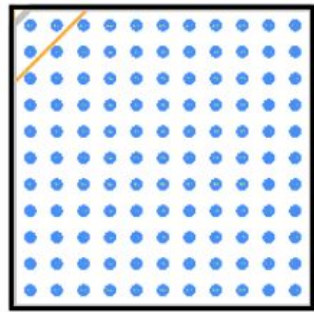


TFBGA 240+25

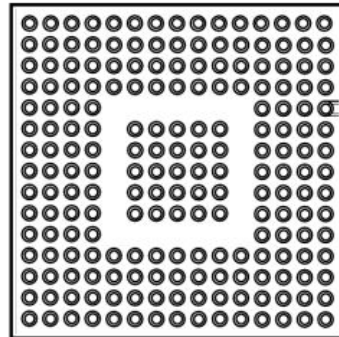
Changes compared to previous presentations

- Platform is now called **OpenIPMC-HW**
- Switched MCU from **STM32H745II** (176 balls 0.65mm pitch) to **STM32H745XI** (240 balls 0.8mm pitch)
 - It's an elephant, but it seems to still fit on available board space, and **is easier to solder**
- Removed iCE40 FPGA from the design (as suggested by Peter Wittich)
 - Makes the hardware design and signal routing easier
 - Removes the necessity of programming a second device in the board

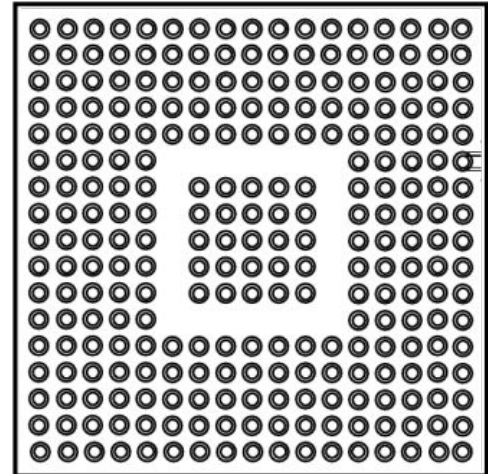
iCE40HX8K
caBGA121 (9x9mm) P0,80mm



STM32H745II
UFBGA176 + 25 (10x10mm) P0,65mm

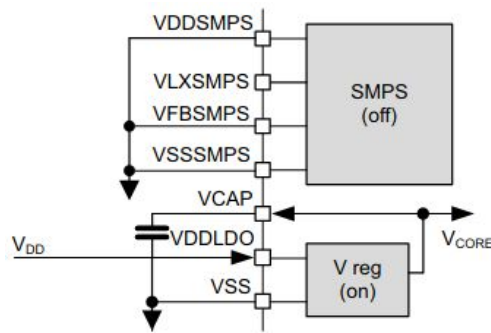


STM32H745XI
TFBGA240 + 25 (14x14mm) P0,80mm

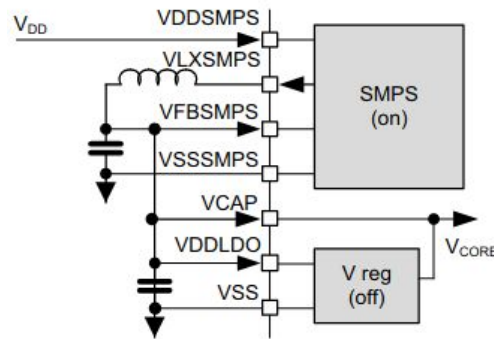


STM32H745XI Microcontroller: SMPS x LDO

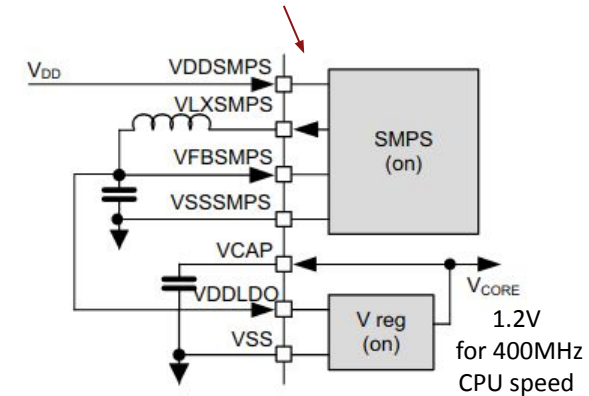
- Vcore power sources
 - Integrated step-down SMPS and LDO to be chosen or combined
 - Each power scheme requires a different off-chip extra circuitry
- Options available in OpenIPMC-HW (by add/remove components)
 - LDO only: low efficiency
 - SMPS only: high efficiency
 - SMPS supplying LDO: good efficiency & maximum CPU speeds



LDO only



SMPS only



SMPS supplying LDO





















Polaris test @ CERN 06/05/2021 page 1/6

<input type="checkbox"/>	Req 3.1 IPMI Request and Response Format	Failed	05-06-2021 15:12:44... Multiple Errors Occured. Last Error: Get Event Receiver failed with Completion Code 0xC1.
<input checked="" type="checkbox"/>	Req 3.2 NetFn Used by ATCA Defined Commands Request	Passed	05-06-2021 15:12:44... Validated that AdvancedTCA defined commands use a NetFn of 2Ch in the request.
<input checked="" type="checkbox"/>	Req 3.3 NetFn Used by ATCA Defined Commands Response	Passed	05-06-2021 15:12:46... Validated that responses to AdvancedTCA defined commands use a NetFn of 2Dh.
<input checked="" type="checkbox"/>	Req 3.4 PICMG Identifier Used by ATCA Defined Commands	Passed	05-06-2021 15:12:46... Validated that the first byte of the Data Bytes area of both the ATCA request and response are the PICMG identifier of 00h.
<input checked="" type="checkbox"/>	Req 3.5 Reserved Bits in all Commands	Passed	05-06-2021 15:12:47... Validated that reserved bits and fields in commands (request messages) and responses are written as 0.
<input checked="" type="checkbox"/>	Req 3.13 Invalid Completion Code for Not Applicable Commands	Passed	05-06-2021 15:12:48... Validated that IPM Controller returns a Completion Code of Invalid Command(C1h) to the IPMI commands that are listed as not applicable (NA) in the ...
<input checked="" type="checkbox"/>	Req 3.15 Completion Code Returned by IPM Controller	Passed	05-06-2021 15:12:49... Validated that the IPMC 0x8A returns the Completion Codes as described in the Completion Codes section of the IMPI Specification...
<input checked="" type="checkbox"/>	Req 3.17 Checking Invalid FRU Device ID in Request Data	Passed	05-06-2021 15:12:50... Validated that all commands that take a FRU Device ID exceeding the maximum value as request Data, IPMC returns a 'parameter Out of Range(C9h)' c...
<input checked="" type="checkbox"/>	Req 3.19 Checking FRU Device ID of Absent FRU in Request Data		
<input type="checkbox"/>	Req 3.21 Board Containing Multiple Physical Slots		
<input checked="" type="checkbox"/>	Req 3.26 Event Receiver and LUN	Failed	05-06-2021 15:12:51... Error: No support for Get Event Receiver command. (Completion Code = 0xC1)
<input checked="" type="checkbox"/>	Req 3.28 Event Generation in Response to Set Event Receiver Command	Failed	05-06-2021 15:12:52... Error: No support for Get Event Receiver command. (Completion Code = 0xC1)
<input checked="" type="checkbox"/>	Req 3.34 Entity of the Version Change Sensor	Skipped	05-06-2021 15:12:54... Skip cause: Carrier Manager (0x8A) does not implement Version Change Sensor
<input type="checkbox"/>	Req 3.35 Entity of the Version Change Sensor		
<input checked="" type="checkbox"/>	Req 3.46 Hardware to IPMB 0 Address Transformation	Passed	05-06-2021 15:12:54... Validated that each IPM Controller uses a validated Hardware Address shifted left one bit as the upper seven bits of the IPMB address and assign 0 as bit...
<input type="checkbox"/>	Req 3.62 Physical Slot Number of Front Board		
<input checked="" type="checkbox"/>	Req 3.74 Managed FRU Represented by IPM Controller	Passed	05-06-2021 15:12:55... Validated that for each IPMC, every FRU Device ID from 0 to Max FRU Device ID corresponds to a Managed FRU represented by that IPM Controller.
<input checked="" type="checkbox"/>	Req 3.82 Support of Get PICMG Properties Command for IPM Controller	Failed	05-06-2021 15:12:57... Max FRU Device ID in the Get PICMG Properties response is 0.
<input checked="" type="checkbox"/>	Req 3.83 Get Address Info Support for IPM Controller	Passed	05-06-2021 15:12:59... Validated that each IPM Controller supports the 'GetAddressInfo' command as defined in Table 3-13. "'Get Address Info' command (on IPM Controller...
<input checked="" type="checkbox"/>	Req 3.88 Site Type in Get Address Info Command	Passed	05-06-2021 15:12:59... Validated that an IPM Controller returns Site Type values as defined in Table 3-9. 'Site type values' in Get Address Info response.
<input checked="" type="checkbox"/>	Req 3.101 FRU State Support	Passed	05-06-2021 15:13:00... Validated that an intelligent FRU supports, on behalf of itself and all the other FRUs it represents, the FRU states
<input checked="" type="checkbox"/>	Req 3.103 Set FRU Activation Policy Command	Failed	05-06-2021 15:14:06... Error: Timeout waiting for transition of 0x8A FRU #0, M4->M5 (in range 5->12)
<input checked="" type="checkbox"/>	Req 3.138 Payload Power after Completion of Deactivation Process	Passed	05-06-2021 15:14:06... Validated the Payload Power when the IPMC with all its Managed FRUs have transitioned to M1 state...
<input type="checkbox"/>	Req 3.157 Transition to M0 State for FRU Device ID 0		
<input type="checkbox"/>	Req 3.184 Implementation of Cold Reset Command for IPM Controller		
<input checked="" type="checkbox"/>	Req 3.188 Implementation of Warm Reset Command for IPM Controller	Passed	05-06-2021 15:14:18... Validated that an IPM Controller (0x8A) does not implement the Warm Reset command.
<input checked="" type="checkbox"/>	Req 3.189 Operational State of IPMC and Payload Due to Warm Reset Command	Skipped	05-06-2021 15:14:18... Skip cause: Warm Reset command is not supported by IPMC: 0x8A (CC 0xc1).
<input checked="" type="checkbox"/>	Req 3.251 Support of Get FRU LED Properties Command for IPMC	Passed	05-06-2021 15:14:19... Validated that an IPM Controller implements the "Get FRU LED Properties" command.
<input checked="" type="checkbox"/>	Req 3.253 Support of Get LED Color Capabilities Command for IPMC	Passed	05-06-2021 15:14:20... Validated that an IPM Controller implements the Get LED Color Capabilities command
<input checked="" type="checkbox"/>	Req 3.254 Completion Code CCh in Response to Get LED Color Capabilities Command	Passed	05-06-2021 15:14:21... Validated that if an LED is not present or is not under the control of the IPM Controller, the IPM Controller returns the "invalid data field in Request (CCh)...
<input checked="" type="checkbox"/>	Req 3.257 Hardware Restriction Bit in Response to Get FRU LED State Command		
<input type="checkbox"/>	Req 3.258 Invalid Completion Code in Current State Due to Dissatisfy Hardware Restriction		
<input type="checkbox"/>	Req 3.264 RTM as Managed FRU		
<input type="checkbox"/>	Req 3.266 FRU Hotswap Sensor for RTM		
<input type="checkbox"/>	Req 3.274 RTM FRU Information		
<input type="checkbox"/>	Req 3.275 Message Bridging to Intelligent Sub FRU		
<input type="checkbox"/>	Req 3.276 IPMI Message Channel 7		
<input type="checkbox"/>	Req 3.277 Get Address Info from Channel 7		
<input checked="" type="checkbox"/>	Req 3.350 Sensor Device Commands	Passed	05-06-2021 15:14:24... Verified that IPM Controller (0x8A) implements the mandatory Sensor Device commands.
<input checked="" type="checkbox"/>	Req 3.351 Get Device SDR	Passed	05-06-2021 15:14:24... Verified that IPM Controller (0x8A) implements the mandatory Get Device SDR and Get Device SDR Info as per IPMI1.5 Errata 310.
<input type="checkbox"/>	Req 3.353 Reserve Device SDR Repository		
<input checked="" type="checkbox"/>	Req 3.354 FRU Device Locator Record	Passed	05-06-2021 15:14:25... Verified that IPM Controller 0x8A contains FRU Device Locator Records for each FRU that is represented by the IPM Controller except FRU Device ID 0.
<input checked="" type="checkbox"/>	Req 3.355 MC Device Locator Record	Passed	05-06-2021 15:14:26... Verified that the IPMC 0x8A contains a Management Device Controller Record that described the IPMC and FRU Device ID ...
<input checked="" type="checkbox"/>	Req 3.356 Sensors of IPMC and all its Managed FRU is Described in Sensor Data Record	Passed	05-06-2021 15:14:28... Validated that each IPMC maintains a Sensor Data Record for every sensor that it wants to report to the Shelf Manager for every sensor on every present...
<input type="checkbox"/>	Req 3.357 IPMC SDR Merging for Non Intelligent FRU		
<input type="checkbox"/>	Req 3.358 IPMC SDR Removing for Non Intelligent FRU		
<input checked="" type="checkbox"/>	Req 3.359 IPMC Implements Physical IPMB0 Sensor	Passed	05-06-2021 15:14:28... Validated that each IPM Controller implements a physical IPMB0-sensor.
<input type="checkbox"/>	Req 3.379 Entity ID and Entity Instance of Front Board		
<input type="checkbox"/>	Req 3.380 Entity ID Entity Instance of RTM		
<input type="checkbox"/>	Req 3.385 Intelligent FRU Entity		
<input checked="" type="checkbox"/>	Req 3.390 Containment Relationship of Entity in Device SDRs	Skipped	05-06-2021 15:14:29... Skip cause: Device Entity Association record is not found.
<input checked="" type="checkbox"/>	Req 3.391 Top Level Containment	Skipped	05-06-2021 15:14:30... Skip cause: Device Entity Association record is not found.
<input type="checkbox"/>	Req 3.392 Entity of Non FRU Components		
<input checked="" type="checkbox"/>	Req 3.400 IPMC as Event Generator	Failed	05-06-2021 15:14:33... Error: IPMC 0x8A does not support Get Event Receiver Command.
<input checked="" type="checkbox"/>	Req 3.403 IPM Controller Sends All Events to Event Receiver	Failed	05-06-2021 15:14:33... Error: No support for Get Event Receiver command for the IPM Controller 0x8A. (Completion Code = 0xC1)
<input checked="" type="checkbox"/>	Req 3.405 FRU Inventory Device Command Support for IPM Controller	Passed	05-06-2021 15:14:34... Validated that each IPM Controller supports the FRU Inventory Device commands
<input checked="" type="checkbox"/>	Req 3.406 FRU Information is Available without Payload Power	Passed	05-06-2021 15:14:38... Validated that FRU information is available even when main power is not applied to the unit's Payload Function.

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<input checked="" type="checkbox"/>	Req 3.407 Primary FRU at FRU Device ID 0	Failed	05-06-2021 15:14:38.... Error: Device Capabilities field of Management Controller does not match with Additional Device Support of the response of Get Device Id Command.
<input checked="" type="checkbox"/>	Req 3.408 Contiguous FRU Device ID	Passed	05-06-2021 15:14:39.... Validated that FRU Device IDs are contiguous.
<input checked="" type="checkbox"/>	Req 3.409 Entity Responsible for Updating Checksums in FRU Information	Passed	05-06-2021 15:14:41.... Validated that the entity updating the FRU Information is responsible for updating all appropriate checksums as well.
<input type="checkbox"/>	Req 3.413 Population of Predefined Fields of FRU Information		
<input checked="" type="checkbox"/>	Req 3.414 Multi Records in Multi Record Information Area	Failed	05-06-2021 15:14:41.... Multirecord Info Area is not present in Carrier (0x8A) FRU Information
<input checked="" type="checkbox"/>	Req 3.415 Presence of Multirecord of IPMC Implementing Shelf FRU Information		
<input type="checkbox"/>	Req 3.416 Implementation of Board Info Area		
<input checked="" type="checkbox"/>	Req 3.418 Implementation of Chassis Info Area	Passed	05-06-2021 15:14:42.... Validated that the IPMC Controller not supporting the Shelf FRU Information populates the Chassis Info Area Starting Offset in the Common Header with...
<input type="checkbox"/>	Req 3.419 Implementation of Chassis Info Area for IPMC Implementing Shelf FRU Information		
<input checked="" type="checkbox"/>	Req 3.420 Board Point to Point Connectivity Record	Failed	05-06-2021 15:14:43.... Multirecord Area is not present in Carrier (0x8A) FRU Information
<input checked="" type="checkbox"/>	Req 3.421 Product Info Area for Non Zero FRUs	Passed	05-06-2021 15:14:45.... Validated that each IPMC Controller that represents one or more FRUs with a non-zero FRU Device ID provides a Product Info Area associated with the co...
<input checked="" type="checkbox"/>	Req 3.422 Product Info Area Identify Distinct FRU Types	Passed	05-06-2021 15:14:45.... Validated that for any two or more otherwise identical FRUs with visually distinct Face Plates, the Product Info Area Fields distinguish and identify the di...
<input checked="" type="checkbox"/>	Req 3.466 E-Keying Entry in Board FRU Information	Skipped	05-06-2021 15:14:48.... Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input checked="" type="checkbox"/>	Req 3.467 Get and Set Port State	Skipped	05-06-2021 15:14:48.... Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input type="checkbox"/>	Req 3.487 Board Channel in Board FRU Information		
<input type="checkbox"/>	Req 3.488 Separate Link Descriptor for every Protocol in a Channel		
<input checked="" type="checkbox"/>	Req 3.491 Multi Channel Links in Board FRU Information	Skipped	05-06-2021 15:14:49.... Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input type="checkbox"/>	Req 3.492 Link Descriptor in Board FRU Information		
<input type="checkbox"/>	Req 3.493 Link Designator in Board FRU Information		
<input checked="" type="checkbox"/>	Req 3.494 Link Type Values in Board FRU Information	Skipped	05-06-2021 15:14:50.... Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input checked="" type="checkbox"/>	Req 3.495 Link Type Extension Values in Board FRU Information	Skipped	05-06-2021 15:14:51.... Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input checked="" type="checkbox"/>	Req 3.496 Link Type in Range F0 to FE in Board FRU Information	Skipped	05-06-2021 15:14:52.... Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input checked="" type="checkbox"/>	Req 3.497 Combined OEM GUID Table in Board Point to Point Connectivity Record	Skipped	05-06-2021 15:14:53.... Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input checked="" type="checkbox"/>	Req 3.498 OEM GUID in Board Point to Point Connectivity Record	Skipped	05-06-2021 15:14:54.... Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input checked="" type="checkbox"/>	Req 3.503 Data Format of Set Port State Command	Skipped	05-06-2021 15:14:55.... Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input checked="" type="checkbox"/>	Req 3.504 Data Format of Get Port State Command	Skipped	05-06-2021 15:14:56.... Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input checked="" type="checkbox"/>	Req 3.603 IPMB 0 Sensors for IPMC	Passed	05-06-2021 15:14:57.... Validated the physical IPMB-0 sensors are implemented by each IPMC Controller and used to monitor the state of the IPMBs.
<input checked="" type="checkbox"/>	Req 3.604 Get Sensor Reading for Physical IPMB 0 Sensor	Passed	05-06-2021 15:14:58.... Validated the data format of "Get Sensor Reading" command (physical IPMB-0 sensor)
<input checked="" type="checkbox"/>	Req 3.607 Get IPMB Link Info Command for IPMC Not Connecting to IPMB-0 on a Radial Basis	Failed	05-06-2021 15:14:59.... Get IPMB Link Info command returns 0xC1 instead of 0x00 as Completion Code.
<input checked="" type="checkbox"/>	Req 3.608 C9n Completion Code for Get IPMB Link Info	Failed	05-06-2021 15:15:00.... Get IPMB Link Info command returns 0xC1 instead of 0xC9 as Completion Code.
<input checked="" type="checkbox"/>	Req 3.609 Physical IPMB 0 Status Change Event Message	Failed	05-06-2021 15:15:32.... Error: Timeout waiting for IPMB-0 Status Change event (in range 39->39)
<input checked="" type="checkbox"/>	Req 3.610 Set IPMB State Command Support	Passed	05-06-2021 15:15:32.... Validated the data format for the Set IPMB State command.
<input checked="" type="checkbox"/>	Req 3.611 IPMC Refuses Set IPMB State Causing for Isolation	Passed	05-06-2021 15:15:34.... Validated that an IPMC Controller refuses any "Set IPMB State" command that would cause it to become isolated from both buses.
<input type="checkbox"/>	Req 3.612 IPMC Operation With Both Buses		
<input checked="" type="checkbox"/>	Req 3.613 Invalid Command C1n Completion Code for Set IPMB State Command	Passed	05-06-2021 15:15:34.... Validated that an IPMC that does not connect to IPMB-0 on a radial basis and receives a radial-topology-specific "Set IPMB State" request returns an "In...
<input checked="" type="checkbox"/>	Req 3.614 Set IPMB State Command in a Radial Topology	Skipped	05-06-2021 15:15:35.... Skip cause: No IPMB Link Mapping Record found
<input type="checkbox"/>	Req 3.627 Status of the FRU Local IPMB Segment		
<input checked="" type="checkbox"/>	Req 3.668 Power Command Support	Passed	05-06-2021 15:15:49.... Validated that IPMC supports the Power Commands for every FRU that it supports.
<input type="checkbox"/>	Req 3.669 Compute Power Properties Command Support		
<input checked="" type="checkbox"/>	Req 3.674 Power Draws through Set Power Level Command	Passed	05-06-2021 15:15:49.... Validated the Minimum and Maximum Power Draws through Get Power Level command.
<input checked="" type="checkbox"/>	Req 3.676 Power Level Value while FRU is in Steady State Power Draw Level	Passed	05-06-2021 15:15:53.... Validated Power Level Values in Steady State Power Draw Levels.
<input checked="" type="checkbox"/>	Req 3.679 Power Level in early Power Draw Levels	Failed	05-06-2021 15:16:03.... Error: Power Drawn is not same as previously granted via the "Set Power Level" command (index: 0)
<input checked="" type="checkbox"/>	Req 3.680 Compute Power Properties Locks Different Power Levels	Passed	05-06-2021 15:16:27.... Validated that the IPMC locks "Desired steady state power draw levels" and "Desired early levels" after it receives "Compute Power Properties" comman...
<input checked="" type="checkbox"/>	Req 3.681 Compute Power Properties Locks Power Draws	Passed	05-06-2021 15:16:50.... Validated that the IPMC 0x8A locks the Power Draw Array Size and the Values after it receives "Compute Power Properties" command.
<input checked="" type="checkbox"/>	Req 3.682 Power Draw Adjustment Due to Set Power Level Command	Passed	05-06-2021 15:17:27.... Validated the Power Draw Adjustment Due to the Set Power Level command.
<input checked="" type="checkbox"/>	Req 3.683 Power Draw Levels for Different Power Types	Passed	05-06-2021 15:17:28.... Validated that the Power Draws is not greater for the "Desired steady state draw levels" than the Power Draws for the "Desired early levels" values.
<input checked="" type="checkbox"/>	Req 3.684 FRU Power up by Set Power Level Command	Passed	05-06-2021 15:17:51.... Validated that the IPMC 0x8A does not Power up any of its FRUs until it receives a Set Power Level command with a power level greater than 0 from the...
<input checked="" type="checkbox"/>	Req 3.685 Power Management of IPMC	Passed	05-06-2021 15:17:57.... Validated the Power Management of IPMC via Get and Set Power Level commands.
<input checked="" type="checkbox"/>	Req 3.736 Temperature Sensor	Passed	05-06-2021 15:17:57.... Validated that all Boards and other intelligent FRUs support at least one temperature sensor and its corresponding sensor record (SDR).
<input checked="" type="checkbox"/>	Req 3.739 Readability of Temperature Sensor	Passed	05-06-2021 15:17:58.... Validated that even if represented by a "virtual sensor", each temperature sensor is individually readable.
<input checked="" type="checkbox"/>	Req 3.741 Power Supply Sensor	Passed	05-06-2021 15:17:59.... Validated that all Boards and other intelligent FRUs support at least one power supply sensor monitoring the status of the power Feed fuses.
<input checked="" type="checkbox"/>	Req 3.742 Sensor Data Record for Power Supply Sensor	Passed	05-06-2021 15:18:00.... Validated that the Sensor Data Record shall be provided for each power supply sensor.
<input checked="" type="checkbox"/>	Req 3.744 Temperature Event Message	Passed	05-06-2021 15:18:11.... Validated that Temperature Event message have the data format defined in Table 3-92, "Temperature event message."
<input checked="" type="checkbox"/>	Req 3.745 Assert Deassert Temperature Events	Passed	05-06-2021 15:18:21.... Validated that IPMC Controllers indicate when they have reached a minor temperature alert condition by asserting a "07h = Upper Non-critical (minor) - ...
<input checked="" type="checkbox"/>	Req 3.746 Assert Deassert Temperature Events Critical	Skipped	05-06-2021 15:18:21.... Skip cause: All the temperature sensors are skipped
<input checked="" type="checkbox"/>	Req 3.747 Assert Deassert Temperature Events Upper Non Recoverable	Skipped	05-06-2021 15:18:22.... Skip cause: All the temperature sensors are skipped
<input checked="" type="checkbox"/>	Req 3.748 Temperature Sensors Threshold Commands	Failed	05-06-2021 15:18:23.... Error: Get Sensor Threshold failed for sensor 3. (Completion Code = 0xC1)
























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<input checked="" type="checkbox"/>  Req 3.749 Temperature Sensors Thresholds	Passed	05-06-2021 15:18:34.... Validated that all temperature sensors should have appropriate levels set for minor, major, and critical thresholds.
<input checked="" type="checkbox"/>  Req 3.750 Temperature Sensor Hysteresis Commands	Skipped	05-06-2021 15:18:34.... Skip cause: All the temperature sensors are skipped
<input checked="" type="checkbox"/>  Req 3.751 Temperature Sensor Default Hysteresis Values	Passed	05-06-2021 15:18:35.... Validated that all temperature sensors provide default hysteresis values.
<input checked="" type="checkbox"/>  Req 3.752 Critical Temperature Alert Condition	Skipped	05-06-2021 15:18:38.... Skip cause: No Fan Geography record found in the Shelf FRU Information.
<input checked="" type="checkbox"/>  Req 3.763 Telco Alarm Commands	Skipped	05-06-2021 15:18:38.... Skip cause: IPMC 0x8A does not implement any FRU with Telco Alarm functionality.
<input checked="" type="checkbox"/>  Req 3.764 Invalid Data Field in Request for Telco Alarm Commands	Skipped	05-06-2021 15:18:39.... Skip cause: IPMC 0x8A does not implement any FRU with Telco Alarm functionality.
<input checked="" type="checkbox"/>  Req 3.766 Telco Alarm State	Skipped	05-06-2021 15:18:41.... Skip cause: IPMC 0x8A does not implement any FRU with Telco Alarm functionality.
<input checked="" type="checkbox"/>  Req 3.767 Telco Alarm Input Sensor	Skipped	05-06-2021 15:18:41.... Skip cause: IPMC 0x8A does not implement any FRU with Telco Alarm functionality.
<input checked="" type="checkbox"/>  Req 3.768 Telco Alarm Event Message	Skipped	05-06-2021 15:18:42.... Skip cause: IPMC 0x8A does not implement any FRU with Telco Alarm functionality.
<input type="checkbox"/>  Req 3.769 Telco Alarm Minor Reset Input		
<input type="checkbox"/>  Req 3.770 Telco Alarm Major Reset Input		
<input type="checkbox"/>  Req 3.771 Telco Alarm Cutoff Function		
<input checked="" type="checkbox"/>  Req 3.772 Shelf Manager and IPMC Functionality	Passed	05-06-2021 15:18:43.... Validated that Shelf Manager and IPM Controller functions are supported as defined in Table 3-99.
<input checked="" type="checkbox"/>  Req 3.773 Command Number Assignment	Passed	05-06-2021 15:18:44.... Validated that IPMI Command number functions and requirements are supported as defined in Table 3-100.
<input checked="" type="checkbox"/>  Req 3.776 Sensor Specific Event Reading Type	Failed	05-06-2021 15:18:46.... Error: IPMC 0x8A does support Event Receiver command
<input checked="" type="checkbox"/>  Req 3.777 Entity ID Assignment	Passed	05-06-2021 15:18:46.... Validated that PICMG  Entity ID assignments shall be supported as defined in Table 3-104, "PICMG Entity ID assignments."
<input checked="" type="checkbox"/>  SDR Requirements	Failed	05-06-2021 15:18:48.... Get Device SDR Info reports wrong number of sensors for LUN 0 (8 instead of 6)
<input checked="" type="checkbox"/>  Board E-Keying	Skipped	05-06-2021 15:18:51.... Skip cause: No Board Point-to-Point Connectivity Record found
<input checked="" type="checkbox"/>  Watchdog Timer Commands Support	Skipped	05-06-2021 15:18:52.... Skip cause: No support for Watchdog Timer commands




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<input type="checkbox"/>	Req 3.1 IPMI Request and Response Format		
<input checked="" type="checkbox"/>	Req 3.2 NetFn Used by ATCA Defined Commands Request		
<input checked="" type="checkbox"/>	Req 3.3 NetFn Used by ATCA Defined Commands Response		
<input checked="" type="checkbox"/>	Req 3.4 PICMG Identifier Used by ATCA Defined Commands		
<input checked="" type="checkbox"/>	Req 3.5 Reserved Bits in all Commands		
<input checked="" type="checkbox"/>	Req 3.13 Invalid Completion Code for Not Applicable Commands		
<input checked="" type="checkbox"/>	Req 3.15 Completion Code Returned by IPM Controller		
<input checked="" type="checkbox"/>	Req 3.17 Checking Invalid FRU Device ID in Request Data		
<input checked="" type="checkbox"/>	Req 3.19 Checking FRU Device ID of Absent FRU in Request Data		
<input type="checkbox"/>	Req 3.21 Board Containing Multiple Physical Slots	Skipped	05-06-2021 16:40:56.... Skip cause: IPMC 0x8A does not span multiple slots.
<input checked="" type="checkbox"/>	Req 3.26 Event Receiver and LUN		
<input checked="" type="checkbox"/>	Req 3.28 Event Generation in Response to Set Event Receiver Command		
<input checked="" type="checkbox"/>	Req 3.34 Entity of the Version Change Sensor		
<input type="checkbox"/>	Req 3.35 Entity of the Version Change Sensor	Skipped	05-06-2021 16:41:07.... Skip cause: Carrier Manager (0x8A) does not implement any Version Change Sensor.
<input type="checkbox"/>	Req 3.46 Hardware to IPMB 0 Address Transformation		
<input type="checkbox"/>	Req 3.62 Physical Slot Number of Front Board	Passed	05-06-2021 16:41:19.... Validated that site number (7th byte of the response) is equal to Physical Slot Number of the front board.
<input checked="" type="checkbox"/>	Req 3.74 Managed FRU Represented by IPM Controller		
<input checked="" type="checkbox"/>	Req 3.82 Support of Get PICMG Properties Command for IPM Controller		
<input checked="" type="checkbox"/>	Req 3.83 Get Address Info Support for IPM Controller		
<input checked="" type="checkbox"/>	Req 3.88 Site Type in Get Address Info Command		
<input checked="" type="checkbox"/>	Req 3.101 FRU State Support		
<input checked="" type="checkbox"/>	Req 3.103 Set FRU Activation Policy Command		
<input checked="" type="checkbox"/>	Req 3.138 Payload Power after Completion of Deactivation Process		
<input type="checkbox"/>	Req 3.157 Transition to M0 State for FRU Device ID 0	Passed	05-06-2021 16:42:58.... Validated the transition to M0 State for the FRU #0 and all its managed FRUs.
<input checked="" type="checkbox"/>	Req 3.184 Implementation of Cold Reset Command for IPM Controller	Passed	05-06-2021 16:43:20.... Validated that an IPM Controller implements the Cold Reset command.
<input checked="" type="checkbox"/>	Req 3.188 Implementation of Warm Reset Command for IPM Controller		
<input checked="" type="checkbox"/>	Req 3.189 Operational State of IPMC and Payload Due to Warm Reset Command		
<input checked="" type="checkbox"/>	Req 3.251 Support of Get FRU LED Properties Command for IPMC		
<input checked="" type="checkbox"/>	Req 3.253 Support of Get LED Color Capabilities Command for IPMC		
<input checked="" type="checkbox"/>	Req 3.254 Completion Code CCh in Response to Get LED Color Capabilities Command		
<input checked="" type="checkbox"/>	Req 3.257 Hardware Restriction Bit in Response to Get FRU LED State Command	Passed	05-06-2021 16:44:07.... Validated that "Hardware restriction" bit (bit 3) is set in the LED States byte of the response to the Get FRU LED State command.
<input type="checkbox"/>	Req 3.258 Invalid Completion Code in Current State Due to Dissatisfy Hardware Restriction	Passed	05-06-2021 16:44:15.... Validated that While the hardware restriction is not met, the IPMC responds with return code D5h.
<input type="checkbox"/>	Req 3.264 RTM as Managed FRU	Skipped	05-06-2021 16:44:43.... Skip cause: The IPMC (0x8A) does not implement RTM.
<input type="checkbox"/>	Req 3.266 FRU Hotswap Sensor for RTM	Skipped	05-06-2021 16:44:52.... Skip cause: The IPMC (0x8A) does not implement RTM.
<input type="checkbox"/>	Req 3.274 RTM FRU Information	Skipped	05-06-2021 16:44:58.... Skip cause: The IPMC (0x8A) does not implement RTM.
<input type="checkbox"/>	Req 3.275 Message Bridging to Intelligent Sub FRU	Skipped	05-06-2021 16:45:19.... Skip cause: The IPMC (0x8A) does not implement ant managed FRU.
<input type="checkbox"/>	Req 3.276 IPMI Message Channel 7	Skipped	05-06-2021 16:46:26.... Skip cause: The IPMC (0x8A) does not implement ant managed FRU.
<input type="checkbox"/>	Req 3.277 Get Address Info from Channel 7	Skipped	05-06-2021 16:46:09.... Skip cause: The IPMC (0x8A) does not implement any intelligent FRU.
<input checked="" type="checkbox"/>	Req 3.350 Sensor Device Commands		
<input checked="" type="checkbox"/>	Req 3.351 Get Device SDR		
<input type="checkbox"/>	Req 3.353 Reserve Device SDR Repository	Passed	05-06-2021 16:47:33.... Verified that an IPM Controller, having SDR with length more than 24, implements Reserve Device SDR Repository command...
<input checked="" type="checkbox"/>	Req 3.354 FRU Device Locator Record		
<input checked="" type="checkbox"/>	Req 3.355 MC Device Locator Record		
<input checked="" type="checkbox"/>	Req 3.356 Sensors of IPMC and all its Managed FRU is Described in Sensor Data Record		
<input type="checkbox"/>	Req 3.357 IPMC SDR Merging for Non Intelligent FRU	Skipped	05-06-2021 16:48:15.... Skip cause: No non-intelligent FRU is available for the IPMC 0x8A.
<input type="checkbox"/>	Req 3.358 IPMC SDR Removing for Non Intelligent FRU	Skipped	05-06-2021 16:48:53.... Skip cause: No non-intelligent FRU is available for the IPMC 0x8A.
<input checked="" type="checkbox"/>	Req 3.359 IPMC Implements Physical IPMB0 Sensor		
<input type="checkbox"/>	Req 3.379 Entity ID and Entity Instance of Front Board	Skipped	05-06-2021 16:49:55.... Skip cause: Board containing the IPMC 0x8A is not a Multi Slot Board.
<input type="checkbox"/>	Req 3.380 Entity ID Entity Instance of RTM	Skipped	05-06-2021 16:50:53.... Skip cause: RTM is not implemented
<input type="checkbox"/>	Req 3.385 Intelligent FRU Entity	Passed	05-06-2021 16:51:37.... Validated that Entity in Management Controller Device Locator record for an IPM Controller is the intelligent FRU's entity.
<input checked="" type="checkbox"/>	Req 3.390 Containment Relationship of Entity in Device SDRs		
<input checked="" type="checkbox"/>	Req 3.391 Top Level Containment		
<input checked="" type="checkbox"/>	Req 3.392 Entity of Non FRU Components	Skipped	05-06-2021 16:52:15.... Skip cause: Device Entity Association record is not found
<input checked="" type="checkbox"/>	Req 3.400 IPMC as Event Generator		
<input checked="" type="checkbox"/>	Req 3.403 IPM Controller Sends All Events to Event Receiver		
<input checked="" type="checkbox"/>	Req 3.405 FRU Inventory Device Command Support for IPM Controller		
<input checked="" type="checkbox"/>	Req 3.406 FRU Information is Available without Payload Power		

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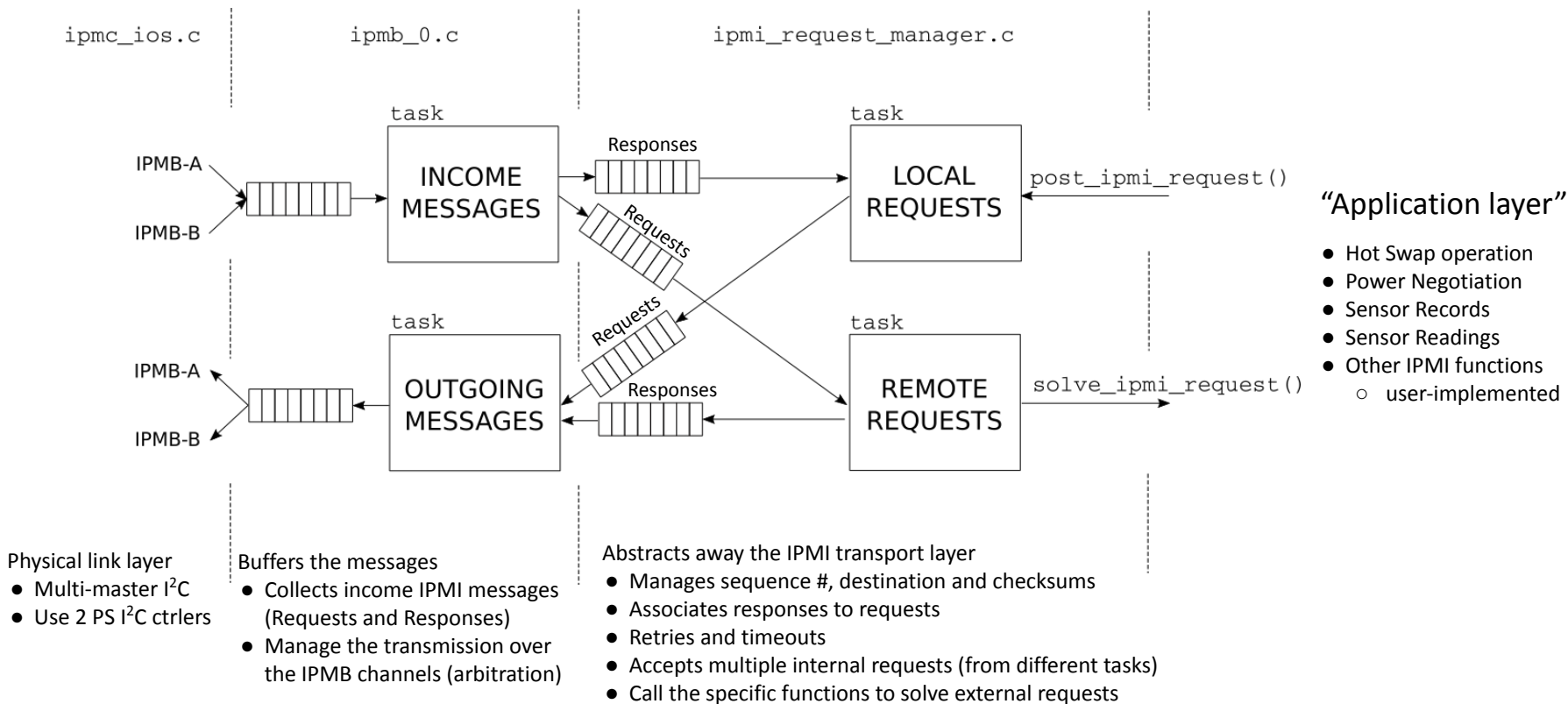
<input type="checkbox"/>  Req 3.412 Entry responsible for updating checkmarks in FRU information			
<input type="checkbox"/>  Req 3.413 Population of Predefined Fields of FRU Information	Passed	05-06-2021 16:55:06....	Validated that each IPM Controller populates all the predefined fields of the Board Info Area and Product Info Area associated with FRU Device ID 0, LUN.
<input type="checkbox"/>  Req 3.414 Multi Records in Multi Record Information Area			
<input type="checkbox"/>  Req 3.415 Presence of Multirecord of IPMC Implementing Shelf FRU Information	Failed	05-06-2021 16:58:59....	Error: Error while retrieving FRU #1 Information at 0x8A: Cannot Get FRU Inventory Area Info (FRU #1) cc=0xC9
<input type="checkbox"/>  Req 3.416 Implementation of Board Info Area	Passed	05-06-2021 16:56:55....	Validated that IPM Controllers implements valid data in all the predefined fields of the Board Info Area.
<input type="checkbox"/>  Req 3.418 Implementation of Chassis Info Area			
<input type="checkbox"/>  Req 3.419 Implementation of Chassis Info Area for IPMC Implementing Shelf FRU Information	Passed	05-06-2021 16:57:29....	Validated that each IPMC that is representing the Shelf FRU Information shall populate the Chassis Info Area Starting Offset with a valid offset to the Ch...
<input type="checkbox"/>  Req 3.420 Board Point to Point Connectivity Record			
<input type="checkbox"/>  Req 3.421 Product Info Area for Non Zero FRUs			
<input type="checkbox"/>  Req 3.422 Product Info Area Identify Distinct FRU Types			
<input type="checkbox"/>  Req 3.466 E-Keying Entry in Board FRU Information			
<input type="checkbox"/>  Req 3.467 Get and Set Port State			
<input type="checkbox"/>  Req 3.487 Board Channel in Board FRU Information	Skipped	05-06-2021 16:59:43....	Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input type="checkbox"/>  Req 3.488 Separate Link Descriptor for every Protocol in a Channel	Skipped	05-06-2021 16:59:54....	Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input type="checkbox"/>  Req 3.491 Multi Channel Links in Board FRU Information			
<input type="checkbox"/>  Req 3.492 Link Descriptor in Board FRU Information	Skipped	05-06-2021 17:00:04....	Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input type="checkbox"/>  Req 3.493 Link Designator in Board FRU Information	Skipped	05-06-2021 17:00:14....	Skip cause: No Board Point To Point Connectivity Record (PICMG Record ID: 0x14) is found in Shelf FRU Information
<input type="checkbox"/>  Req 3.494 Link Type Values in Board FRU Information			
<input type="checkbox"/>  Req 3.495 Link Type Extension Values in Board FRU Information			
<input type="checkbox"/>  Req 3.496 Link Type in Range F0 to FE in Board FRU Information			
<input type="checkbox"/>  Req 3.497 Combined OEM GUID Table in Board Point to Point Connectivity Record			
<input type="checkbox"/>  Req 3.498 OEM GUID in Board Point to Point Connectivity Record			
<input type="checkbox"/>  Req 3.503 Data Format of Set Port State Command			
<input type="checkbox"/>  Req 3.504 Data Format of Get Port State Command			
<input type="checkbox"/>  Req 3.603 IPMB 0 Sensors for IPMC			
<input type="checkbox"/>  Req 3.604 Get Sensor Reading for Physical IPMB 0 Sensor			
<input type="checkbox"/>  Req 3.607 Get IPMB Link Info Command for IPMC Not Connecting to IPMB-0 on a Radial Basis			
<input type="checkbox"/>  Req 3.608 C9h Completion Code for Get IPMB Link Info			
<input type="checkbox"/>  Req 3.609 Physical IPMB 0 Status Change Event Message			
<input type="checkbox"/>  Req 3.610 Set IPMB State Command Support			
<input type="checkbox"/>  Req 3.611 IPMC Refuses Set IPMB State Causing for Isolation			
<input type="checkbox"/>  Req 3.612 IPMC Operation With Both Buses	Passed	05-06-2021 17:01:02....	Validated that each IPM Controller begins operation with both buses in Local Control state.
<input type="checkbox"/>  Req 3.613 Invalid Command C1h Completion Code for Set IPMB State Command			
<input type="checkbox"/>  Req 3.614 Set IPMB State Command in a Radial Topology			
<input type="checkbox"/>  Req 3.627 Status of the FRU Local IPMB Segment	Passed	05-06-2021 17:01:33....	Validated that reading the IPMB-0 sensor, returns the status of the FRU's local IPMB segment
<input type="checkbox"/>  Req 3.668 Power Command Support			
<input type="checkbox"/>  Req 3.669 Compute Power Properties Command Support	Passed	05-06-2021 17:01:30....	Validated the support for "Compute Power Properties command" for single slot boards, non-Board FRU and multi slot boards.
<input type="checkbox"/>  Req 3.674 Power Draws through Get Power Level Command			
<input type="checkbox"/>  Req 3.678 Power Level Value while FRU is in Steady State Power Draw Level			
<input type="checkbox"/>  Req 3.679 Power Level in early Power Draw Levels			

Polaris test @ CERN 06/05/2021 page 6/6

-  Req 3.769 Telco Alarm Minor Reset Input
-  Req 3.770 Telco Alarm Major Reset Input
-  Req 3.771 Telco Alarm Cutoff Function
-  Req 3.772 Shelf Manager and IPMC Functionality
-  Req 3.773 Command Number Assignment

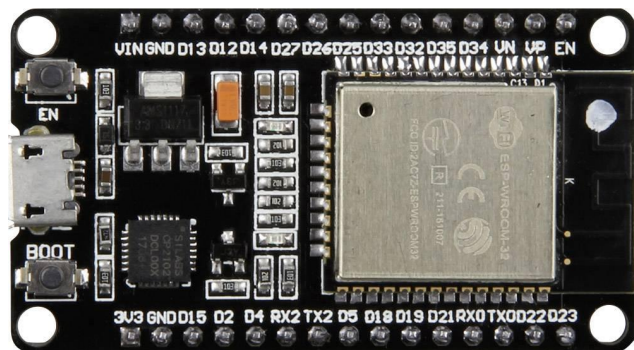
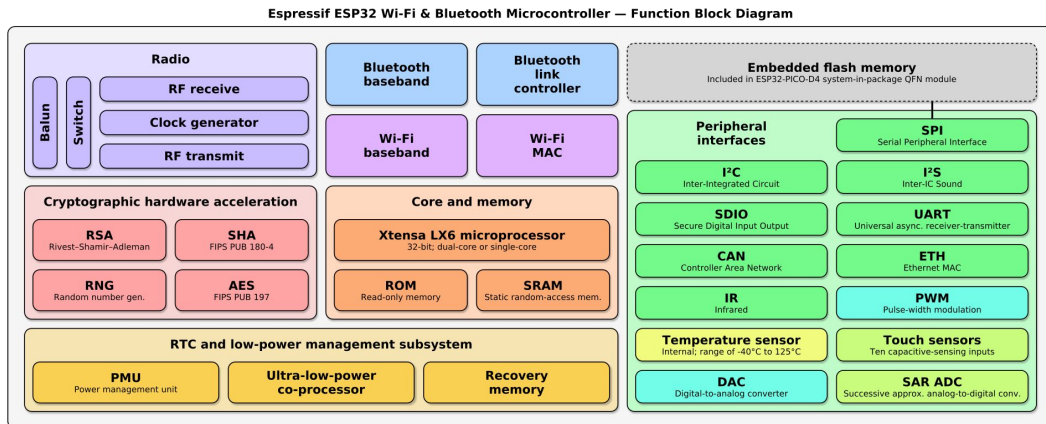
Skipped 05-06-2021 17:04:18.... Skip cause: IPMC 0x8A does not implement any FRU with Telco Alarm functionality.
Skipped 05-06-2021 17:04:19.... Skip cause: IPMC 0x8A does not implement any FRU with Telco Alarm functionality.
Skipped 05-06-2021 17:04:20.... Skip cause: IPMC 0x8A does not implement any FRU with Telco Alarm functionality.

OpenIPMC Internal Concept



OpenIPMC on ESP32 (Espressif Systems, CN)

- Quite powerful & flexible uC
 - 240 MHz Xtensa LX6 dual core
 - FPU, Big INTs & Crypto
 - WiFi, BT, SPI, I2C, UART...
 - **FreeRTOS support**
- Cheap Linux-supported boards
 - CP2102 USBtoUART converter
 - Boards sell for 5\$
- 3.3 V device (same as IPMB)
- Development software
 - Arduino IDE, PlatformIO or esp-idf
- Very different arch w.r.t a Zynq US+
 - Good exercise on portability/



IPMC firmware & board for Pulsar-2b

- SPRACE collab with Fermilab (2014-2016)

- **AM+FPGA L1 Track Finder**
- One contribution was the **IPMC for the Pulsar-2b**
- MCU: NXP LPC1700 (ARM Cortex-M3)
- RTOS: ARM Keil RTX (proprietary compiler)
- IPMC worked well and reliably, but....

- **Non-generic implementation**

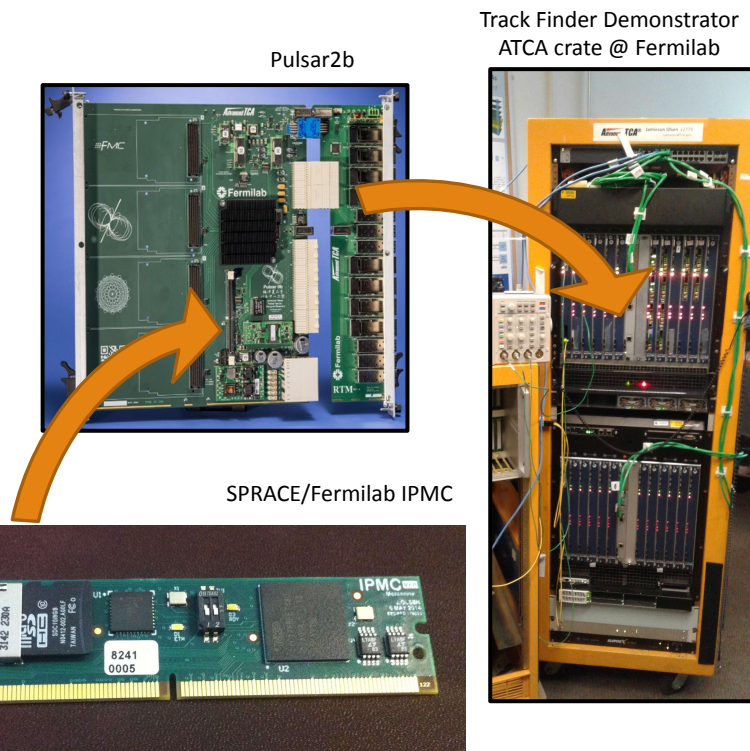
- Minimum set of required IPMI commands
 - Hot Swap and sensor readings
- Other Features (not IPMI/PICMG)
 - TCP/IP & Xilinx Virtual Cable (XVC) for FPGA debug

- **Rather rigid code base**

- **Hard coded variables**
- **Difficult to customize and port**
- **Single task** for all IPMI functions

- **Redesign from scratch for ZynqMP**

- Pulsar-2b IPMC was the inspiration
- Led to OpenIPMC



First target platform for ZynqMP development

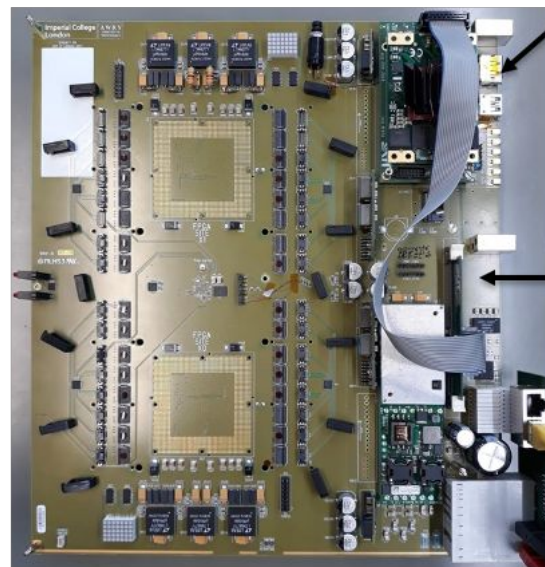
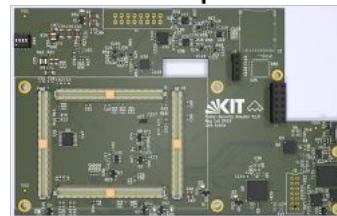
Trenz + Serenity setup (KIT)

- Serenity ATCA card (Imperial College)
- Trenez Elektronik TE0803 module
 - Zynq US+ ZU4EG SoC
- Trenez Adapter board (KIT)
 - Interface TE0803 to COM Express slot
 - Additional IPMC features
 - (I2C buffers, Eth Phy, EEPROM, SDCard...)
 - Interface to DIMM adapter
- DDR3 Mini-DIMM Adapter (KIT)
 - Fits into CERN IPMC-compatible slot
 - Access to IPMC backplane signals

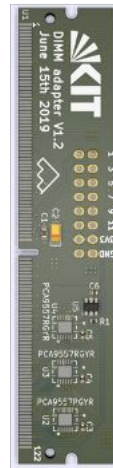
Trenz 0803



Trenz Adapter



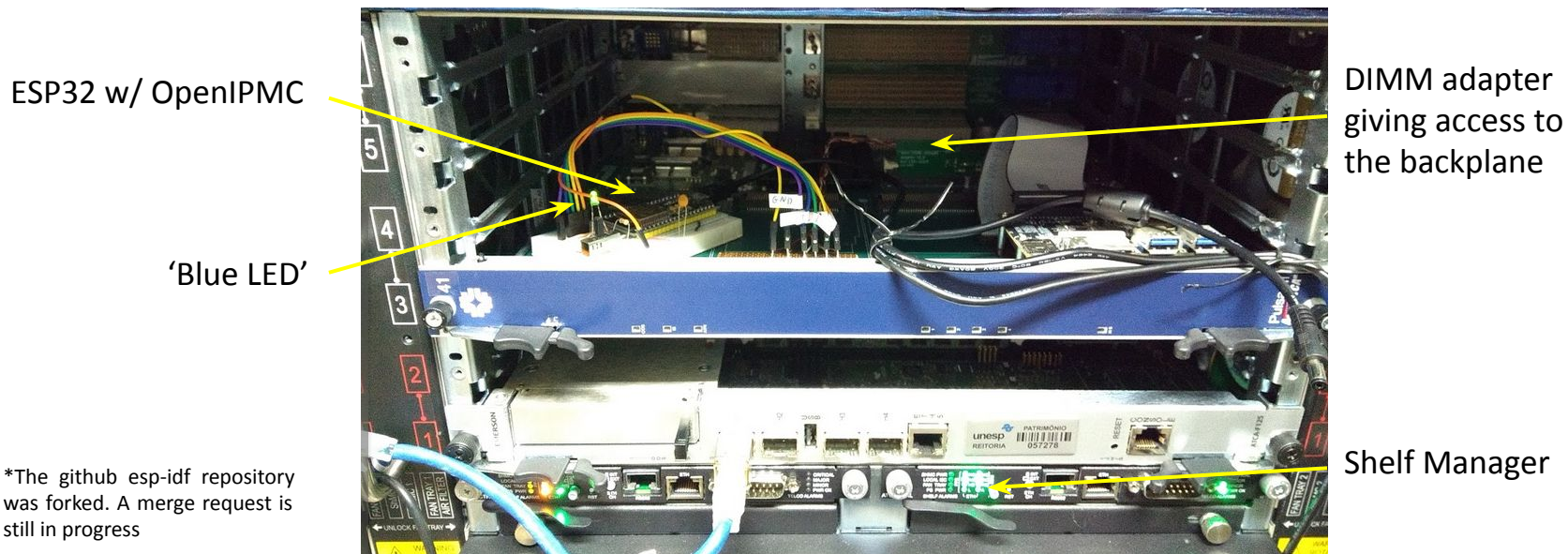
Serenity

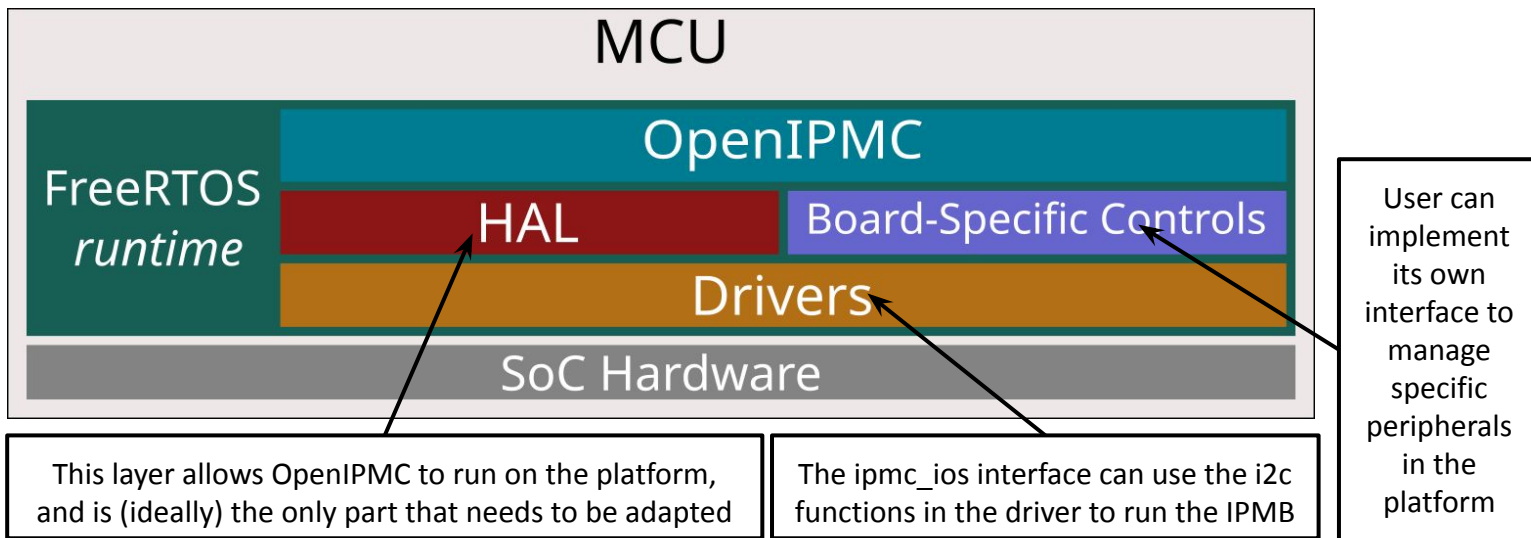


SO-DIMM adapter

Fixes to ESP32 Integrated Development Framework

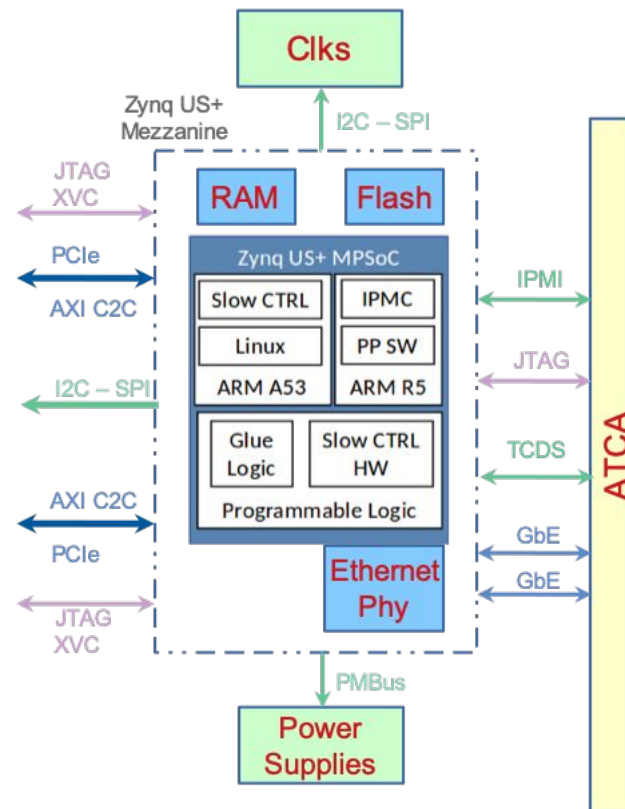
- I2C multi-master with variable size I2C msgs is required for IPMB bus communication
 - End of message is signalled by a stop bit
- The official esp-idf I2C driver was not supporting variable size msgs correctly
 - The driver expected a message size to be specified in advance
- We modified the driver* and now the slave read function correctly returns if receiving a stop bit





Xilinx ZynqMP SoC as unified mgmt module

- **Needs of ATCA boards for LHC experiments**
 - IPMC → board management & monitoring
 - Linux → higher-level functions (e.g. calibration)
 - Xilinx ZynqMP SoCs can satisfy both roles using one unit
- **Zynq Ultrascale+ MPSoC**
 - Two processor domains: Application PU and Real-time PU
 - Xilinx FPGA programmable logic (good 4 sys integration)
 - Plethora of peripherals (PCIe, ETH, I2C, UART, USB, ...)
- **Power domain partitioning**
 - Low PD (ARM-R5 RPU) → IPMC (standalone/RTOS)
 - Full PD (ARM-A53 APU) → Slow Control (Linux)
 - PL PD (FPGA) → partitioned between IPMC and Linux uses
- **Pros and cons of tighter IPMC/Linux integration**
 - Simple IPMC/Linux communication through mem registers
 - Very flexible implementation
 - Can be optimized for reduced board area occupation
 - Complex gymnastics between the two systems

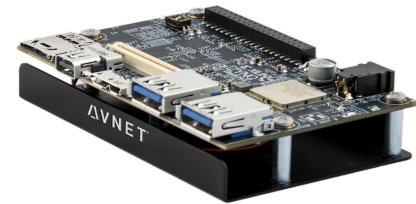
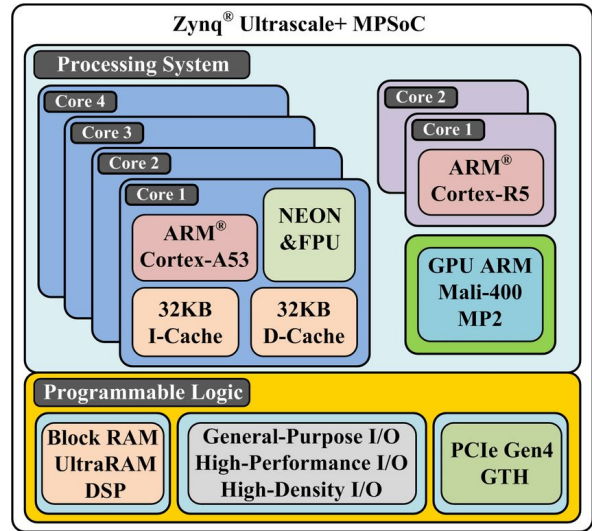


Architectures and boards that run OpenIPMC (so far)

1) Ultra96 + Pulsar-2b

Development platform for ZynqMP: Ultra96

- We began OpenIPMC on AVNET Ultra96
 - <https://www.96boards.org/product/ultra96/>
 - Plenty of tutorials & Vivado support
 - Excellent price (249\$) allows buying more boards
 - More boards can be used by developers
- Ultra96 uses Zynq Ultrascale+ ZU3EG
 - Same family as ZynqMP Mgmt. Module
 - APU → 4 x Cortex A-53
 - RPU → 2 x Cortex R-5
 - PL → Kintex US+ - like FPGA fabric



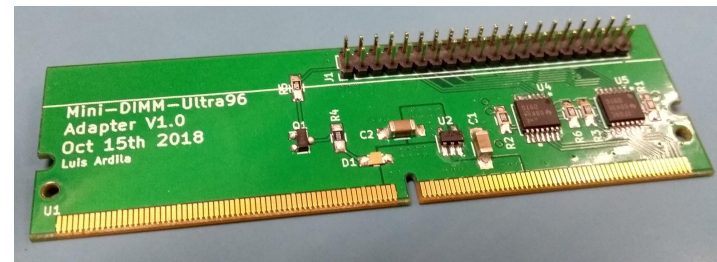
AVNET Ultra96 (Xilinx Zynq UltraScale+ ZU3EG)

Using generic development boards in the ATCA shelf

- Dev board (e.g. Ultra96)
 - Pulsar-2b board exposes signals to DIMM slot
 - IPMB-A and -B buses
 - Pulsar-2b LEDs
 - Pulsar-2b main power enable (not used so far)
 - Pulsar-2b local I2C for sensors (not used so far)
- Mini-DIMM adapter
 - Connects Pulsar-2b DIMM slot to Ultra96
 - Translates 1.8 V (Ultra96) ↔ 3.3V (ATCA)
 - Design and manufacture by Luis Ardila (KIT)
- Comtel CO6 ATCA chassis
 - Full-mesh, 6 slots horizontal
 - 2 PigeonPoint ShelfManagers (redundant)

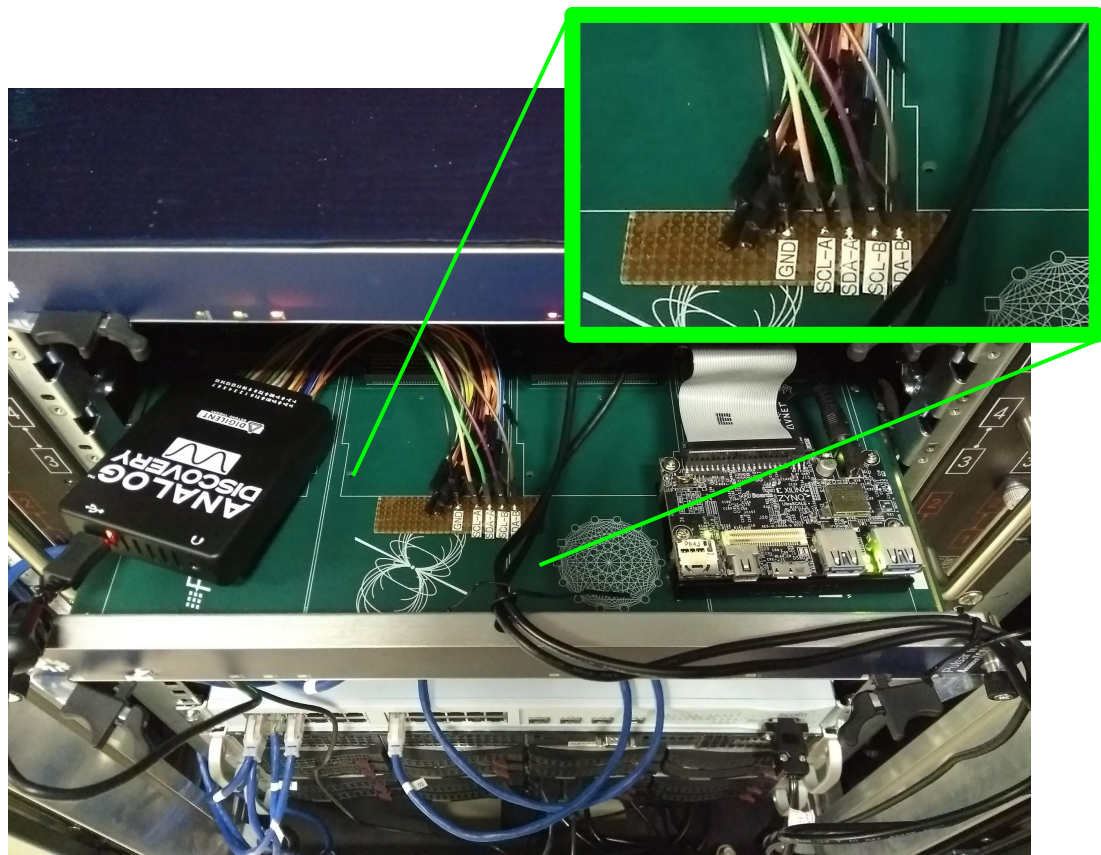


Ultra96 mated to the Pulsar-II through Mini-DIMM adapter



Mini-DIMM adapter

Ultra96 + Pulsar-2b in the shelf



Monitoring IPMB-A with TeK o'scope

Digilent Analog Discovery USB o'scope as I2C logic analyzer

2) Trenz module + Serenity

OpenIPMC tests on Trenz + Serenity setup @ KIT

- From Ultra96, OpenIPMC code was successfully ported to **Trenz+Serenity** setup at KIT
 - Adapting HAL and Board-specific ctrls
 - All changes in one file
- All changes relays into the `ipmc_ios.c` file
- Hot-Swap operation successfully tested on Serenity board
- Since no real sensor are currently being read in this hardware



Trenz-Serenity setup at KIT

OpenIPMC tests on Trenz + Serenity setup @ KIT

Activation Status

```
# clia fru -v 96

Pigeon Point Shelf Manager Command Line Interpreter

96: FRU # 0
  Entity: (0xb0, 0x1)
  Hot Swap State: M4 (Active), Previous: M3 (Activation In Process), Last State Change Cause: Normal State Change (0x0)
  Device ID String: "Trenz-Serenity"
  Site Type: 0x00, Site Number: 02
  Current Power Level: 0x02, Maximum Power Level: 0x02, Current Power Allocation: 100.0 Watts
```

FRU Information (testing data from example code)

```
# clia fruinfo 96 0

Pigeon Point Shelf Manager Command Line Interpreter

96: FRU # 0, FRU Info
Common Header:   Format Version = 1

Board Info Area:
  Version       = 1
  Language Code = 25
  Mfg Date/Time = Oct  1 00:00:00 2019 (12490560 minutes since 1996)
  Board Manufacturer = SPRACE - KIT
  Board Product Name = OpenIPMC @ Trenz-Serenity
  Board Serial Number = 189189981-18998
  Board Part Number  = AA00Y99
  FRU Programmer File ID = 01
```

Sensor Reading (testing data from example code)

```
# clia sensordata 96 3

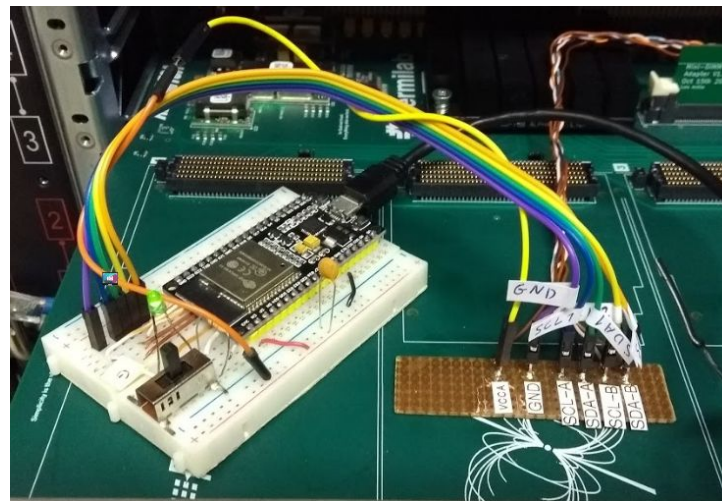
Pigeon Point Shelf Manager Command Line Interpreter

96: LUN: 0, Sensor # 3 ("FPGA TEMP")
  Type: Threshold (0x01), "Temperature" (0x01)
  Belongs to entity (0xa0, 0x60)
  Status: 0xc0
    All event messages enabled from this sensor
    Sensor scanning enabled
    Initial update completed
  Raw data: 50 (0x32)
  Processed data: 50.000000 degrees C
  Current State Mask: 0x00
```

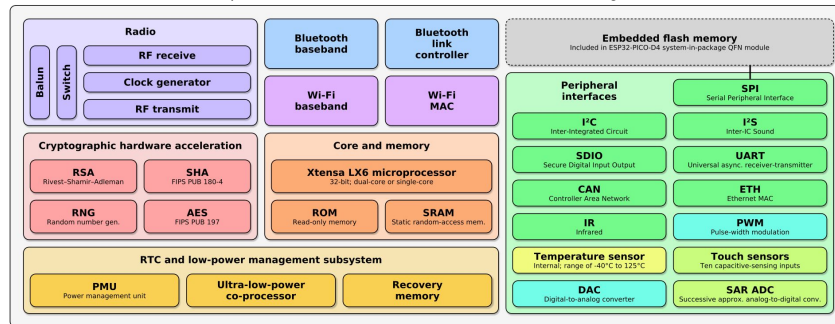
3) ESP32 + Pulsar-2B

Porting OpenIPMC to ESP32

- ESP32 microcontroller (see backup slides)
 - Very different from a Zynq US+
- Questions answered by this exercise
 - Architecture independency
 - Trivial, thanks to C and FreeRTOS
 - Ease of integration on a different SoC
 - OpenIPMC needs I2C peripheral
 - Many SoCs have 2 or more
 - Effort needed to port OpenIPMC
 - Mainly IO/HAL interface bindings
 - Fixes needed in ESP32 IDF (see backup)
 - Porting took just 3 person-weeks :-)
- Overall the exercise was a success
- Repo: gitlab.com/openipmc/ipmc-esp32



Espressif ESP32 Wi-Fi & Bluetooth Microcontroller – Function Block Diagram



OpenIPMC tests on ESP32

- IPMBus communication works
- ShM happily accepts the FRU
- Activation/deactivation are triggered using an 'improvised' Handle Switch
- Activation time significantly longer than in Ultra96
 - Likely due to ESP32 drivers

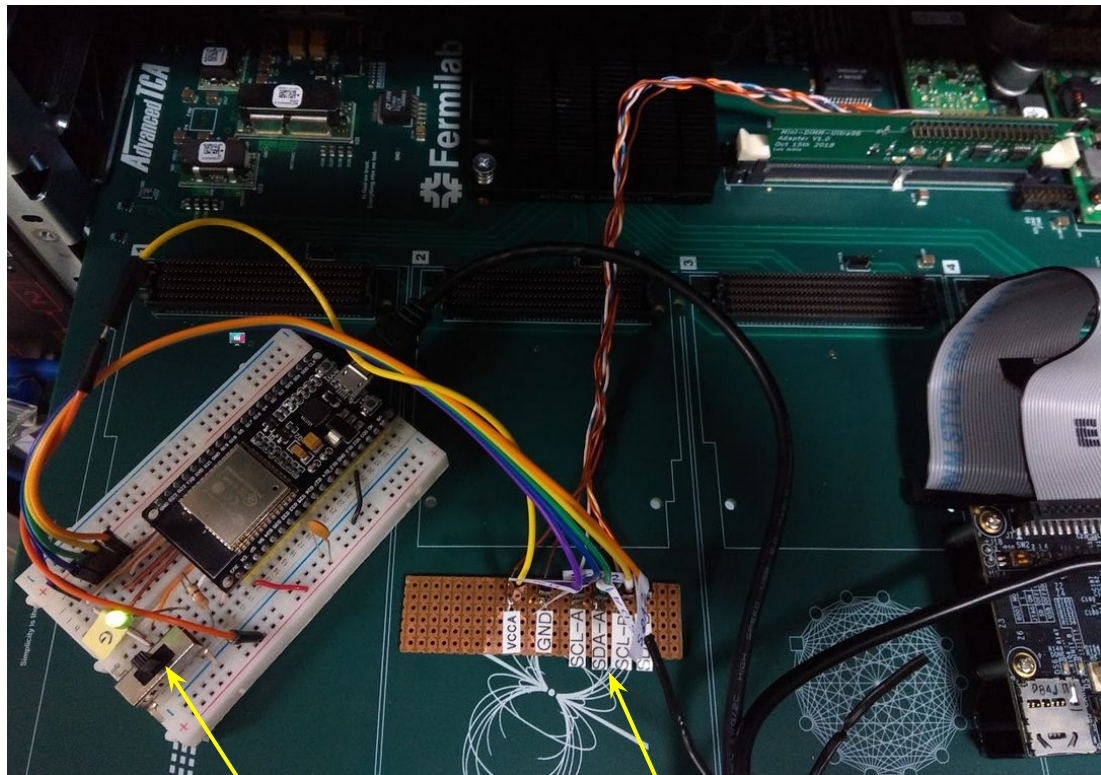
```
86: LUN: 0, Sensor # 4 ("AIR TEMP")
Type: Threshold (0x01), "Temperature" (0x01)
Belongs to entity (0xb0, 0x60)
Status: 0xc0
  All event messages enabled from this sensor
  Sensor scanning enabled
  Initial update completed
Raw data: 32 (0x20)
Processed data: 32.000000 degrees C
Current State Mask: 0x00

86: LUN: 0, Sensor # 5 ("VCC1V0 VOUT")
Type: Threshold (0x01), "Voltage" (0x02)
Belongs to entity (0xb0, 0x60)
Status: 0xc0
  All event messages enabled from this sensor
  Sensor scanning enabled
  Initial update completed
Raw data: 22 (0x16)
Processed data: 0.345400 Volts
Current State Mask: 0x00

# clia fru 86

Pigeon Point Shelf Manager Command Line Interpreter

86: FRU # 0
Entity: (0x0, 0x0)
Hot Swap State: M1 (Inactive), Previous: M6 (Deactivation In Progress)
Device ID String: " "
```



'Handle Switch' for tests

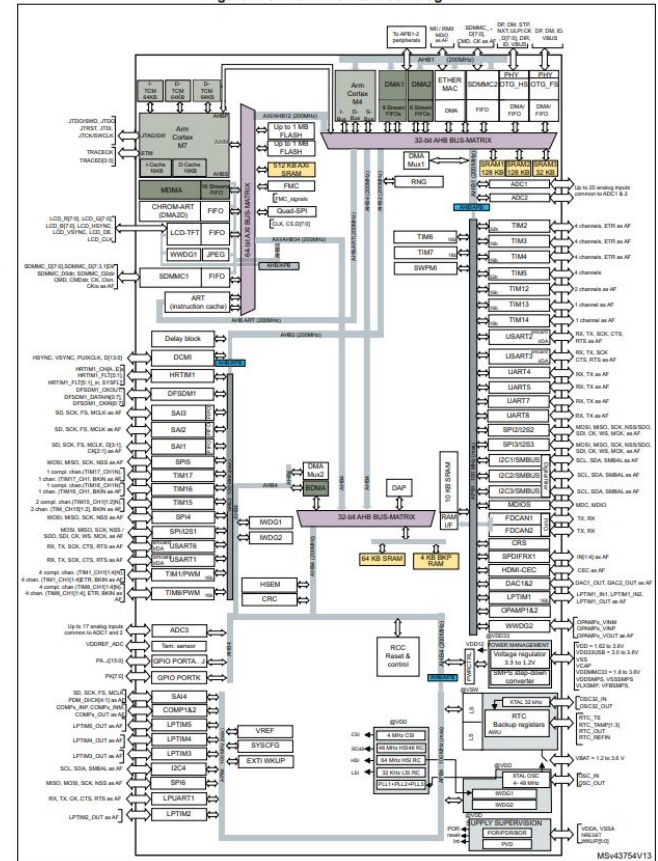
I2C lines connected to DIMM

4) STM32 H745 + Pulsar-2B

ST Microelectronics STM32H745

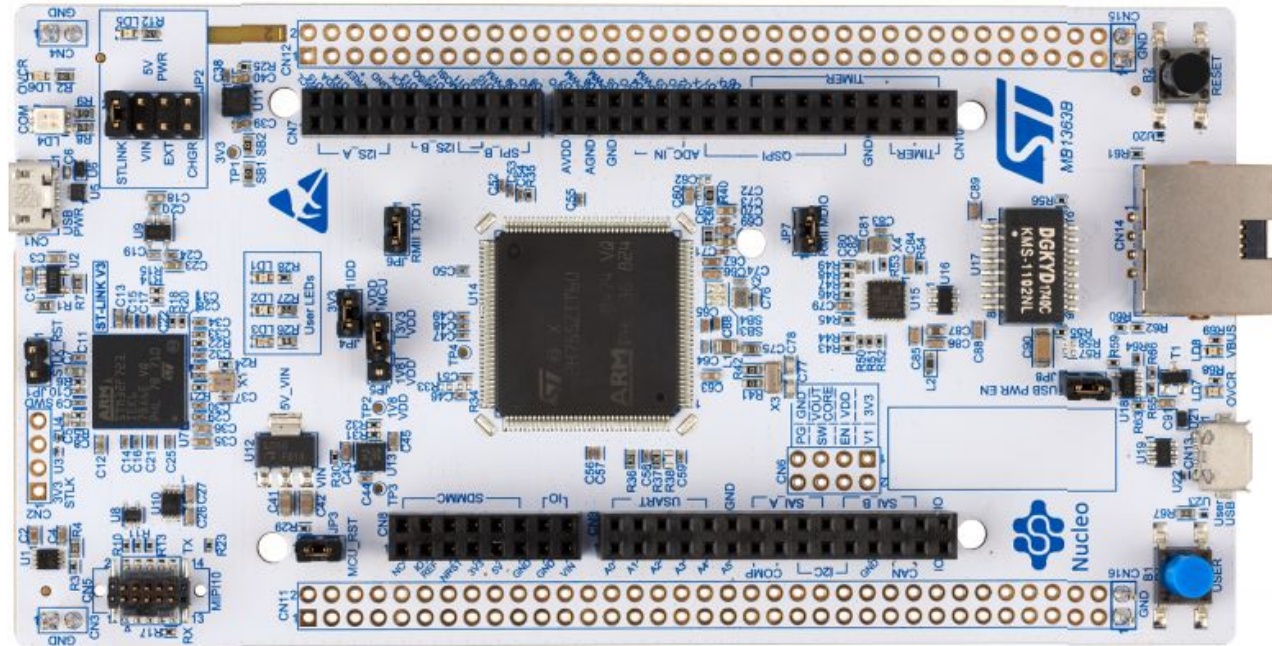
- **Powerful industrial control-oriented MCU**
 - 480 MHz ARM Cortex-M7 main CPU
 - 240 MHz ARM Cortex-M4 aux CPU
- **Plenty of peripherals**
 - 4 x hardware I2C, 6 x hardware SPI
 - 4 USART + 4 UART + 1 LPUART
 - Up to 168 GPIO
- **Moderate current consumption**
 - 600 mA absolute max / 80-200 mA typ current
- **Free development environment & compiler**
 - STM32CubeIDE (gcc in the back-end)
 - Compatible with Linux, OpenOCD and GDB
 - **ST provides a FreeRTOS distribution for STM32**

Figure 1. STM32H745x/G block diagram



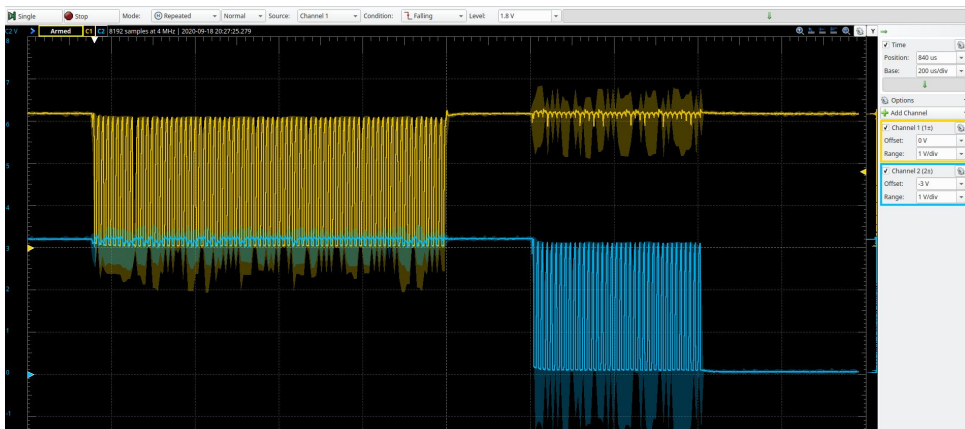
ST Microelectronics NUCLEO

- For development we use the ST [NUCLEO-H745ZI-Q](#) devboard
 - STM32H745 in LQFP-144 package (same silicon, less pins than the TFBGA-240+25)
 - Easy to get from distributors and CERN stores, cheap (around 23 CHF)

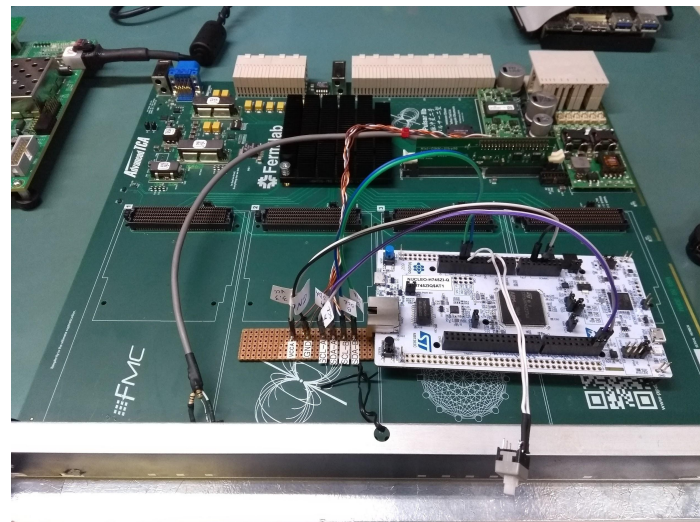


Porting OpenIPMC to STM32

- Porting was similar to ZYNQ and ESP32, thanks to FreeRTOS being supported on STM32
 - We wrote a new OpenIPMC HAL to interface with the STM32 drivers
- Porting OpenIPMC core functions (IPMB-0) took just 4 person-weeks
 - Usual show-stopper was the I2C driver implementation of I2C multi-master mode
 - Relatively painless fix, similar to the Zynq case
- Testing: IPMI communication works properly on STM32



STM32 responding to shelf manager with 200 μ s latency (timeout **300 ms**)



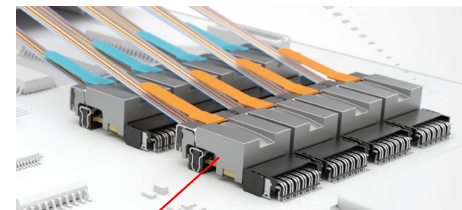
NUCLEO board mounted onto the Pulsar-2b

5) Serenity-A2577 + ZynqMP Mezzanine

OpenIPMC Ported to the ZynqMP R5 Cores



SAMTEC Firefly Optics



- FMC+ management module with ZynqUS+ device
- OpenIPMC ported to the R5 cores
- CentOS 7 based root filesystem + petalinux kernel runs on the A53 cores
- Upstream OpenIPMC software in use via submodule in the Zynq R5 firmware framework.
- new PIM400 sensors working



Board Management Mezzanine

