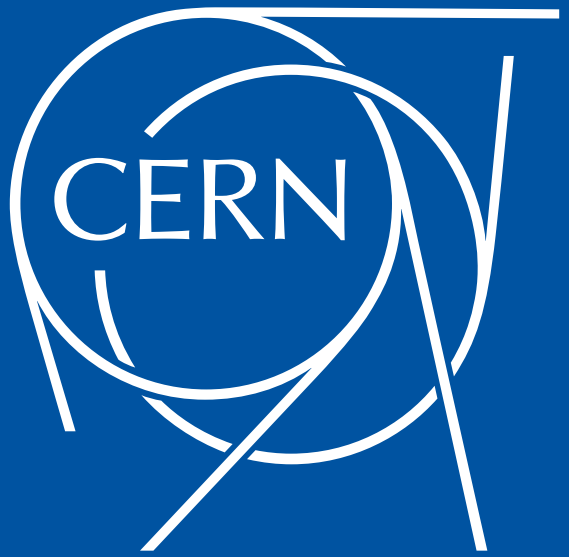

CERN

# Programming Switches for Flow Label Accounting and Routing

CERN Data Center
IT-CS-CE Department

Carmen Misa Moreira
Edoardo Martelli

# Introduction

- Programming Protocol-independent Packet Processors
- EdgeCore Wedge100BF-32QS

# Programming Protocol-independent Packet Processors: P4 language

Language for programming the data plane of network devices

- Define how packets are processed
- P4 program structure: header types, parser/deparser, match-action tables, user-defined metadata and intrinsic metadata

Domain-specific language designed to be implementable on a large variety of targets

- Programmable network interface cards, FPGAs, software switches and hardware ASICs.

# EdgeCore Wedge100BF-32QS

- 100GbE Data Center Switch
  - Bare-Metal Hardware
  - L2/L3 Switching
  - 32xQSFP28 Ports
- Data-Plane Programmability
  - Intel Tofino Switch Silicon
  - Barefoot Networks
- Quad-Pipe Programmable Packet Processing Pipeline
  - 6.4 Tbps Total Bandwidth
- CPU: Intelx86 Xeon 2.0GHz
  - 8-core/48GB/2TB SSD

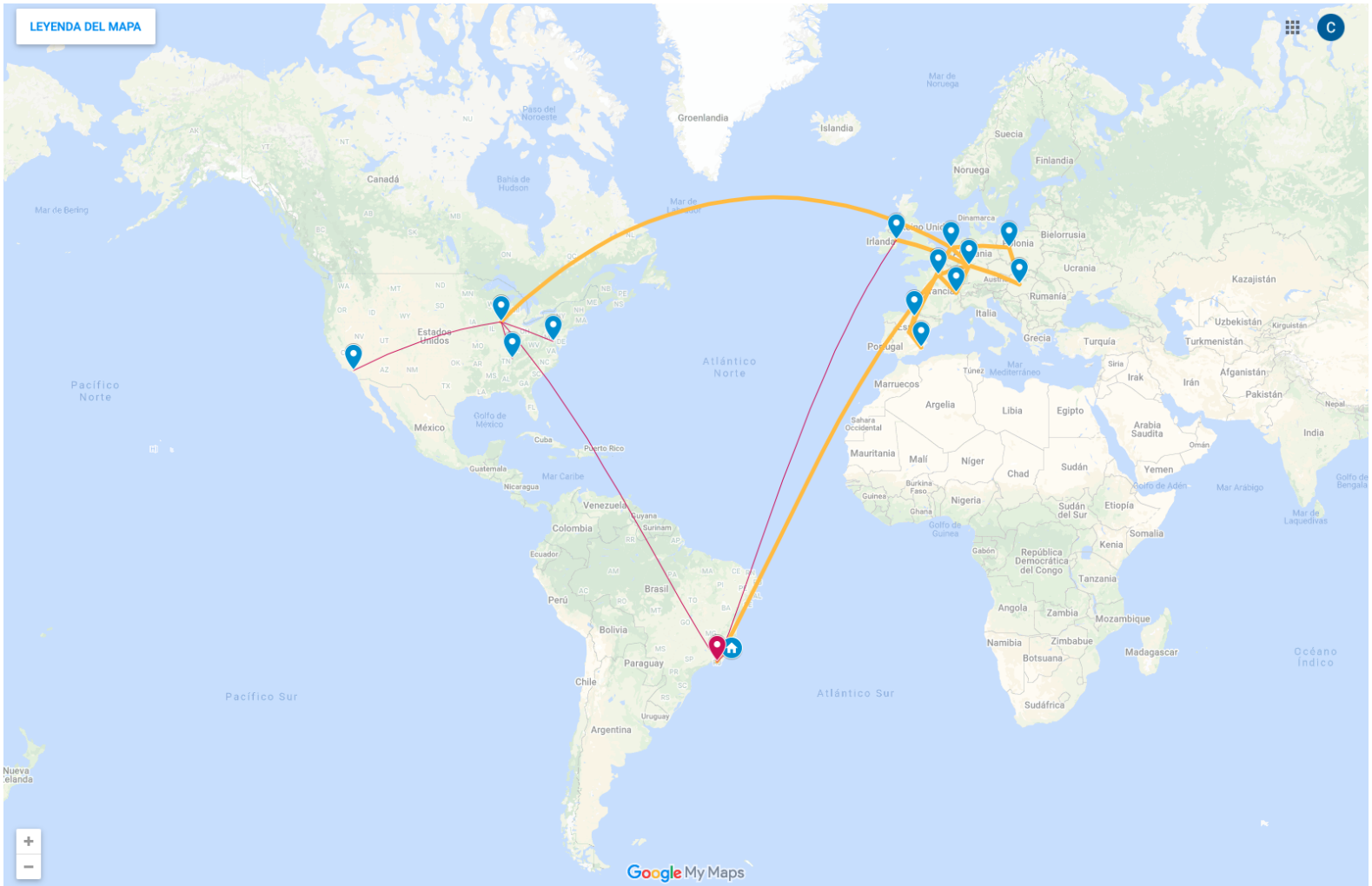

Figure: Intel Tofino P4-programmable Ethernet Switch ASIC

Figure: EdgeCore Wedge100BF-32QS

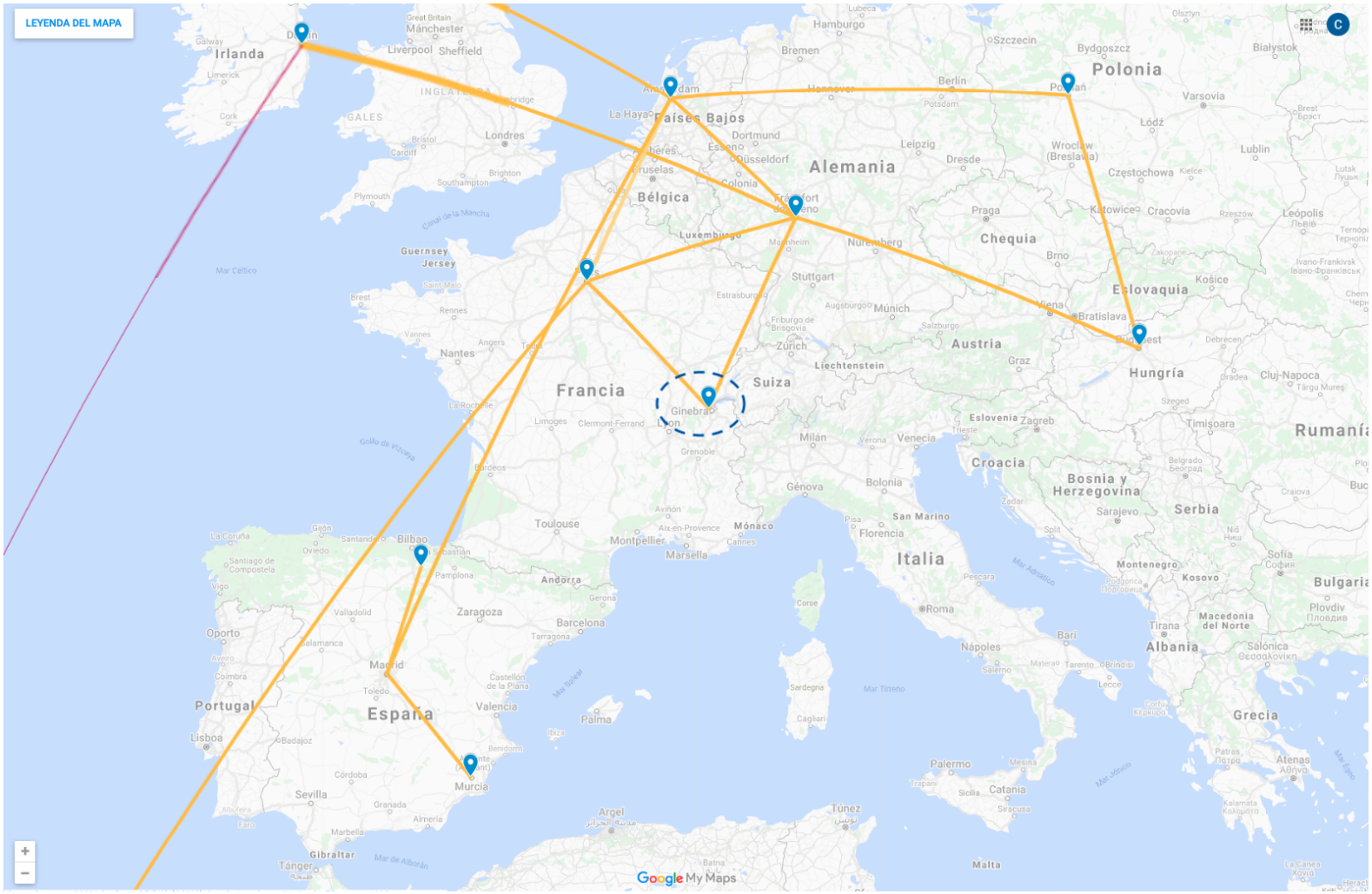
# On-going project

- GÉANT P4 Network
- Network Operating System
- Policy Routing
- Simple Network Management Protocol
- Problems Found and Tips

# GÉANT P4 Network



# GÉANT P4 Network



# Network Operating System

## RARE/FreeRtr

- Controls the data plane by managing entries in routing tables
- Free and open source router operating system
- Export forwarding tables to DPDK or hardware switches
  - via OpenFlow or P4lang
- No global routing table
  - Every routed interface must be in a virtual routing table


# Policy Routing

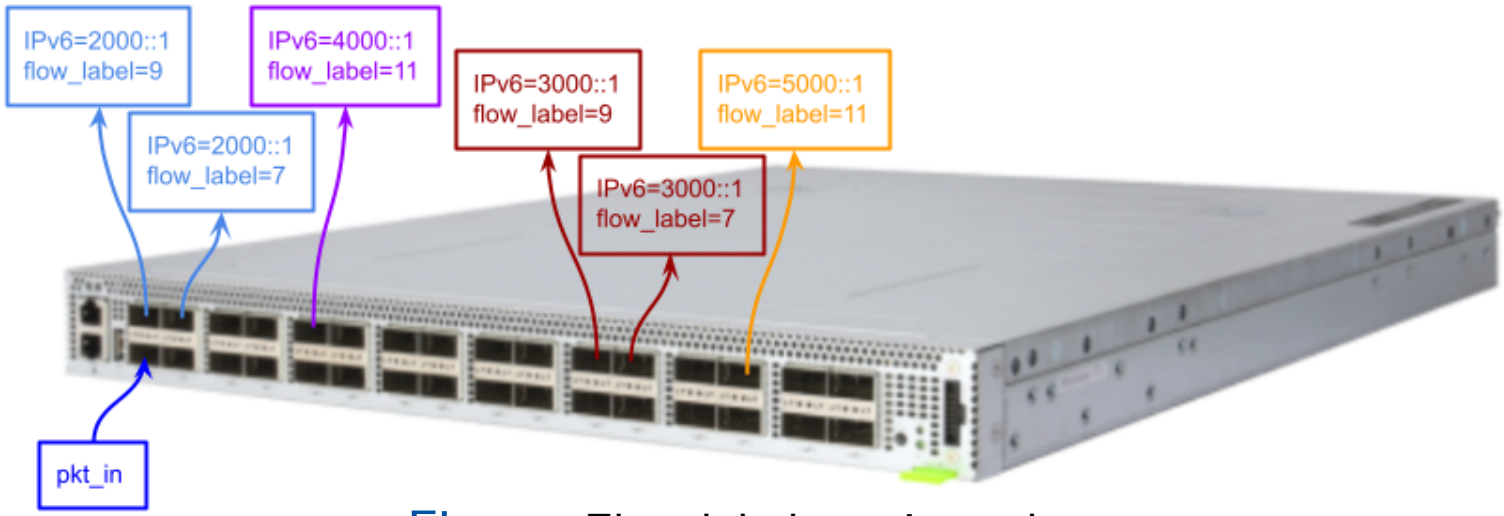


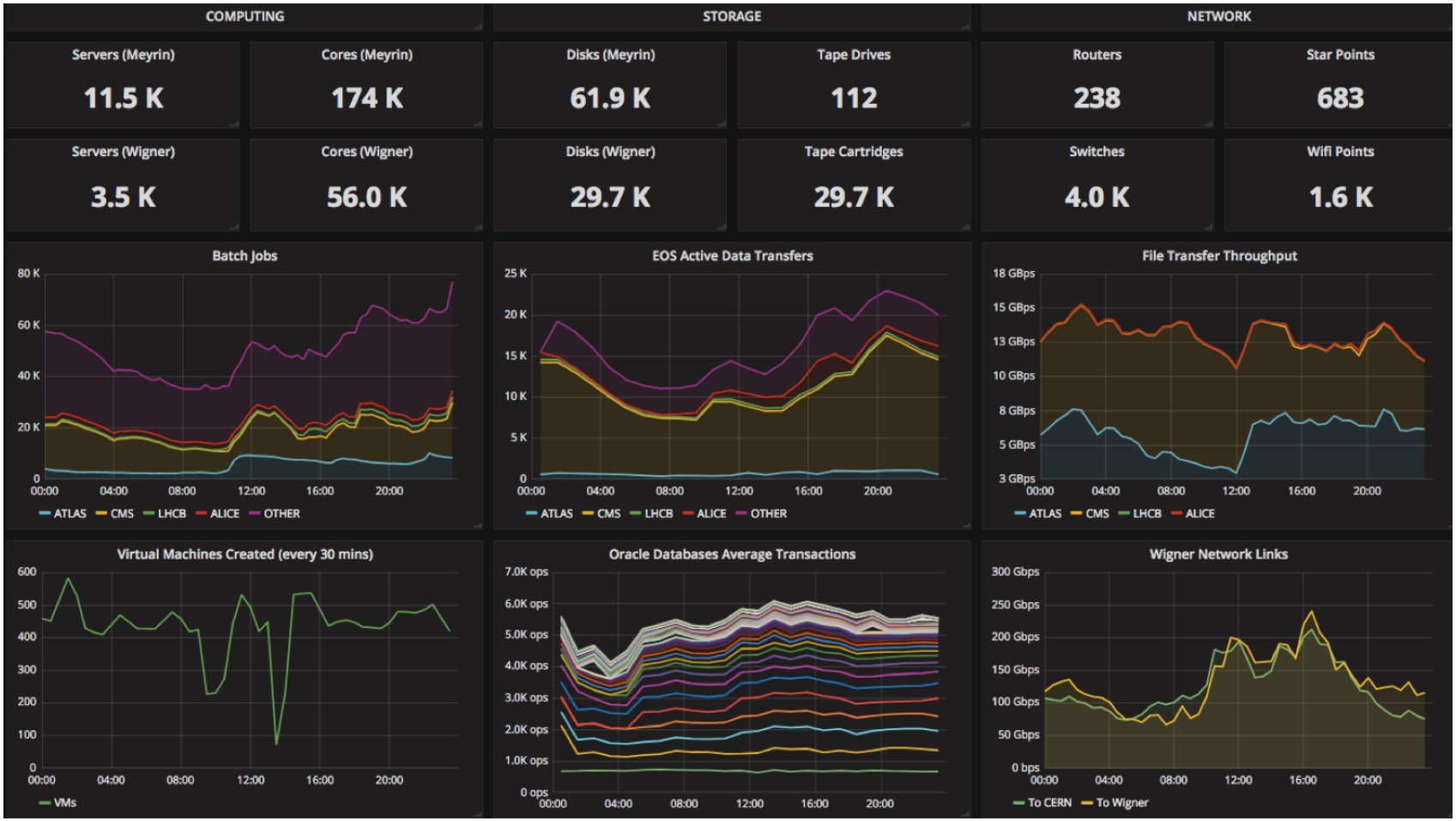

Figure: Flow label routing scheme

Table: Statistics per link

| Port | IPv6 | Flow Label | Number of pkts | Number of bytes |
|---|---|---|---|---|
| 1 | normal traffic | N/A | 4 | 416 |
| 1 | 2000::1 | 9 | 3 | 342 |
| 2 | 2000::1 | 11 | 2 | 288 |
| 3 | 2000::1 | 13 | 1 | 134 |
| 4 | 3000::1 | 9 | 2 | 288 |
| 5 | 3000::1 | 11 | 1 | 134 |
| 6 | 3000::1 | 13 | 3 | 342 |

# Simple Network Management Protocol

## [TO-DO list]



# Problems Found and Tips

- Lack of knowledge in Tofino Native Architecture
  - Unless you attend Intel Connectivity Academy
  - Sign NDA and get access to P4 Studio
- Steep learning curve and development
  - Data plane needs to be implemented: P4 program
  - Control plane needs to be implemented: routing tables
  - New technology $\rightarrow$ still under research and development
- Due to pandemic there is a lack of resources
  - The only switch under stock was EdgeCore Wedge100BF-32QS but... there is none NOS available!
    - Solution: RARE/freeRtr

# Acknowledgements


Frederic Loui
RARE Technical Leader
https://www.rare.freertr.net
https://docs.freertr.net
https://blog.freertr.net

Csaba Mate
RARE/freeRtr Lead Core Developer
https://freertr.net

Alexander Gall
https://github.com/alexandergall/bf-sde-nixpkgs
https://github.com/alexandergall/packet-broker

Ronald van der Pol





# Thanks for your attention!

# Programming Switches for Flow Label Accounting and Routing

CERN Data Center
IT-CS-CE Department

Carmen Misa Moreira
Edoardo Martelli


CERN