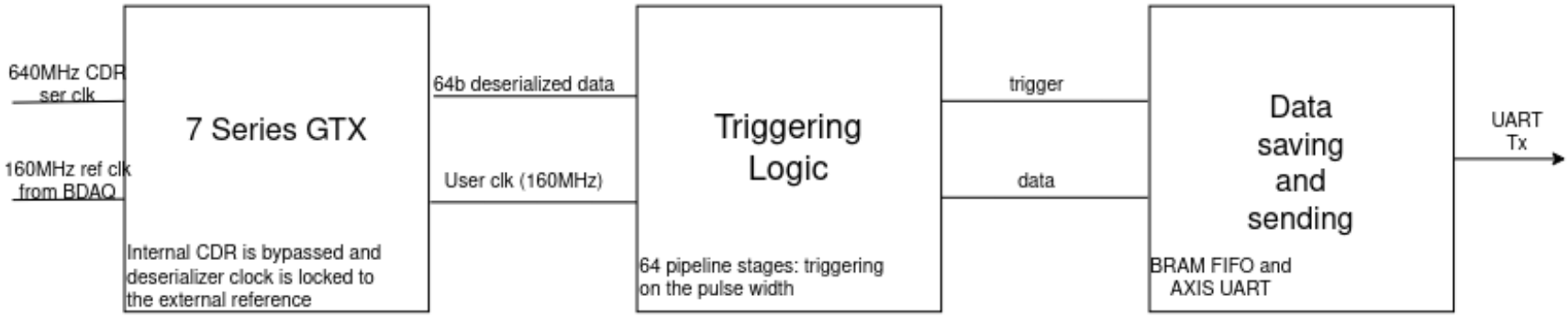
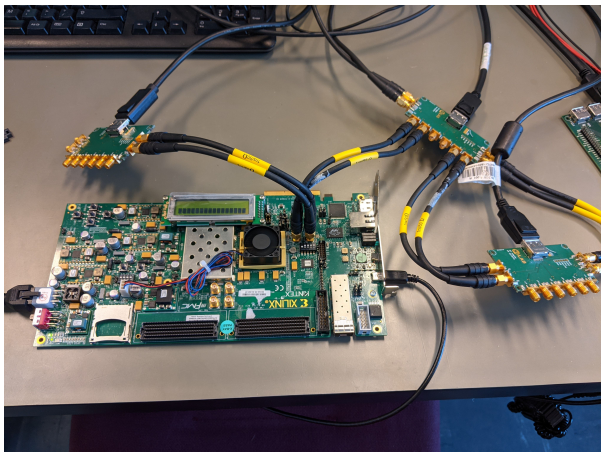
SEE Preliminary Results Campaign in GANIL

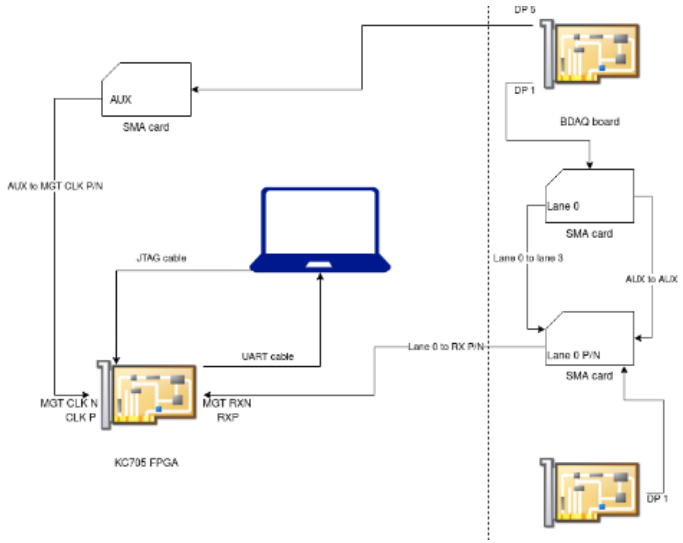
M. Menouni, P. Rymaszewski, D. Fougeron, P. Barrillon, T. Strebler
E. Madsen, L. Flores, J.Lalic

KC705 setup

Clock oversampling with 7 Series Xilinx GTX







10.24Gb/s Oversampling

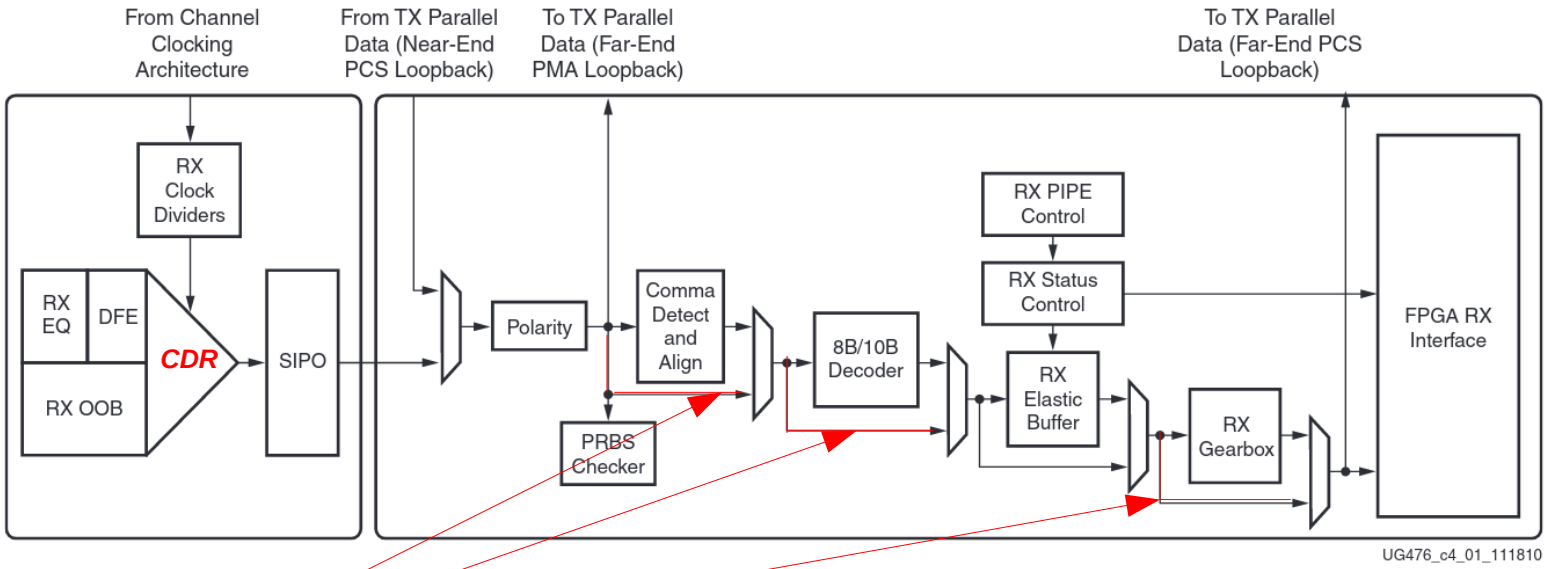


Figure 4-1: **GTX/GTH Transceiver RX Block Diagram**

Bypassing

CDR in 'Lock to reference' mode

RXCDRHOLD = 1'b1
RXCDROVRDEN = 1'b0
Keep CDR locked to reference clock (not locking to incoming data)

Reference clock – 160MHz provided by BDAQ board (needs to be low jitter clock, great impact on the transmitter performance)

Setup developed on KC705 board:

- Kintex-7 XC7K325-2
- Max line rate for GTX: 10.3125Gps
- Rate used for oversampling: 10.24Gb/s => sampling resolution = >97.65625 ps
- Oversampling the 640MHz clock: 16 bits per clock cycle

10.24Gb/s Oversampling

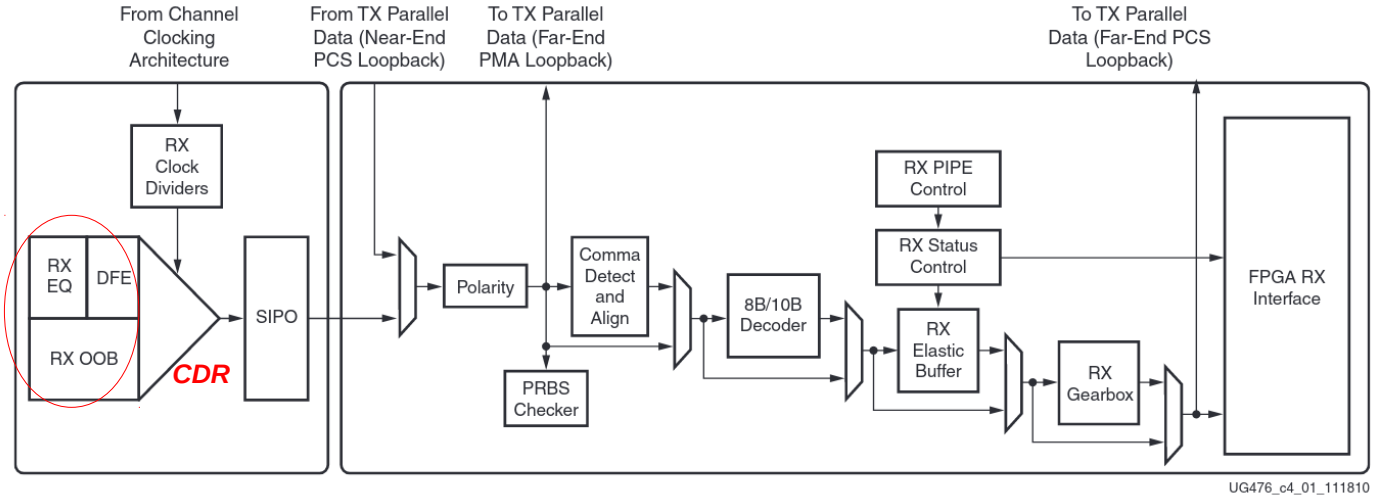


Figure 4-1: **GTX/GTH Transceiver RX Block Diagram**

There are 2 possible Use Modes:

1. DFE (default): A discrete-time adaptive high-pass filter. Uses the auto adapting methods (baseline wander cancellation) to equalize the effects of the channel.
2. LPM mode: Used for final setup (disabled auto-adaptive equalizer)

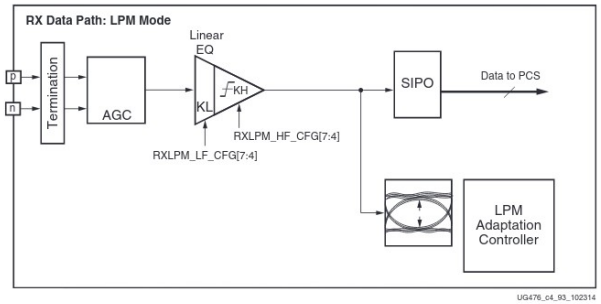
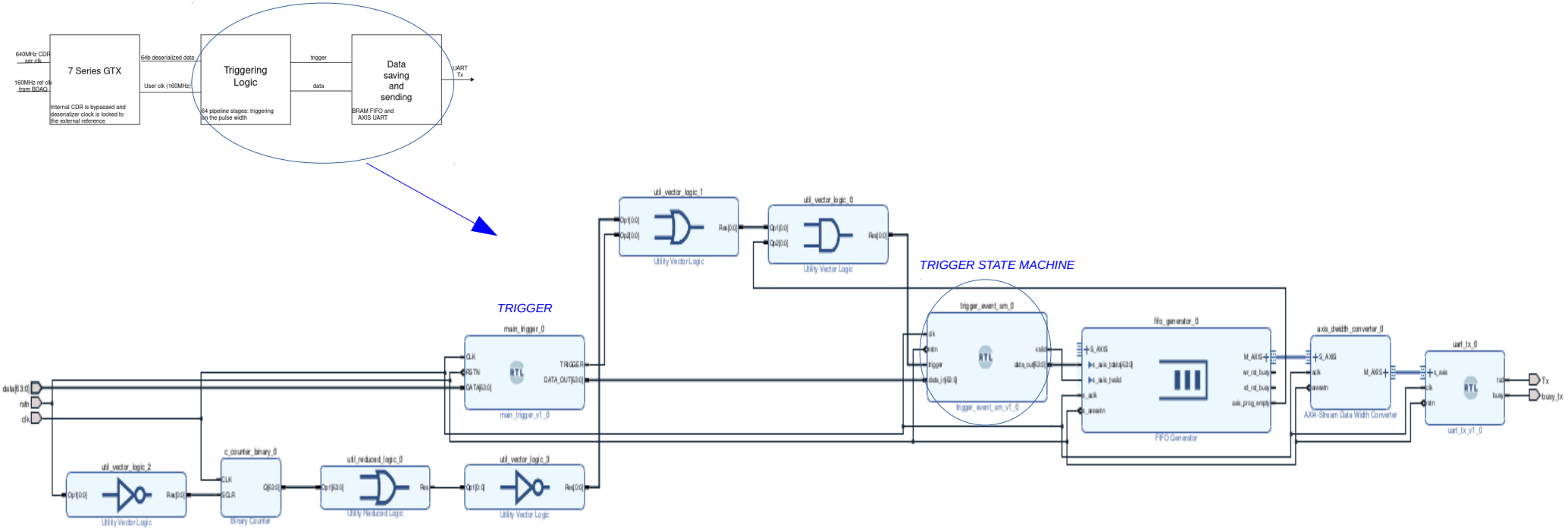


Figure 4-17: **LPM Mode**

GTX as an oversampler:

- LPM mode
- No decoding
- Internal data width 32, external data width 64 (word frequency is 160MHz)
- RX Elastic Buffer enabled
- Bypassing Comma detect, 8b/10b Decode and RX Gearbox blocks
- Common mode set to 1100mV

KC705 setup: Readout



Trigger Event:
“commaStart_timestamp_20usOversampledClk_commaStop”

KC705 setup: Readout

Readout system characteristics:

- Maximum constant trigger rate 2events/sec
- Distribution of events doesn't matter (no dead time after events)

GANIL:

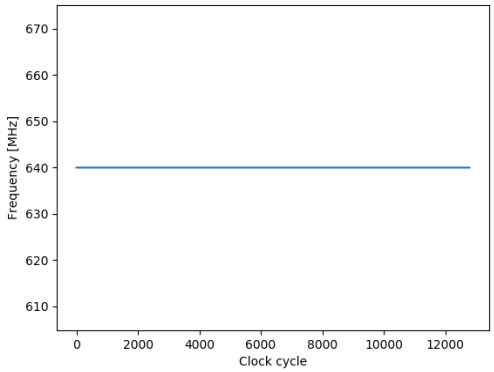
No lost trigger events due to event cross-section!

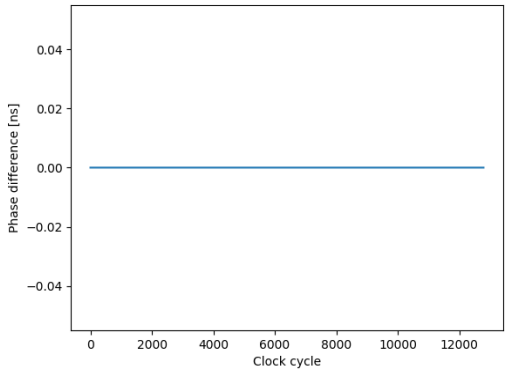
Important: System triggers on freq jump => less sensitive than scope even though it has better resolution

Less trigger events in comparison to scope

After every 1min the "false trigger" is generated (to be sure the communication was functional during the beam in case there are no real triggers in a specific time interval – useful in post-analysis)

Phase and frequency measurement of the "false trigger":





GANIL SEE testing: Overview

ITkPixV1.1 chip used

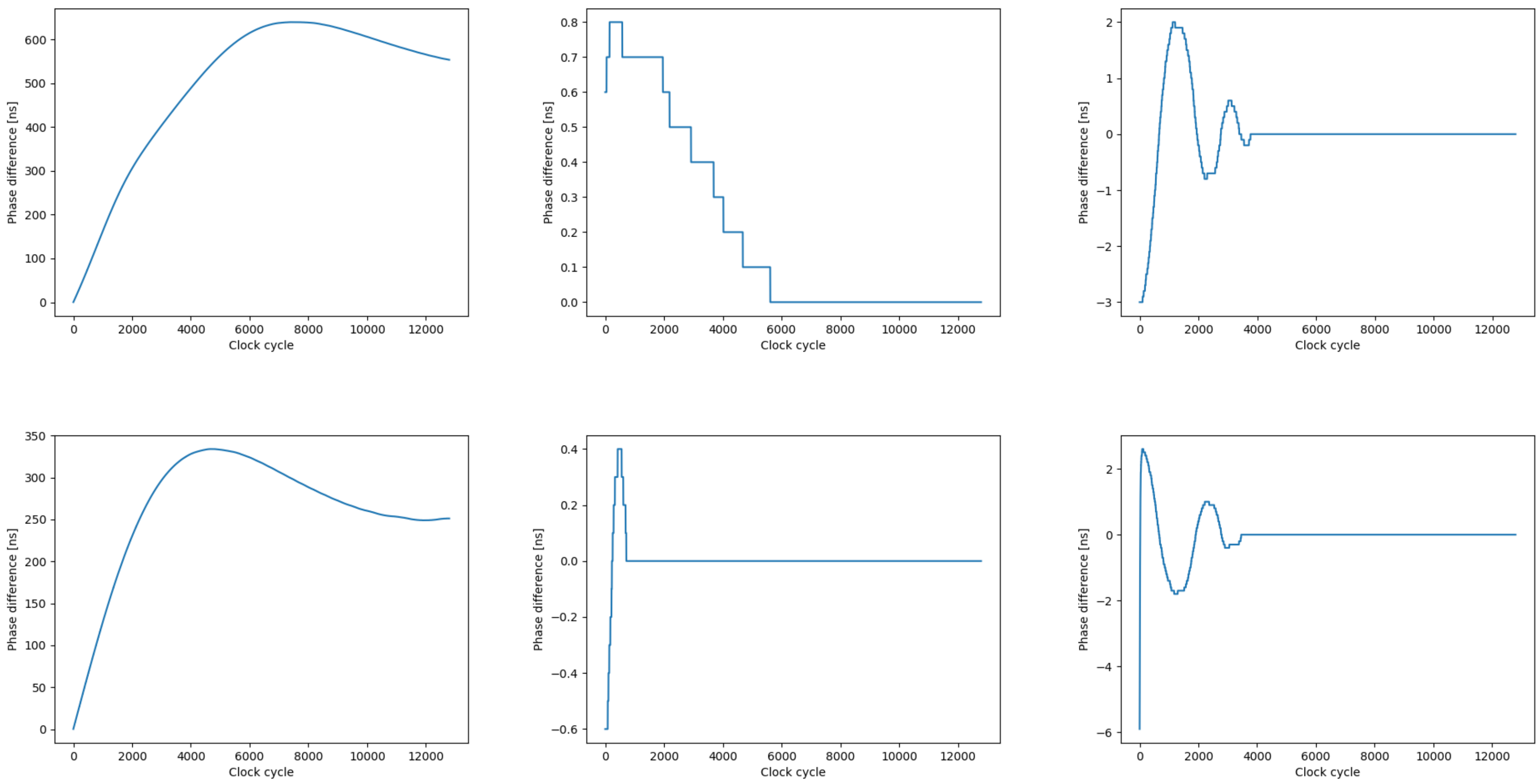
All trigger events classified into "RUN" depending on Flux and running mode!

RUN(PLL Mode@1.28Gbit/s)	Flux [p/cm^2/s]	Time [s]
501	1242	419
502	952	461
503	400	1049
504	640	741

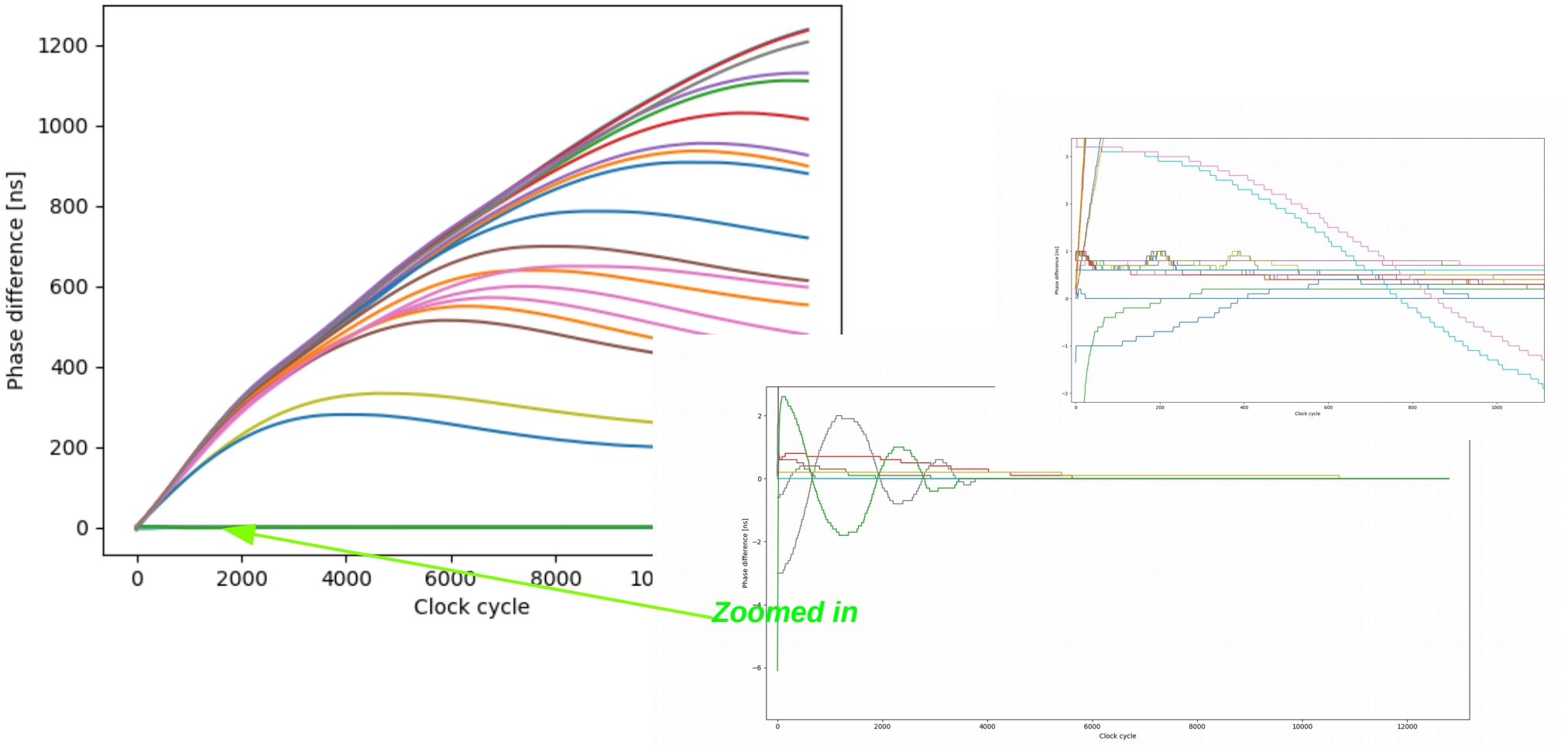
RUN	Flux [p/cm^2/s]	Time [s]
505: Bypass mode@640 MHz	291	2061
506: PLL Mode@1.28Gbit/s	147	4083

RUN 504: Phase measurements

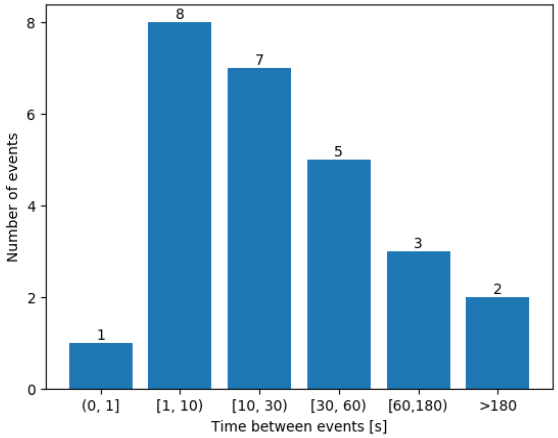
Some characteristic trigger events:

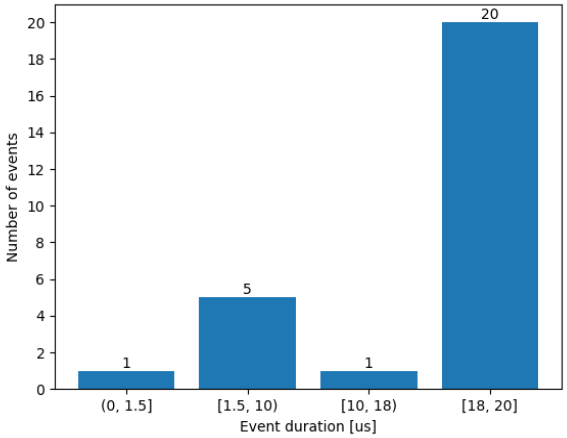


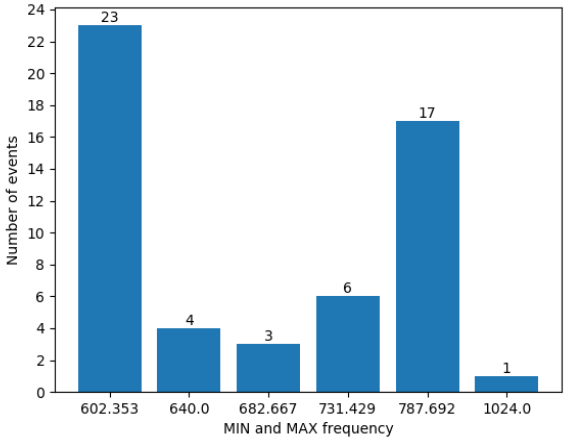
RUN 504: All trigger events

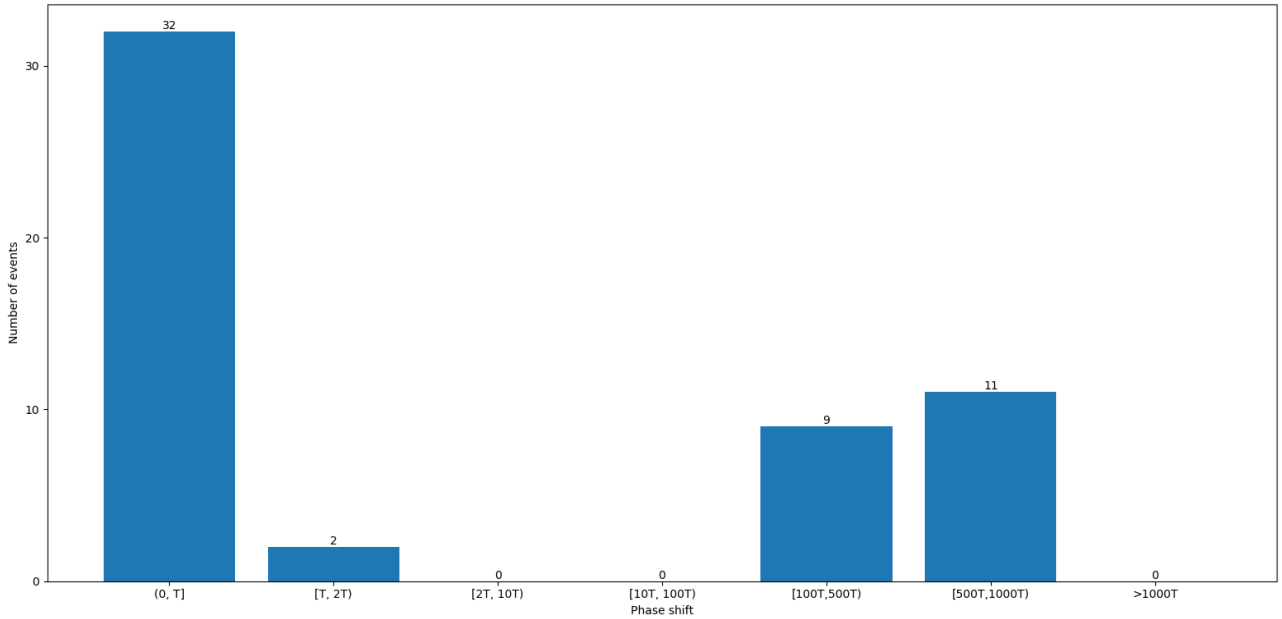


RUN 504: Phase measurements



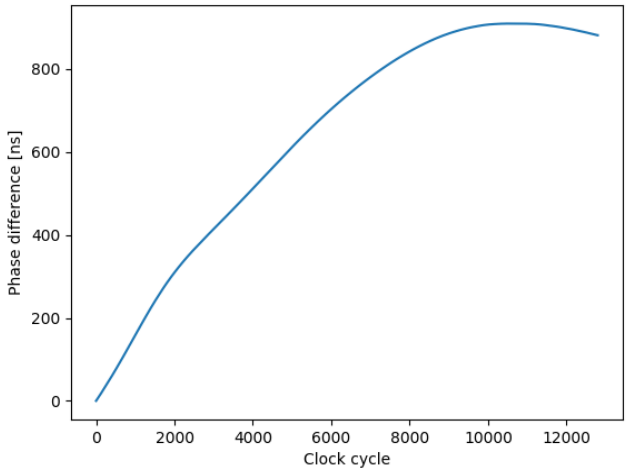


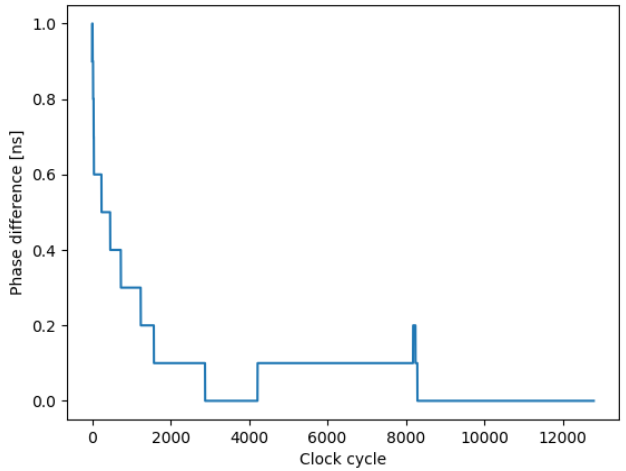


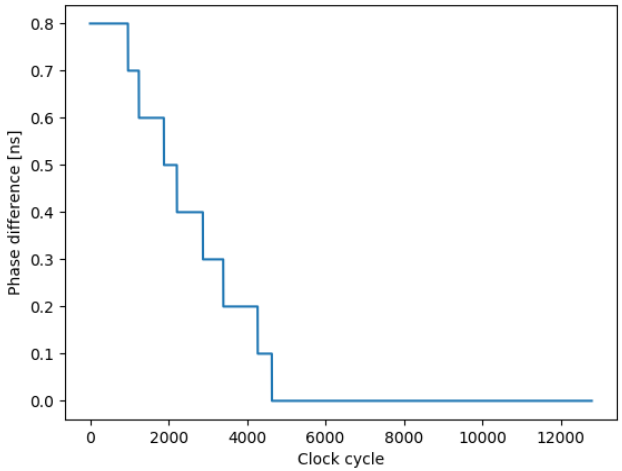


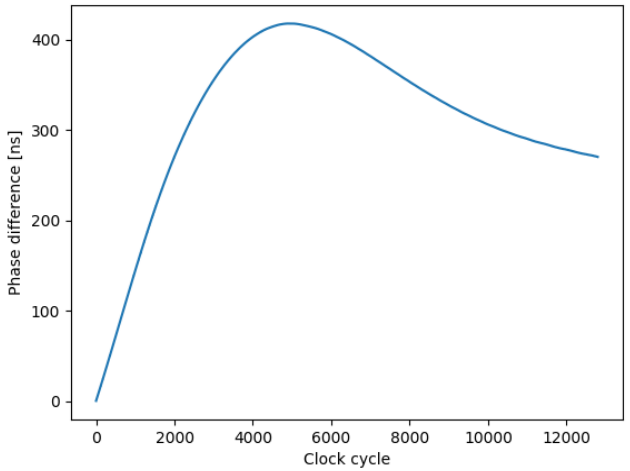
One trigger even makes 2 inputs: min and max value during the event

RUN 503: Phase measurements

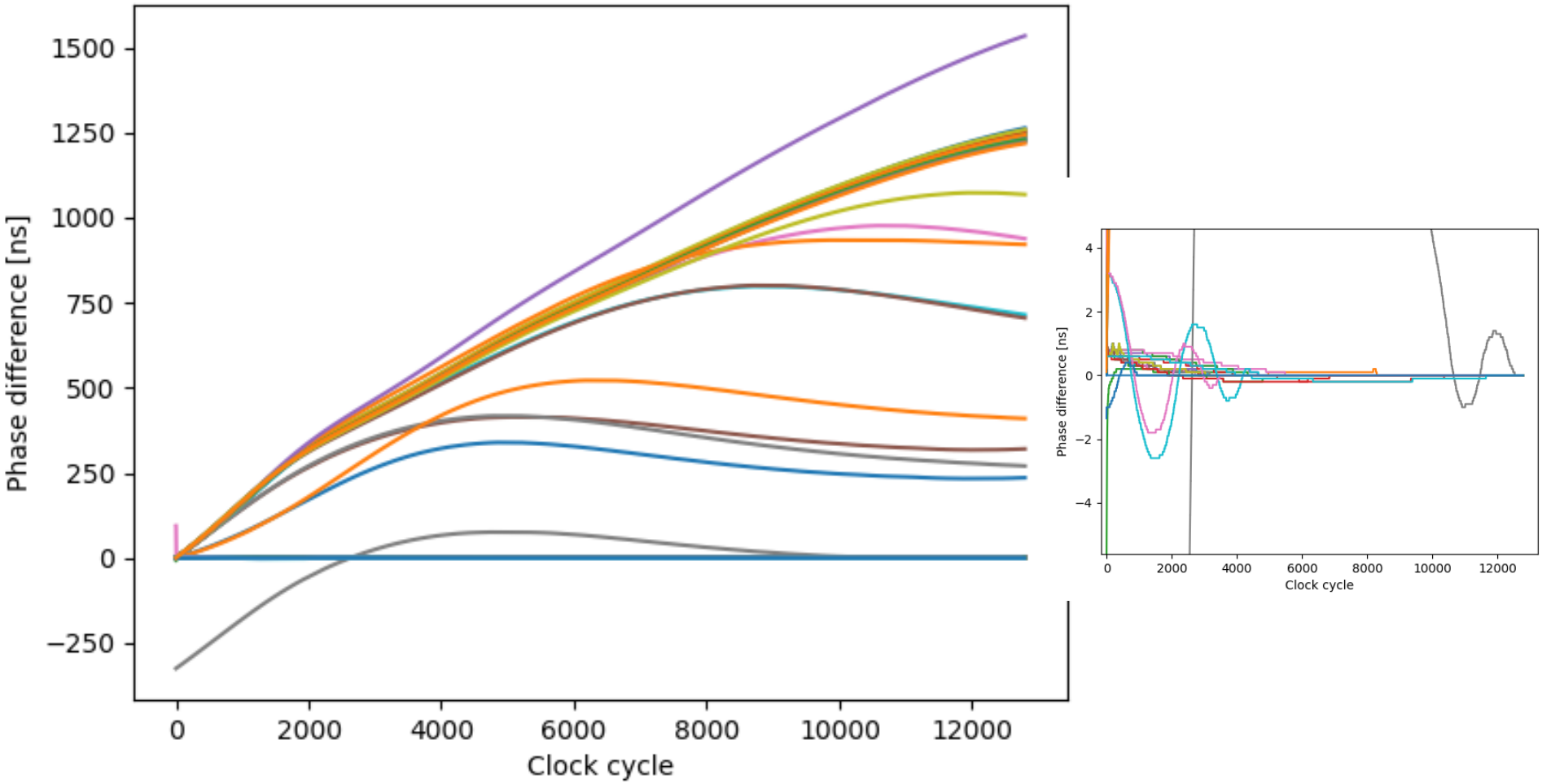






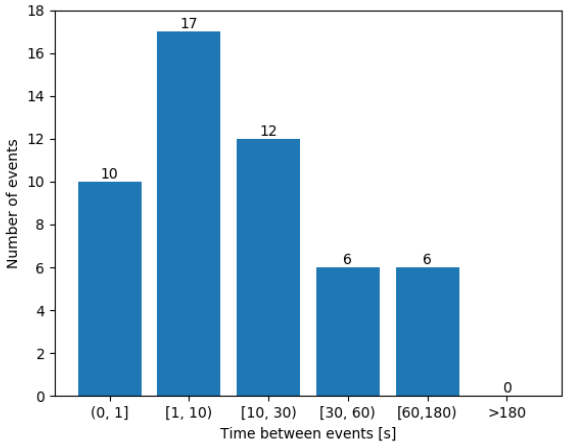


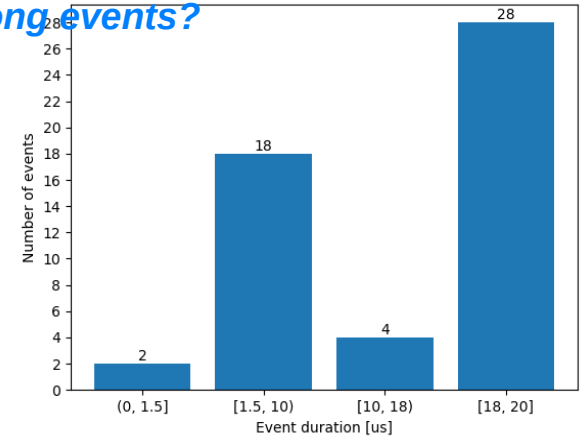
RUN 503: All trigger events

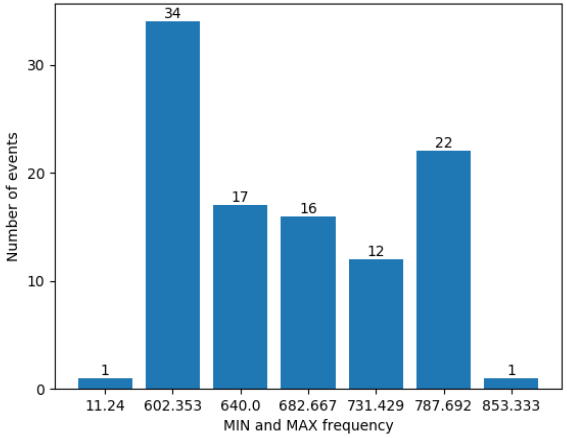


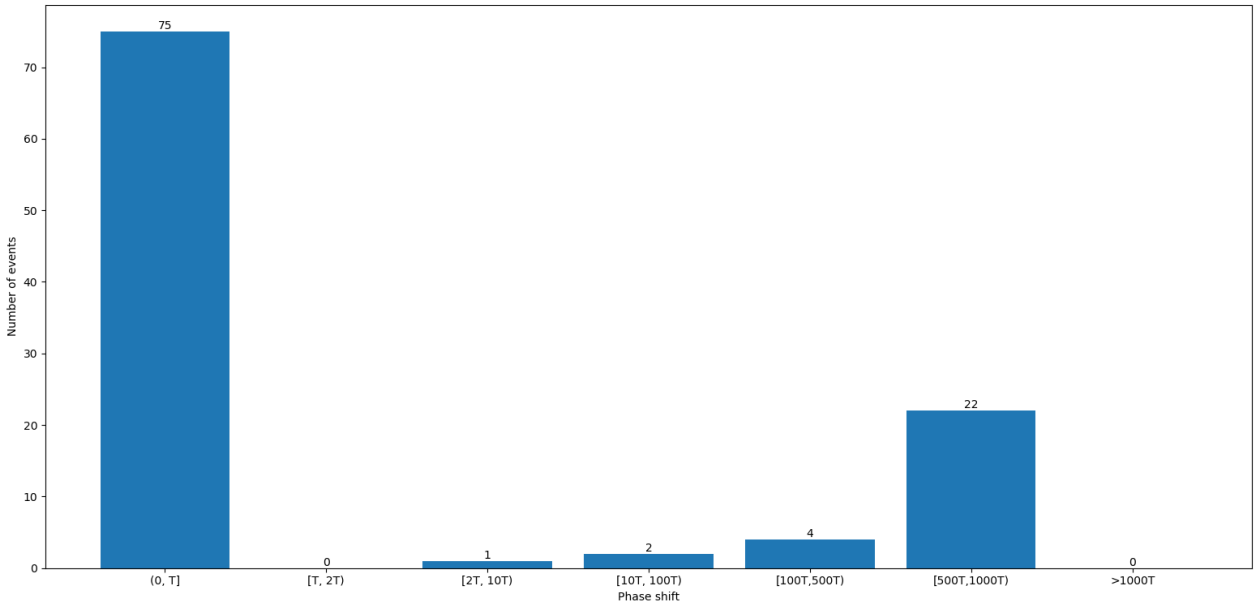
RUN 503: Phase measurements

LVDS receiver upset as a potential source of long events?

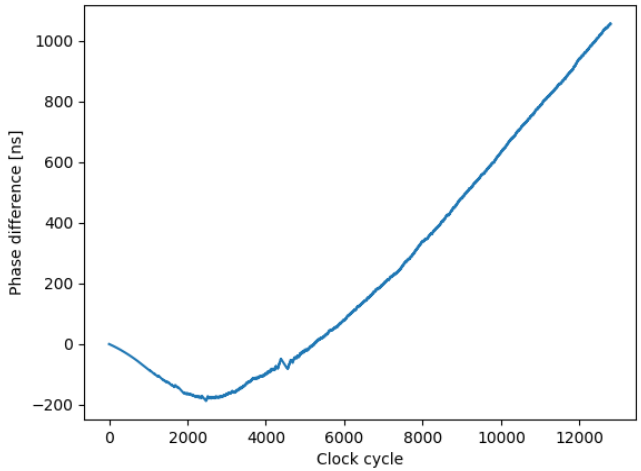


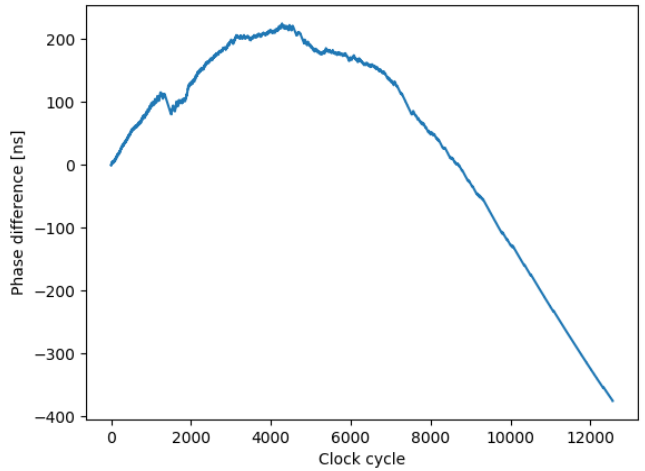


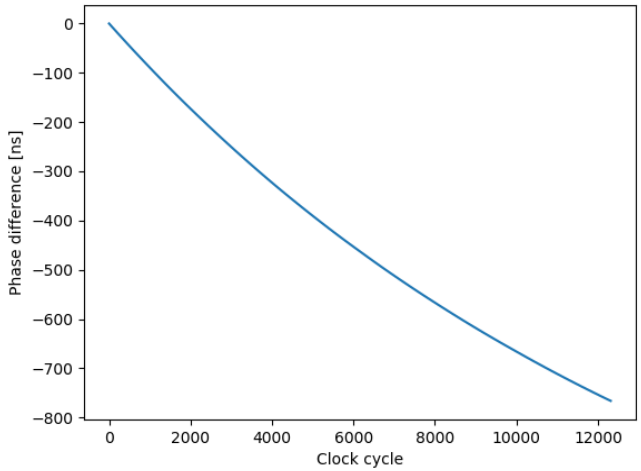


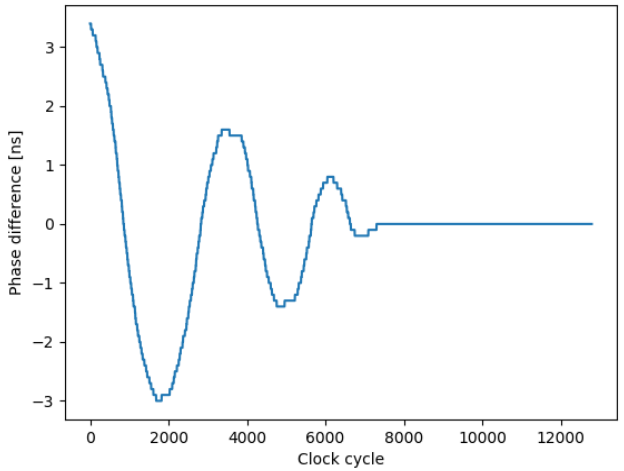


RUN 502: Phase measurements

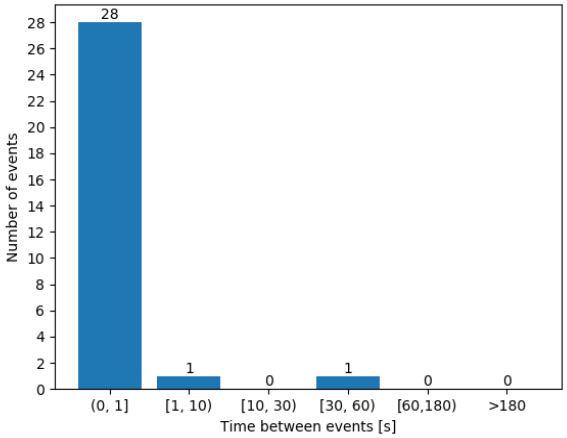


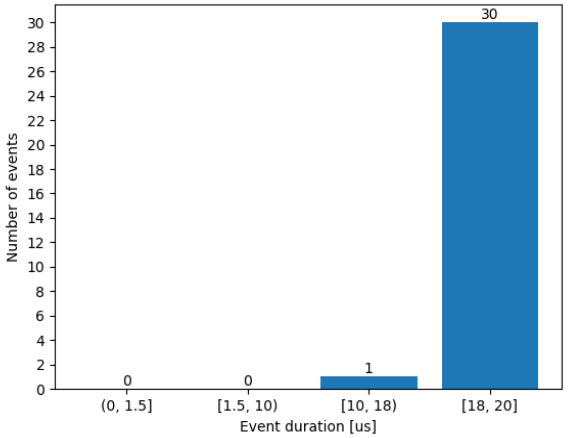


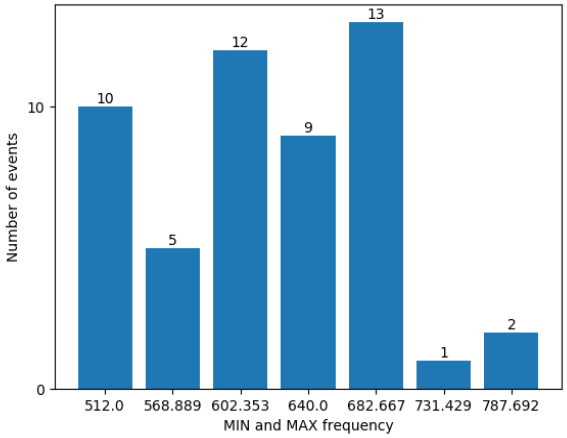


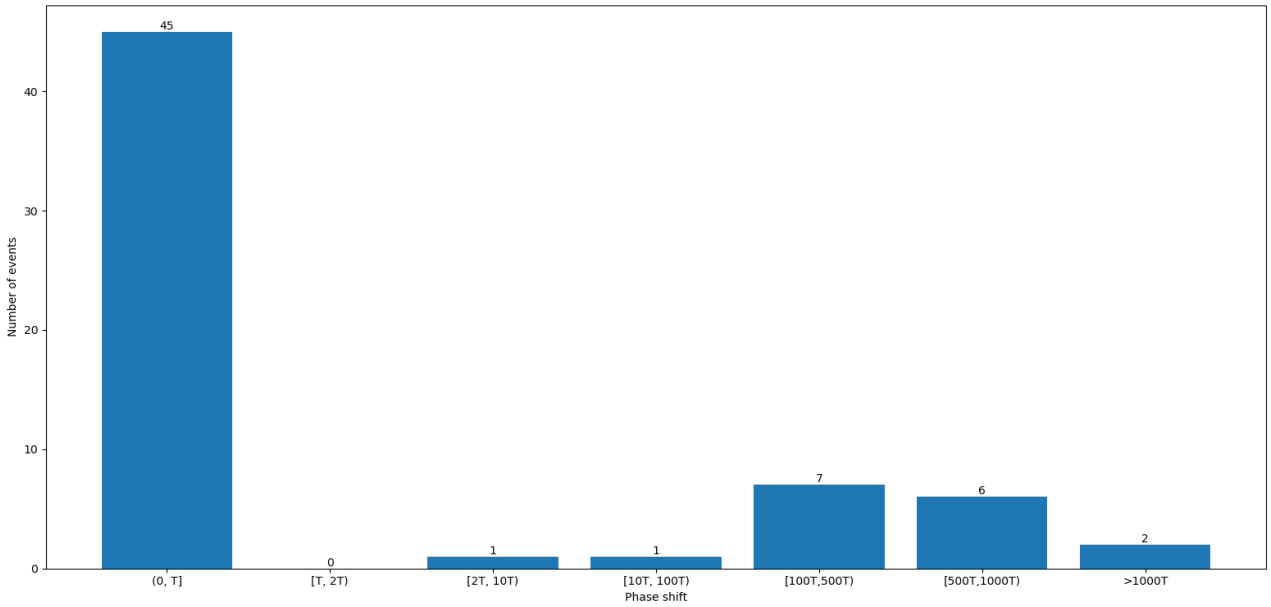


RUN 502: Phase measurements

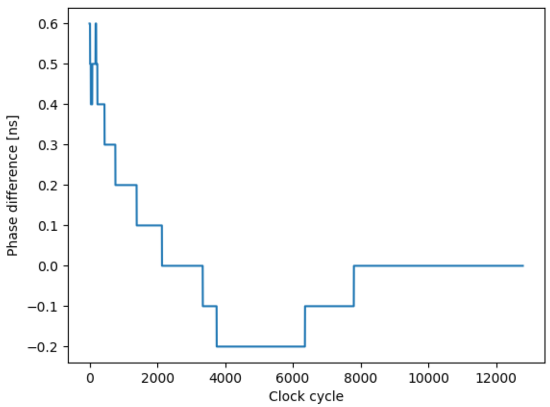


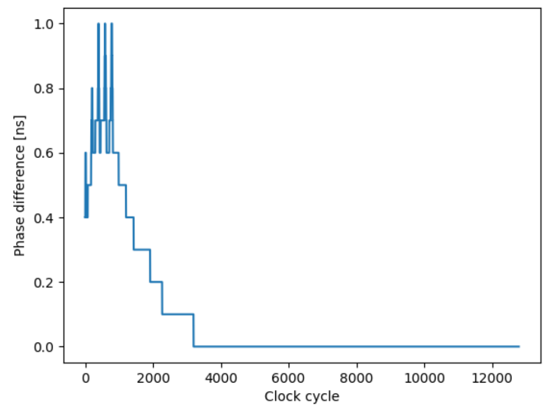


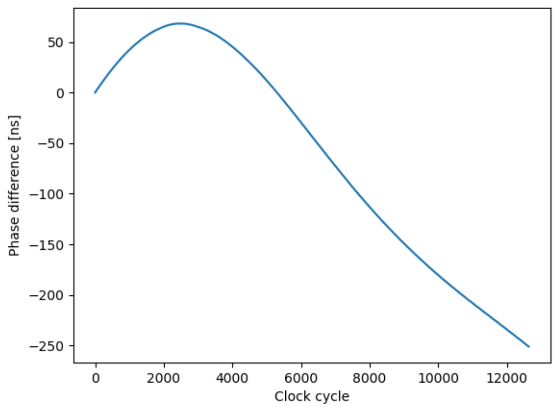


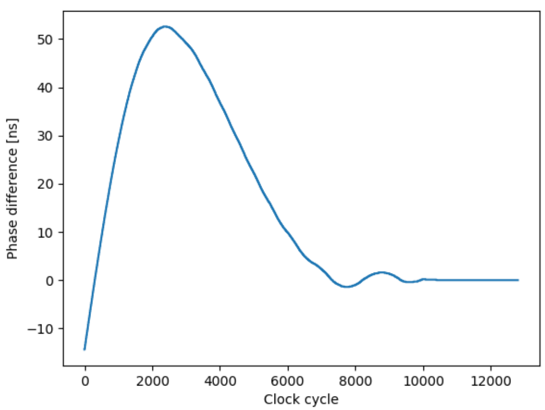


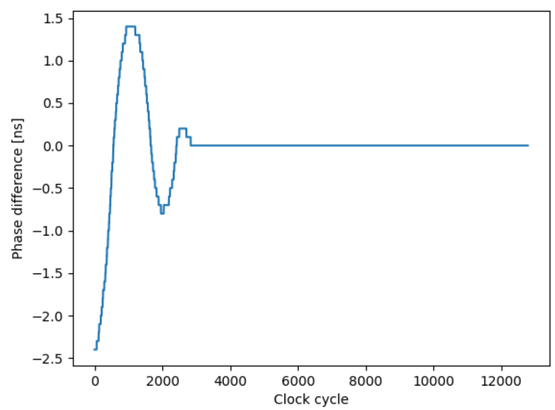
RUN 501: Phase measurements

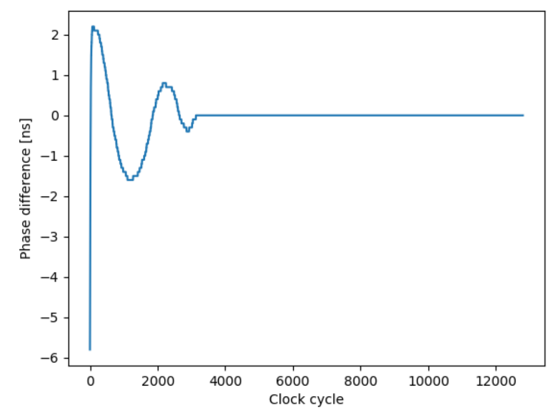




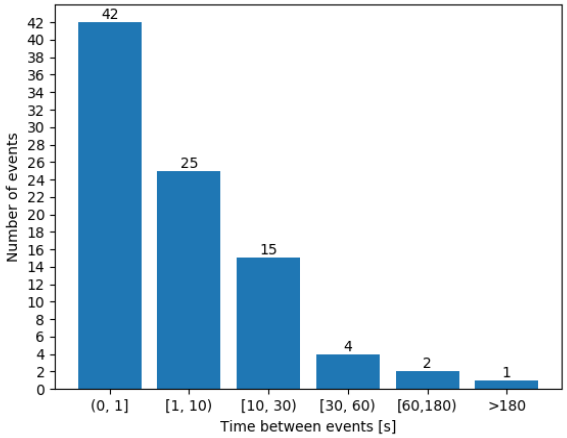


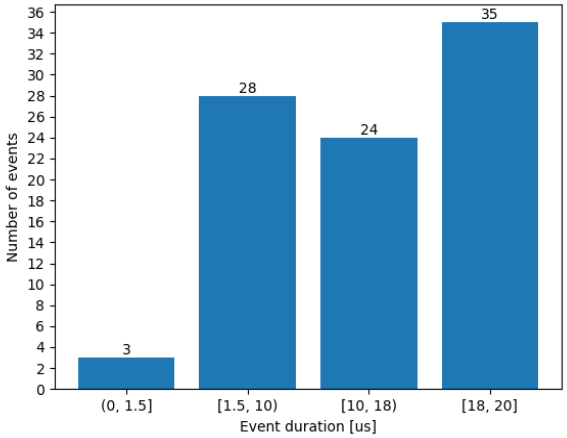


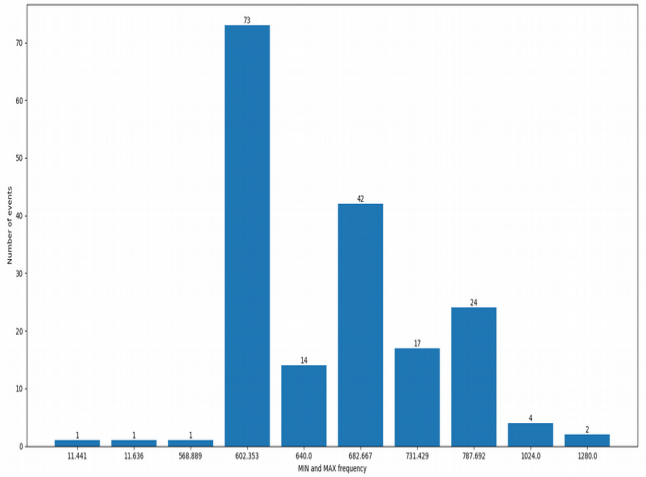


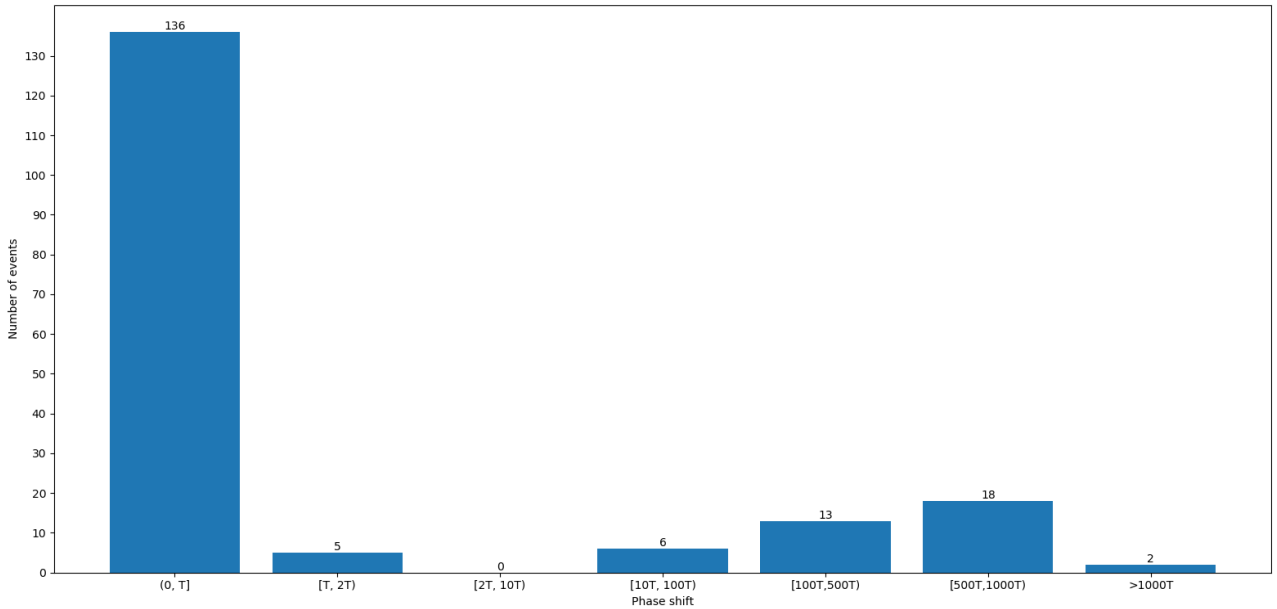


RUN 501: Phase measurements









Events with “gaps”

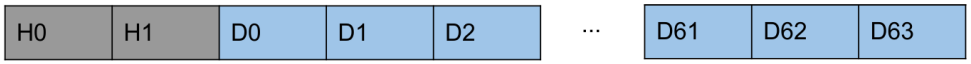
CML driver upset as a source of this event?

RUN(PLL Mode@1.28Gbit/s)	Number of events	Gap interval [ns]
501	0	-
502	14	[1.6, 12.0]
503	18	[1.6, 11.2]
504	2	[7.2, 9.6]

Digital Scan Results Overview

SH_INVALID_CNT_MAX: was set to 16

SEE proton campaign: Aurora link (de)sync issues



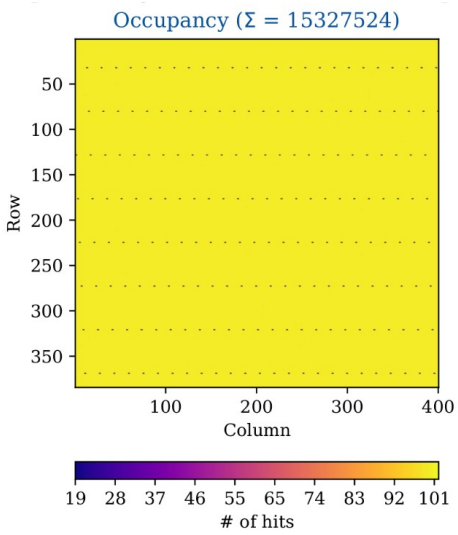
Soft error: Reported by Aurora Xilinx IP if ‘00’ or ‘11’ header is received (illegal headers)

Block Sync SM (for Aurora Xilinx IP):
SH_CNT_MAX (In BDAQ set to: 64)
SH_INVALID_CNT_MAX (In BDAQ set to: 1023)

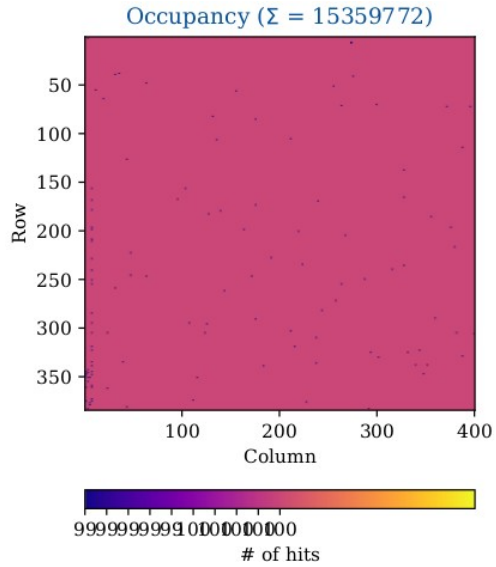
Rx Sync Error:

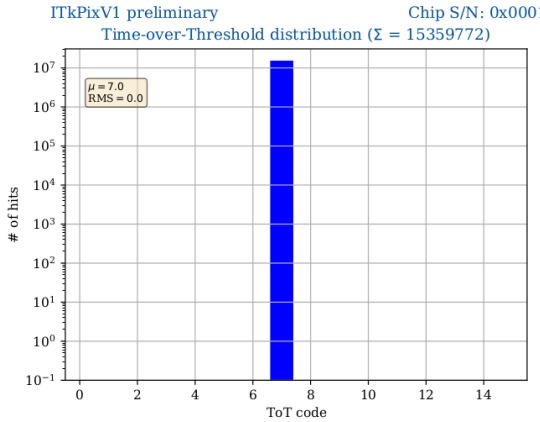
Reported if SH_INVALID_CNT_MAX of soft errors is received inside SH_CNT_MAX received headers. After SH_CNT_MAX headers are received, SH_INVALID_CNT_MAX is set to 0.

4% of data



96% of data





Conclusions

- 2 Setups for monitoring CDR outputs – setup with the scope, and 10.24Gb/s oversampling with Kintex-7. Second setup has higher resolution, but triggering logic is less sensitive. This results in smaller number of captured trigger events in comparison with the first setup, due to triggering on frequency jump

- 3 possible sources of presented events:
  - PLL
  - Differential receiver (emphasis on the events > 20us)
  - CML driver (emphasis on events with “signal gap”)

- Communication and link stability with increased water mark for Aurora Block Sync SM more reliable (compared to the link stability during testing in TRIUMF)

THANK YOU!