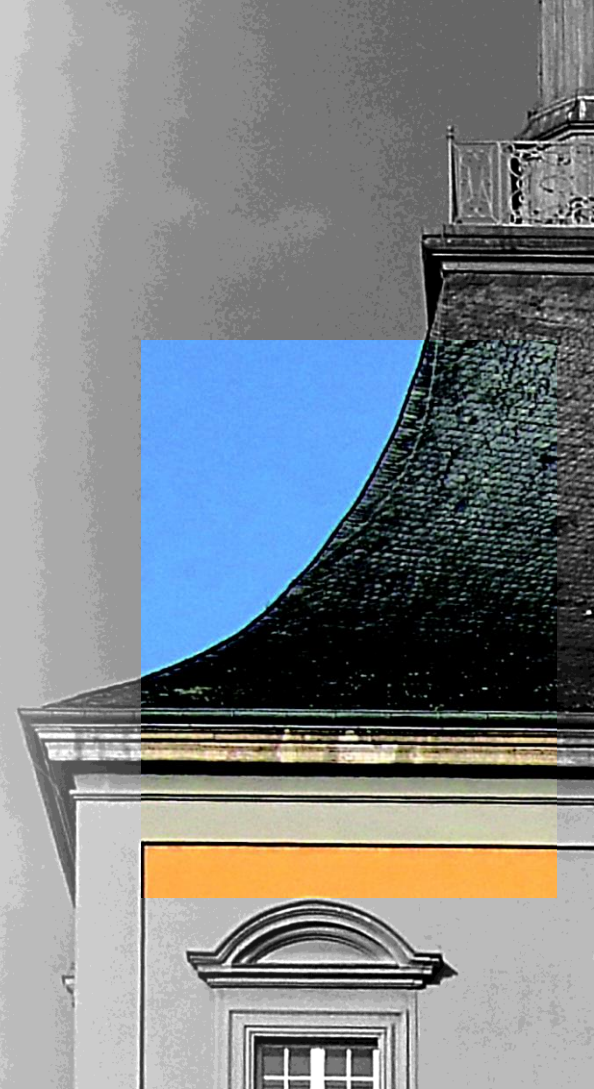


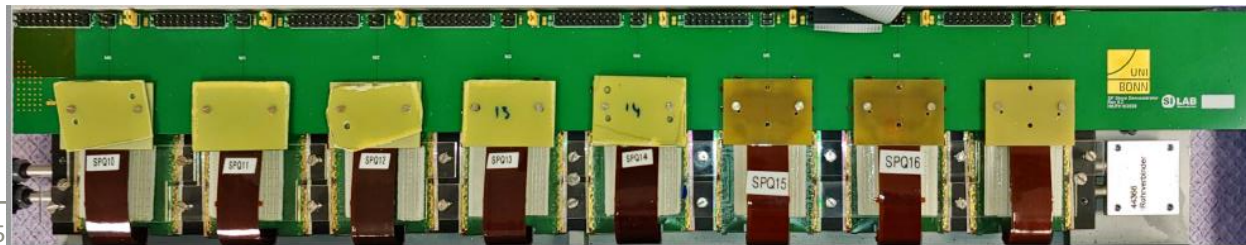
RD53A PLANAR SP CHAIN UPDATE

MATTHIAS HAMER, FLORIAN HINTERKEUSER



RD53A PLANAR SERIAL POWERING CHAIN – REVISED SERVICES

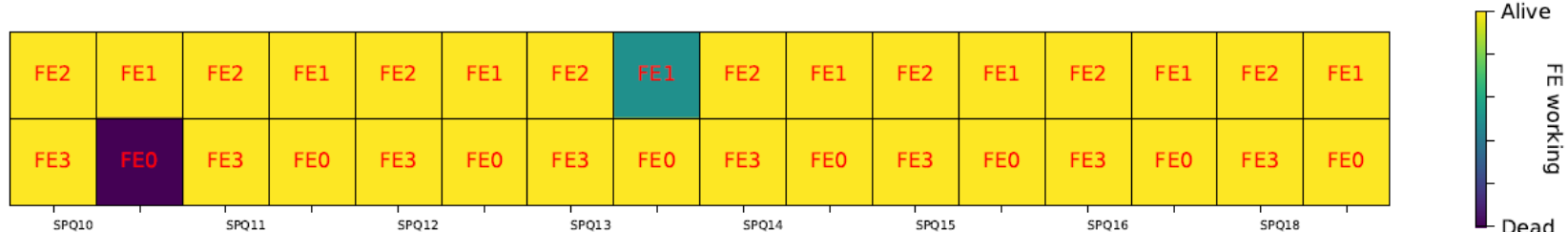
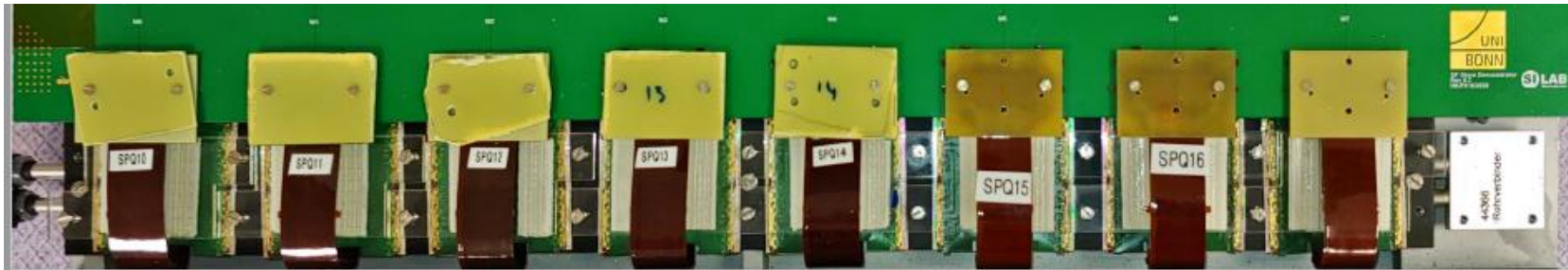
- Using new flexes, **first 10 modules** have been built (**1 digital, 9 thick quads**)
- **Yield** from quick reception test **promising: 7 thick quads fully working** (SPQ11-16, SPQ18)
- **Completed** module characterisation (**SLDO IV, Sensor IV, FE-characterisation**) on all 10 quads
- **First 8 Quads loaded** on stave, „worst“ operational module SPQ17 left out
- **SLDO IV curves** of all modules in serial chain measured
- Measured **threshold distributions** & general chip functionality **for all FE** after tuning to **2ke & 1ke** (LIN & DIFF only) & required startup current for all modules
- Current headroom measurements currently ongoing



Quads SPQ10-SPQ16 & SPQ18 loaded on stave, connected to new revision of stave flex and EoS-Card (not shown).

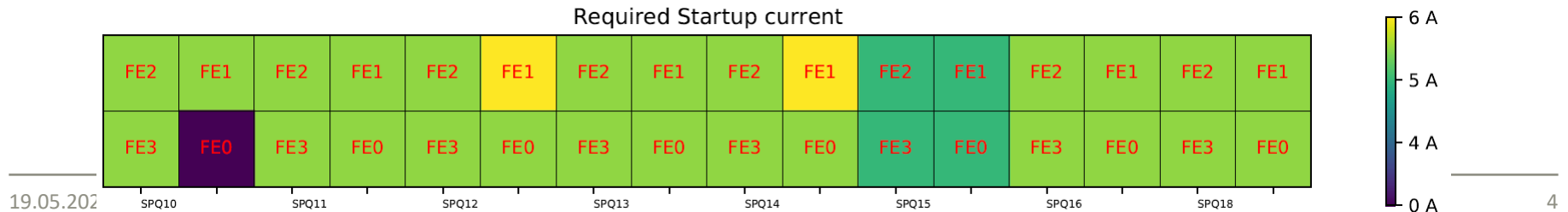
RD53A PLANAR SERIAL POWERING CHAIN – MODULE YIELD

- All chips on-stave but one are alive & communicating
- SPQ10_FE0 has faulty SLDO, can't communicate
- SPQ13_FE1 analog dead after tuning to 1ke



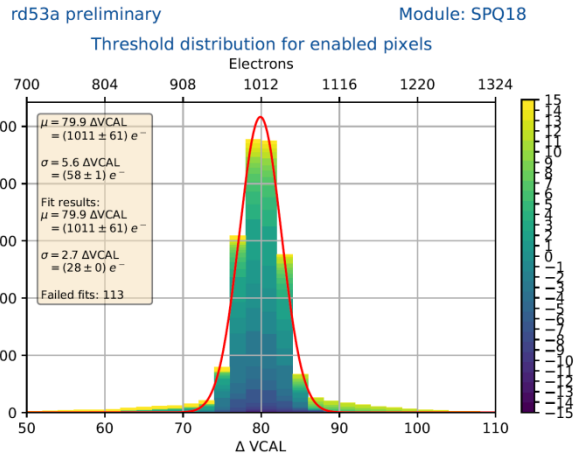
RD53A PLANAR SERIAL POWERING CHAIN – MODULE PERFORMANCE

- All chips on-stave but one are alive & communicating
- SPQ10_FE0 has faulty SLDO, can't communicate
- **Most** modules require $I_{in} \geq 5A$ to fully start
 - First FE start around 3A
- **Some** require **up to 6A** for startup
- > **RD53A specific problem**

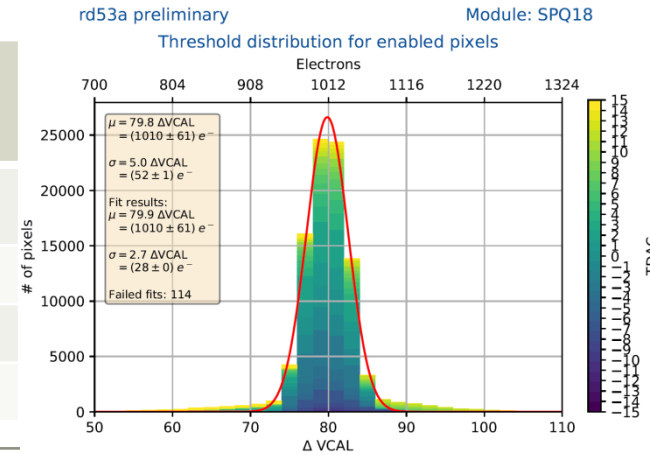


RD53A PLANAR SERIAL POWERING CHAIN – MODULE PERFORMANCE

- For all modules: tuning to 2ke / 1ke, measure threshold distr., noise, in-time-threshold in SP chain
- Compare with results from module reception tests
- Track for different HV schemes, chain current, chain length [...]

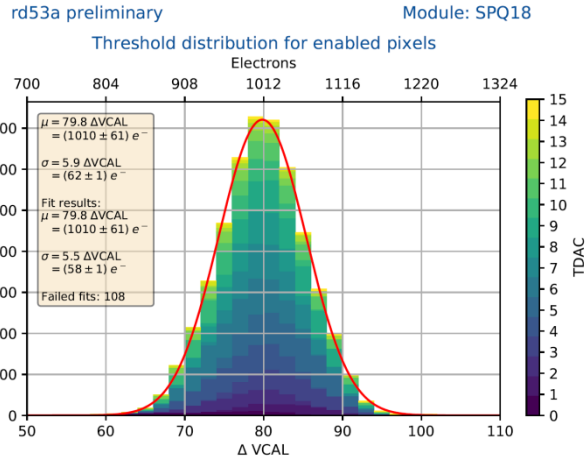


SPQ18_DIFF	Stave, Solo	Stave, SP chain, 1 common HV _{in} , 1 HV _{ret}
Threshold	1011 e	1010 e
Thresh. Disp	28 e	28 e
Noise	(108 ± 7) e	(110 ± 7) e
Failed Fits	113	114

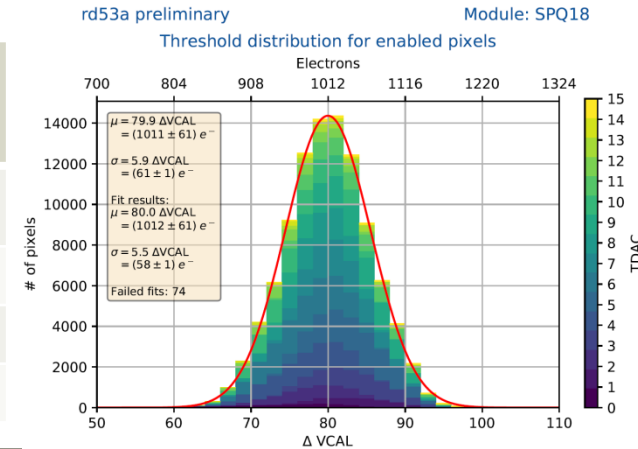


RD53A PLANAR SERIAL POWERING CHAIN – MODULE PERFORMANCE

- For all modules: tuning to 2ke / 1ke, measure threshold distr., noise, in-time-threshold in SP chain
- Compare with results from module reception tests
- Track for different HV schemes, chain current, chain length [...]

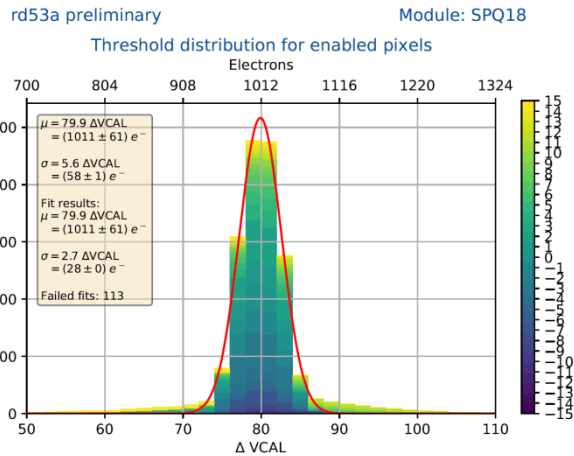


SPQ18_LIN	Stave, Solo	Stave, SP chain, 1 common HV _{in} , 1 HV _{ret}
Threshold	1010 e	1012 e
Thresh. Disp	58 e	58 e
Noise	$(190 \pm 10) e$	$(192 \pm 10) e$
Failed Fits	108	74

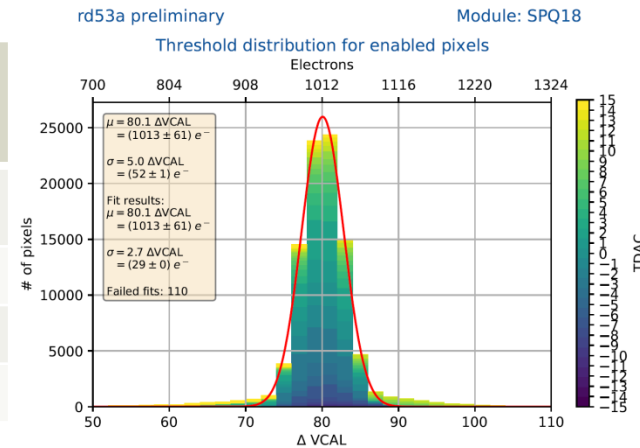


RD53A PLANAR SERIAL POWERING CHAIN – MODULE PERFORMANCE

- For all modules: tuning to 2ke / 1ke, measure threshold distr., noise, in-time-threshold in SP chain
- Compare with results from module reception tests
- Track for different HV schemes, chain current, chain length [...]

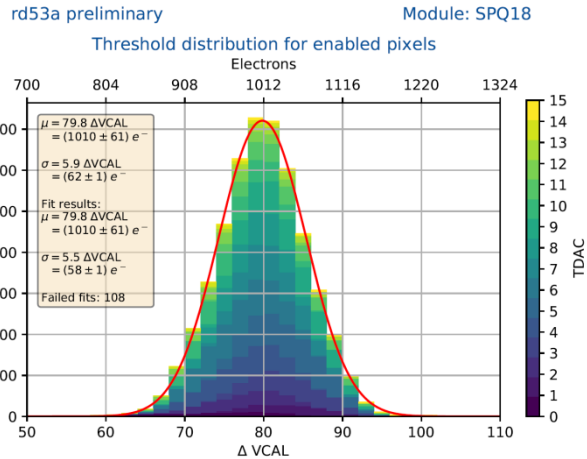


SPQ18_DIFF	Stave, Solo	Stave, SP chain, 2 common HV _{in} , 2 HV _{ret}
Threshold	1011 e	1013 e
Thresh. Disp	28 e	29 e
Noise	(108 ± 7) e	(109 ± 8) e
Failed Fits	113	110

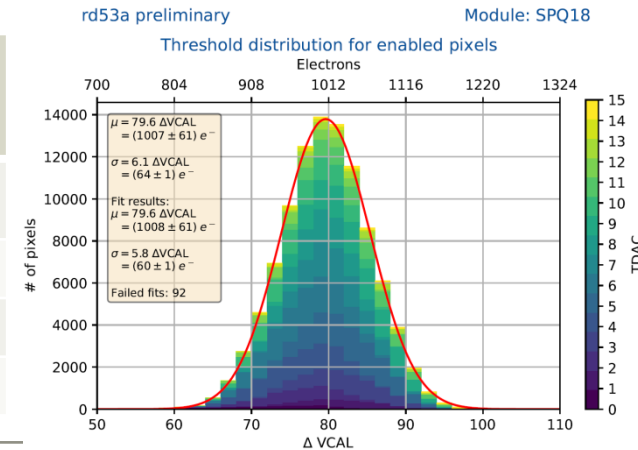


RD53A PLANAR SERIAL POWERING CHAIN – MODULE PERFORMANCE

- For all modules: tuning to 2ke / 1ke, measure threshold distr., noise, in-time-threshold in SP chain
- Compare with results from module reception tests
- Track for different HV schemes, chain current, chain length [...]



SPQ18_LIN	Stave, Solo	Stave, SP chain, 2 common HV _{in} , 2 HV _{ret}
Threshold	1010 e	1008 e
Thresh. Disp	58 e	60 e
Noise	$(190 \pm 10) e$	$(191 \pm 10) e$
Failed Fits	108	92

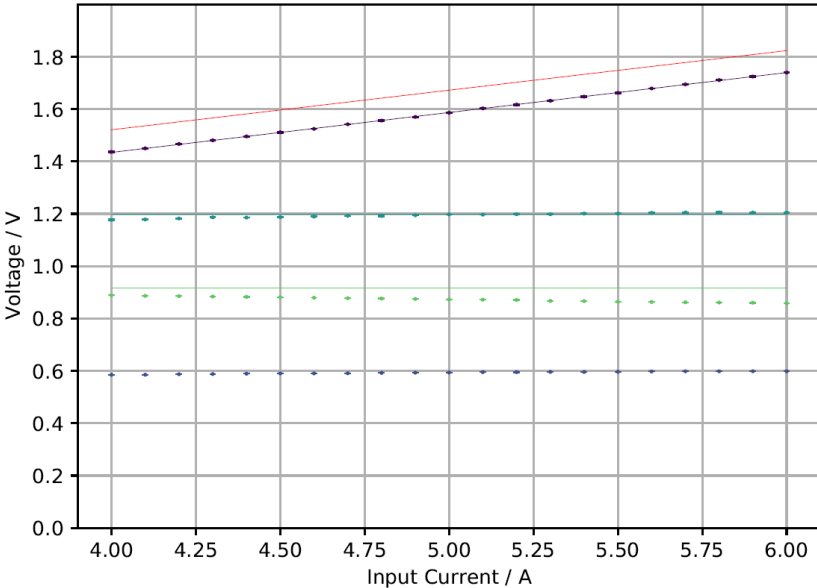


RD53A PLANAR SERIAL POWERING CHAIN – MODULE IV CURVES

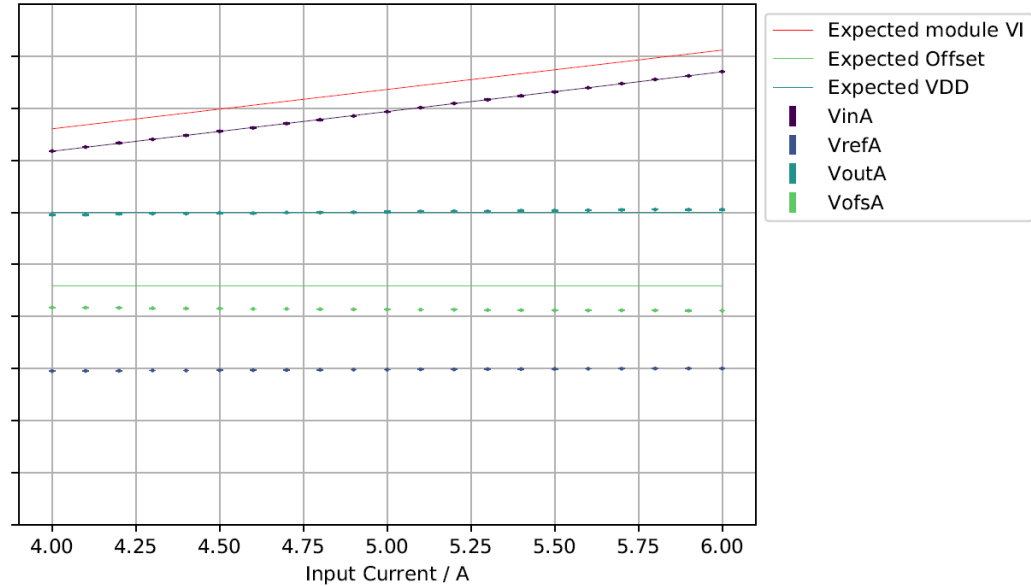
- Measure **SLDO IV** curve for each quad in serial chain & compare with bench test / expectation
 - **From flex loading** expect: $V_{ofs} = 0.9 \text{ V}$, $V_{in} \approx 1.5 \text{ V @ } I_{in} = 4.5 \text{ A}$, $V_{DD} = V_{DDA} = 1.2 \text{ V}$
- **Measure** V_{in} , V_{Out} , V_{ref} , V_{ofs} using **on-chip MUX** (corrected by GND offset)
 - In addition current through R_{ext} for on-module current sharing
- Expectation: **constant** V_{ref} , V_{out} , V_{ofs} ; Input **slope** from **spice**
 - using **Vofs, slopes** obtained in **wafer probing** when possible

RD53A PLANAR SERIAL POWERING CHAIN – MODULE IV CURVES

Input IV curve digital SLDO for FE0
VinD fit parameter: 0.1525 V/A, 0.8244 V



Input IV curve analog SLDO for FE0
VinA fit parameter: 0.1526 V/A, 0.8244 V



RD53A PLANAR SERIAL POWERING CHAIN – MODULE IV CURVES – PRELIMINARY SUMMARY

– Measured **SLDO IV** curve for each quad in serial chain

- $V_{IN_A,D}$ **tied** together on flex
- > **Fits** on V_{in} in very good **agreement**
- **Slope** fits expectation well
- **Offset too small**
- > **known to be RD53A specific**

SPQ13	Slope A	Offset A	Slope D	Offset D
FE0	0.1526 V/A	0.824 V	0.1525 V/A	0.8244 V
FE1	0.1524 V/A	0.828 V	0.153 V/A	0.826 V
FE2	0.1517 V/A	0.825 V	0.1511 V/A	0.828 V
FE3	0.153 V/A	0.825 V	0.1532 V/A	0.824 V

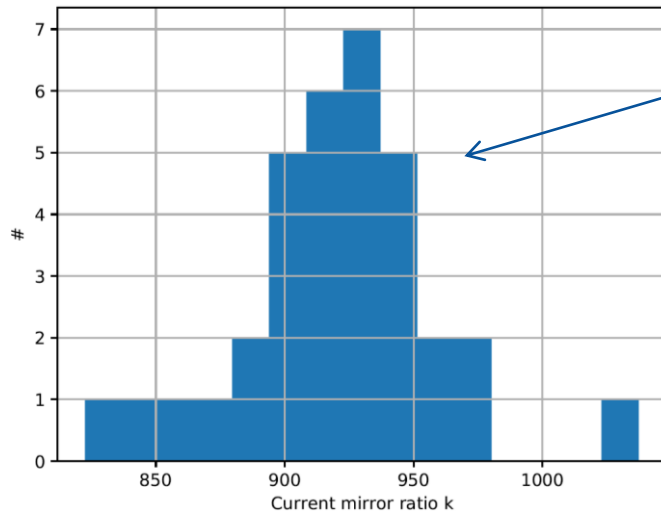
Spice	Full SPQ13
Slope	0.1512 V/A
Offset	0.916 V

RD53A PLANAR SERIAL POWERING CHAIN – MODULE IV CURVES – PRELIMINARY SUMMARY

- **Tried to estimate** on-module **current distribution** using voltage drop on **slope resistors**
- Current mirror ratio **k** from **slope fit** on **waferprobing data**
 - **Not always** usable probing **data available**
 - **Does not include dependency** of **k** on **input current** (k increases with I_{in})
 - > **Both will improve** significantly for **RD53B**
- **Track** current distribution through input IV
- This current distribution is an **estimate** based from observations, **not a hard truth**

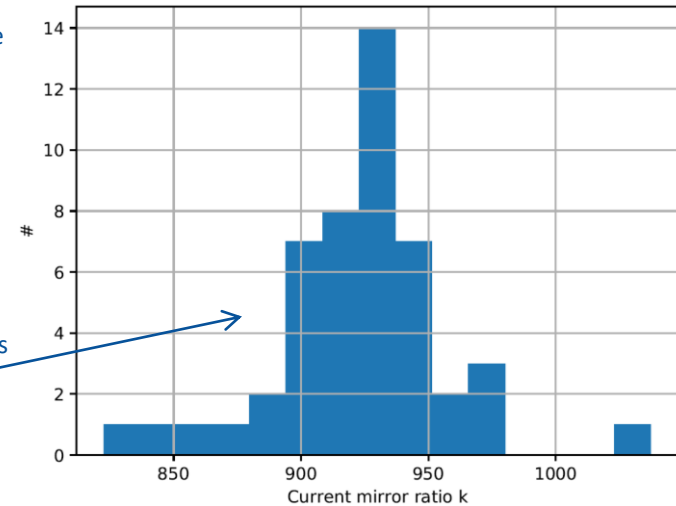
RD53A PLANAR SERIAL POWERING CHAIN – MODULE IV CURVES – PRELIMINARY SUMMARY

- **Tried to estimate** on-module **current distribution** using voltage drop on **slope resistors**
- Current mirror ratio k from **slope fit** on **waferprobing data**



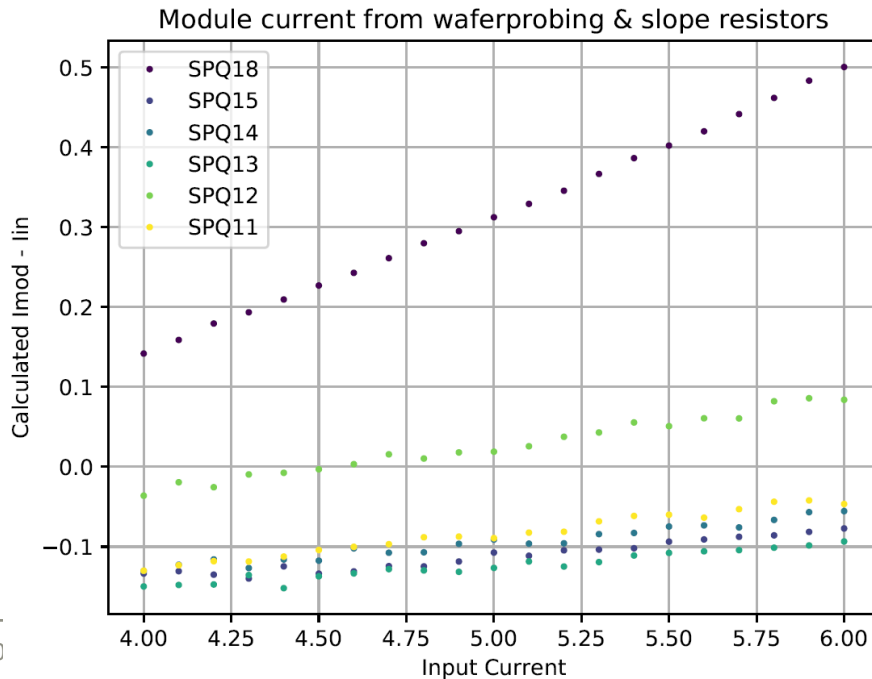
Current mirrors from available data (left), only good fits

Current mirrors with missing data replaced by average of remaining analog/digital SLDOs on given quad



RD53A PLANAR SERIAL POWERING CHAIN – MODULE IV CURVES – PRELIMINARY SUMMARY

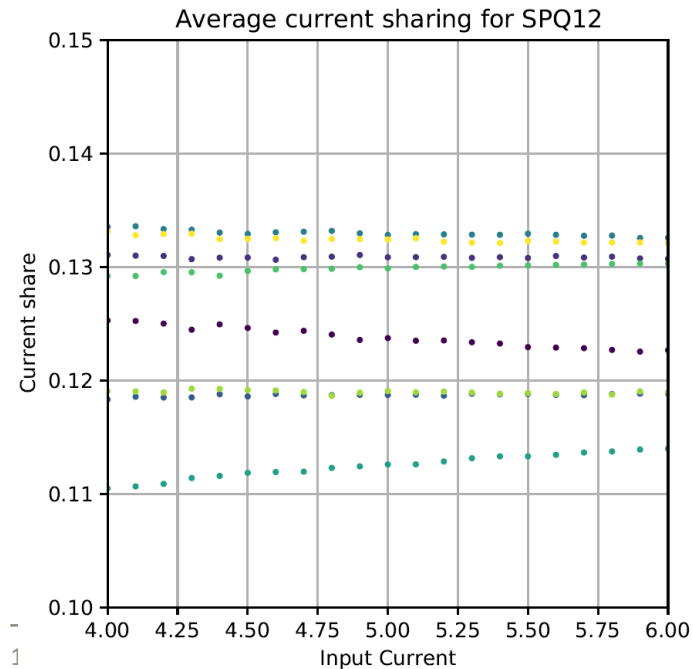
- **Tried to estimate on-module current distribution** using voltage drop on **slope resistors**
- Current mirror ratio k from **slope fit on waferprobing data**



- **Estimate module current I_{mod} by scaling current through R_{ext} with current mirror from wafer probing**
- Plot I_{in} vs $\Delta(I_{\text{mod}}, I_{\text{in}})$
 - Significant uncertainties $O(\%)$
 - Large slope on SPQ18 unexpected
- In general: slope on $\Delta(I_{\text{mod}}, I_{\text{in}})$ agrees with known slope on current mirror

RD53A PLANAR SERIAL POWERING CHAIN – MODULE IV CURVES – PRELIMINARY SUMMARY

- **Tried to estimate on-module current distribution** using voltage drop on **slope resistors**
- Current mirror ratio k from **slope fit on waferprobing data**



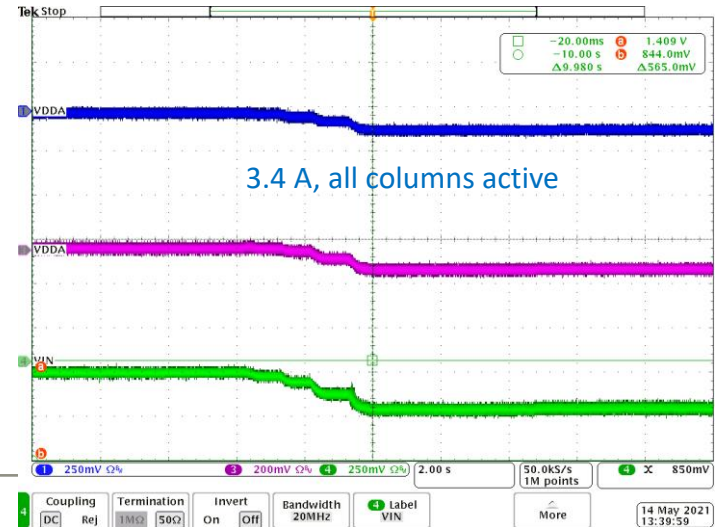
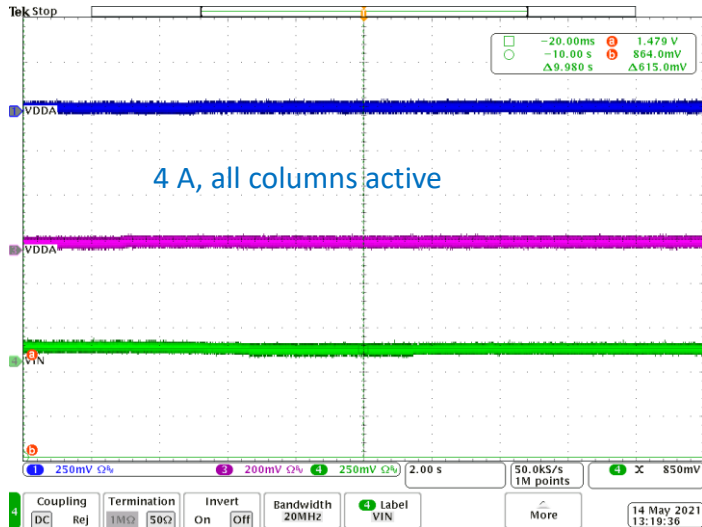
- **Estimate module current I_{mod} by scaling current through R_{ext} with current mirror from wafer probing**
- **Plot relative current sharing between SLDOs on a quad (ideal case: 12.5 %)**
- Slope possibly explained by differing $k(I_{\text{in}})$ dependencies for each SLDO

RD53A PLANAR SERIAL POWERING CHAIN – MODULE CURRENT HEADROOM

- Find **minimum** required **current** module to keep **module operational**
- **Baseline** for **SP Quads & common hybrid**: Module @ **1.5 V, 1.1 A / chip** (including headroom)
-> ~ 4.4 A @ 1.5 V
- **Procedure**: Starting at a safe I_{in} (e.g. 6 A), run defined scan, reduce current, repeat
 - Scan used here: „**random**“ **trigger source scan** (w/o source), **all FE/flavours enabled**
 - **Track VDDAs / VIN_{Quad}** on scope
 - Significant **drop** in both **VIN & VDDA** -> **SLDO overload**

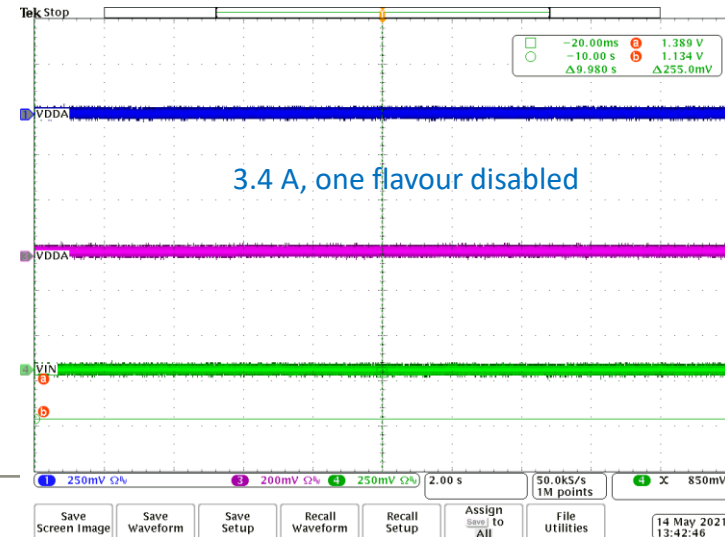
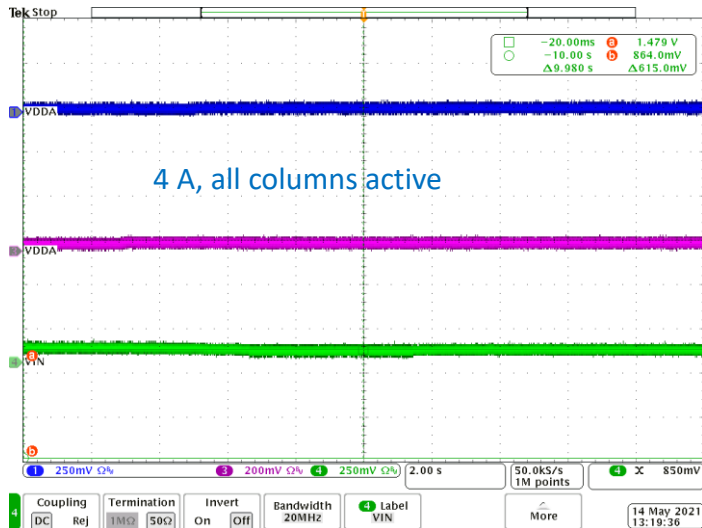
CURRENT HEADROOM

- Starting at $I_{in} = 6A$, reducing in **100 mA** steps
- **Once overload** is reached, measure **current** through **slope resistors**
- **Decrease** module current **consumption** by **disabling** parts of the chip -> does overload go away?



CURRENT HEADROOM

- Starting at $I_{in} = 6A$, reducing in **100 mA** steps
- **Once overload** is reached, measure **current** through **slope resistors**
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CURRENT HEADROOM

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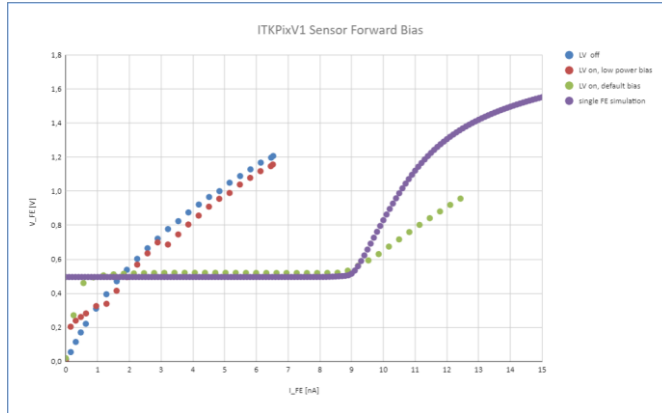
Quad	I_{in} overload / A	Module Voltage / V
SPQ11	3.8	1.4
SPQ12	3.4	1.34
SPQ13	3.6	1.37
SPQ14	3.4	1.35
SPQ15	3.5	1.36
SPQ18	3.5	1.37

CURRENT HEADROOM

- Starting at $I_{in} = 6A$, **reducing in 100 mA** steps
 - **Once overload** is reached, measure **current** through **slope resistors**
 - **Decrease** module current **consumption** by **disabling** parts of the chip -> does overload go away?
- For modules with higher overload current but same IV characteristic, larger current imbalance is expected
- This can not be observed with the currently available data

HV OFF MODE

- open question for HV modules was the requirement of the low-ohmic off-mode, it was not clear that this is really required
 - high impedance off-mode leads to substantial forward bias on sensors in SP chain during interfills
 - measurements done by Anastasia et al. at CERN with irradiated modules have provided an indication for the level of that forward bias and the expected currents (see [Anastasia's presentation](#)) for more details
 - led to a discussion in the sensor group: no issue for sensors, but concerns were raised about risks to the analog FE
 - follow-up measurements done in Bonn (H. Krüger et al.) with an unirradiated ITkPixV1 Chip bonded to a planar Micron sensor:

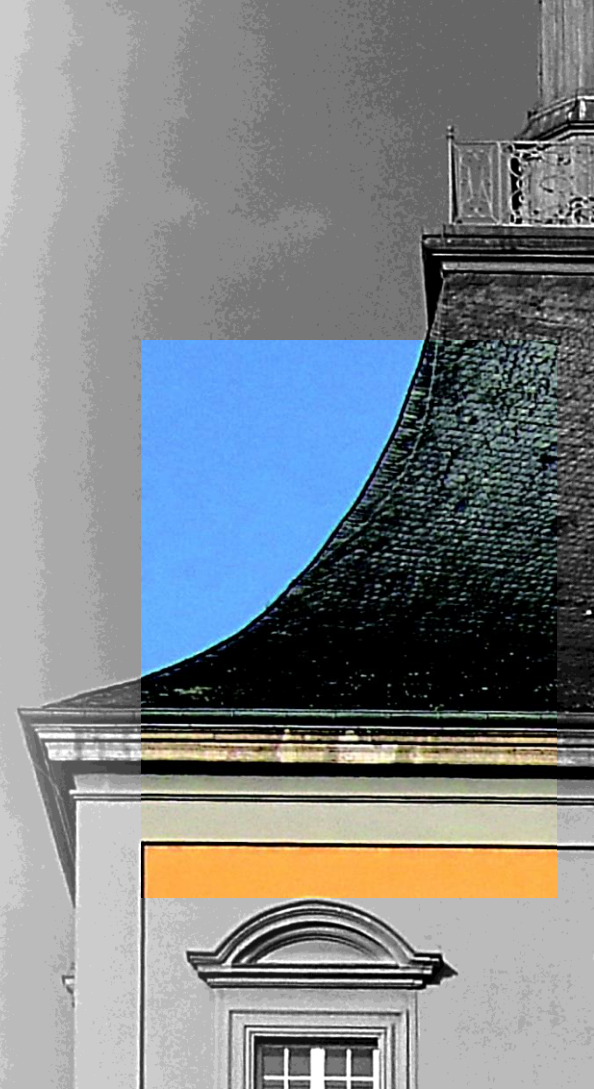


- forward bias applied directly to the backside of the sensor through series resistor
- voltage is measured at the bias grid (PT biasing for the used sensor)
- worst case in the detector: < 3.5 nA per pixel
 - we don't expect to ever get there
 - Anastasia's measurements indicate a maximum current below that
- results still require some more understanding:
 - behaviour of bias-grid potential for small currents (I-V of PT grid?)
 - difference between simulation and measurement at large currents (averaging effect?)
- plan to repeat this measurement with the RD53A quad chain

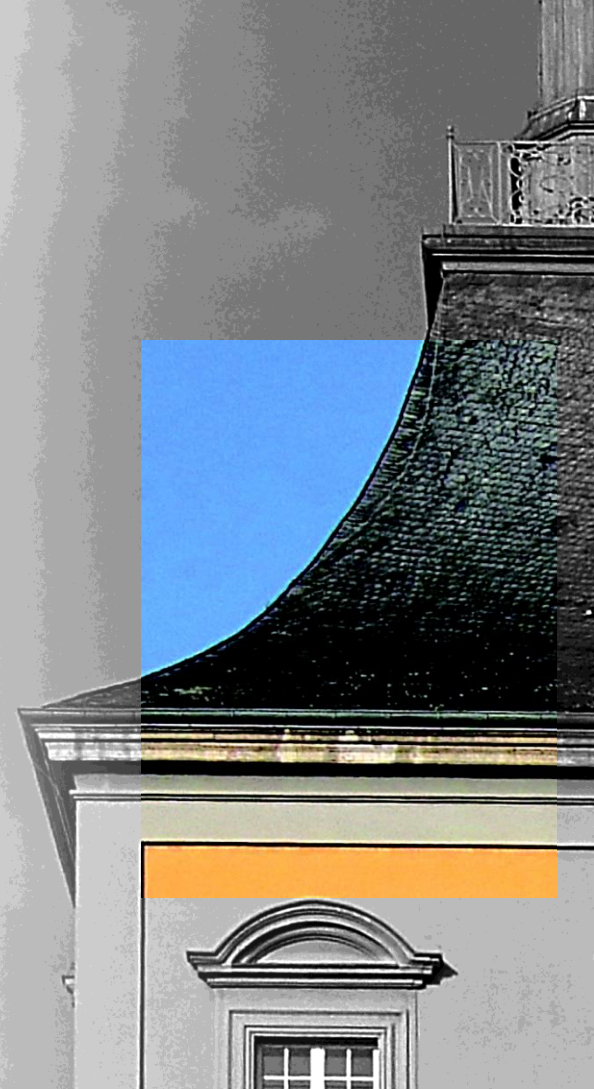
SUMMARY & OUTLOOK

- Characterisation of the **Bonn serial powering test setup** is progressing
 - **Results so far look promising**
 - Did not encounter any surprises
- Can **plug in digital ITkPix modules** when available
 - **First ITkPix V1.0 SP quad** wirebonded yesterday, currently **being tested**
 - **Expect** ITkPix V1.1 chips for digital SP quads to **arrive this week**
 - **Stave** loaded with **ITkPix SP quads ~ June**
 - **Setup with ITkPixV1.1** modules to be **shipped to CERN** for system tests with representative **long services**

THANK YOU



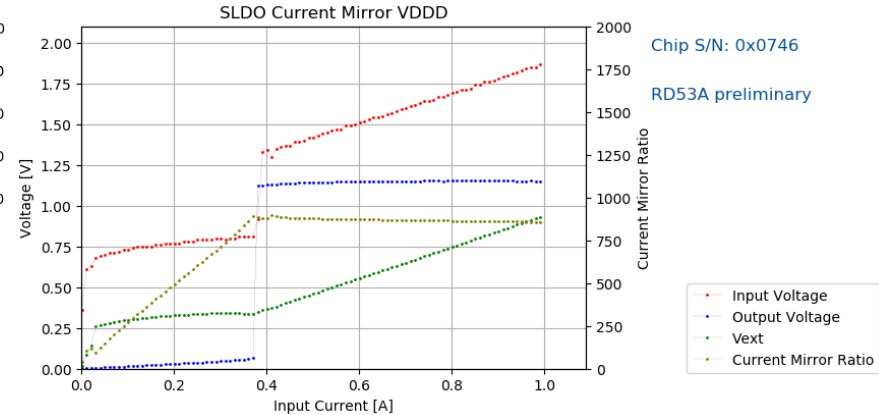
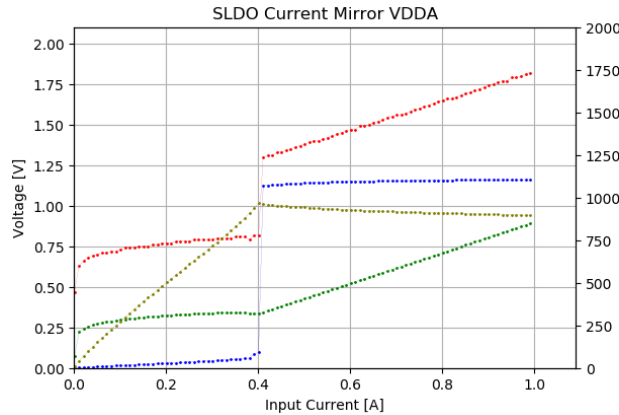
BACKUP



RD53A CURRENT MIRROR EXAMPLE

Current Mirror

R_{ext_A}	$895 \leq k \leq 965$
R_{eff_A}	889
R_{ext_D}	$857 \leq k \leq 894$
R_{eff_D}	900
Ideal case	1000



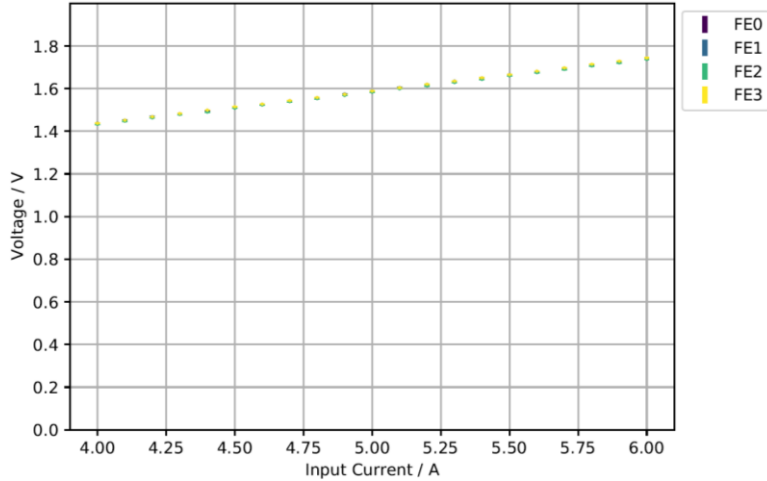
Chip S/N: 0x0746

RD53A preliminary

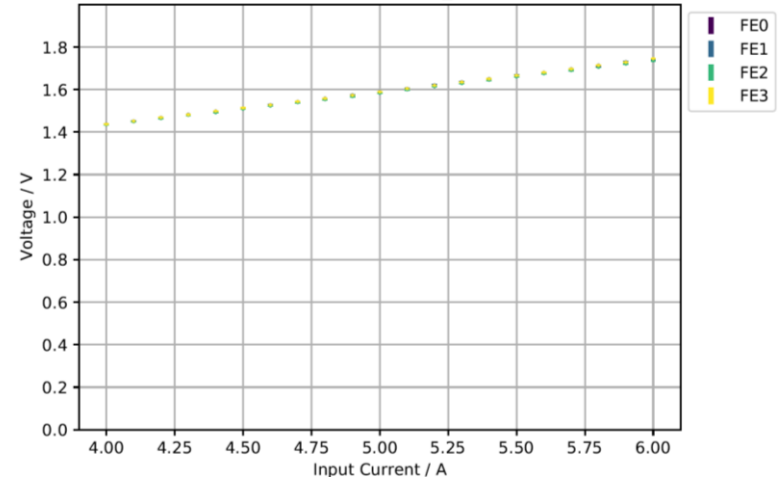
- Current mirror ratio smaller than expected
- K depends on input current
- R_{eff} gives only estimate on k

VINA / VIND DISTRIBUTION ON SPQ13

Distribution of VinA_SLDO



Distribution of VinD_SLDO



SPQ13	Slope A	Offset A	Slope D	Offset D
FE0	0.1526 V/A	0.824 V	0.1525 V/A	0.8244 V
FE1	0.1524 V/A	0.828 V	0.153 V/A	0.826 V
FE2	0.1517 V/A	0.825 V	0.1511 V/A	0.828 V
FE3	0.153 V/A	0.825 V	0.1532 V/A	0.824 V

CURRENT HEADROOM

- Starting at $I_{in} = 6A$, **reducing in 100 mA** steps
- **Once overload** is reached, measure **current** through **slope resistors**
- **Decrease** module current **consumption** by **disabling** parts of the chip -> does overload go away?

Quad	I_{in} overload / A	Module Voltage / V
SPQ11	3.8	1.4
SPQ12	3.4	1.34
SPQ13	3.6	1.37
SPQ14	3.4	1.35
SPQ15	3.5	1.36
SPQ18	3.5	1.37

SPQ18	$I_{SLDO,Analog}$ / A	$I_{SLDO,Digital}$ / A
FE0	0.42	0.4
FE1	0.455	0.46
FE2	0.448	0.415
FE3	0.4	0.45
Total	3.44 A	Expected 3.5 A

SPQ11	$I_{SLDO,Analog}$ / A	$I_{SLDO,Digital}$ / A
FE0	0.442	0.441
FE1	0.43	0.439
FE2	0.363	0.45
FE3	0.42	0.411
Total	3.4 A	Expected 3.8 A