RD53a Triplet
SP chain with sensors

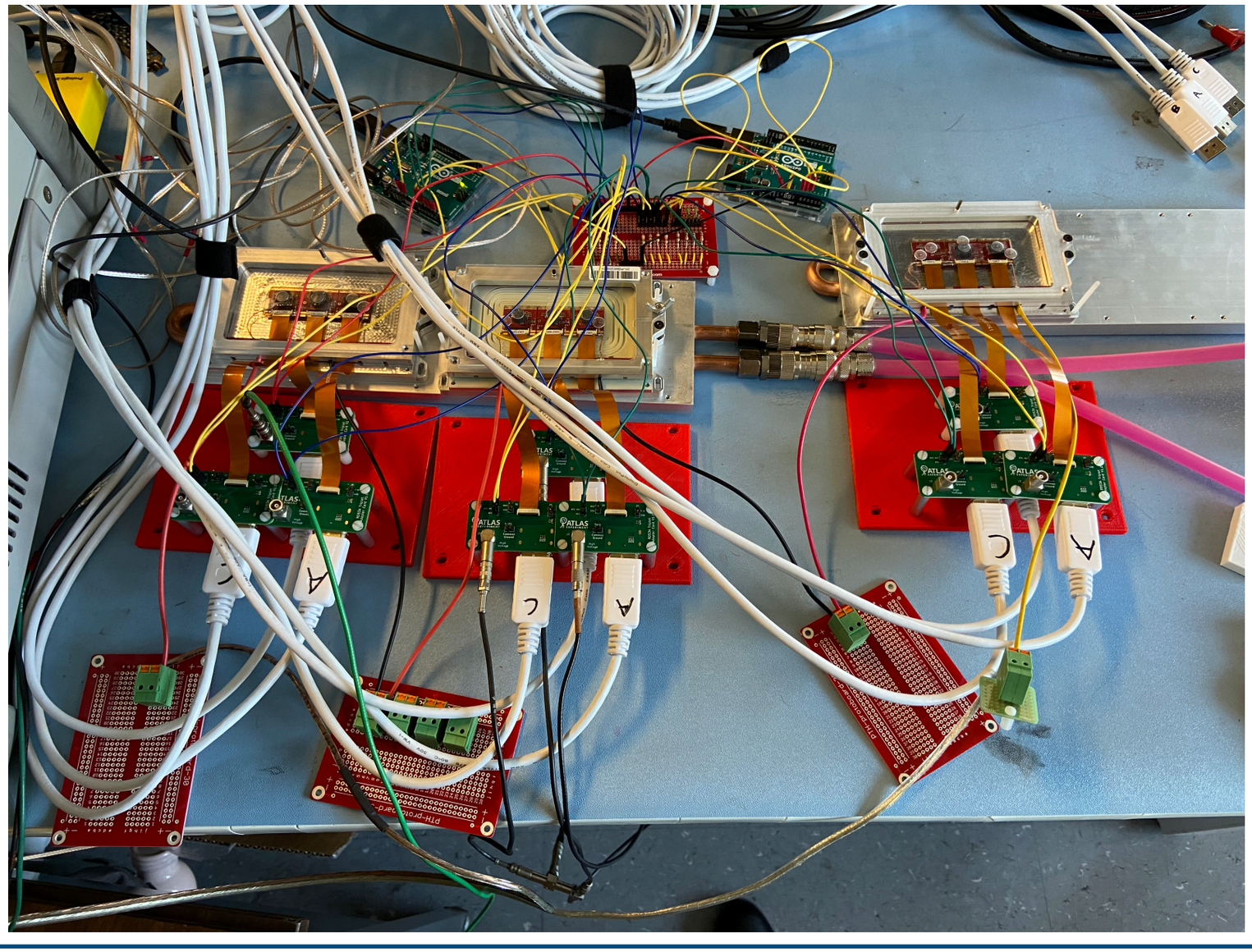
Maurice Sciveres-Garcia, Timon Heim,
Elisabetta Pianori, **Elodie Resseguie**

Lawrence Berkeley National Laboratory

May 19, 2020
RD53b testing meeting

Introduction

- We received 12 3D modules and 10 planar modules
- We assembled 2 triplets with 3D sensors and 1 with planar sensors



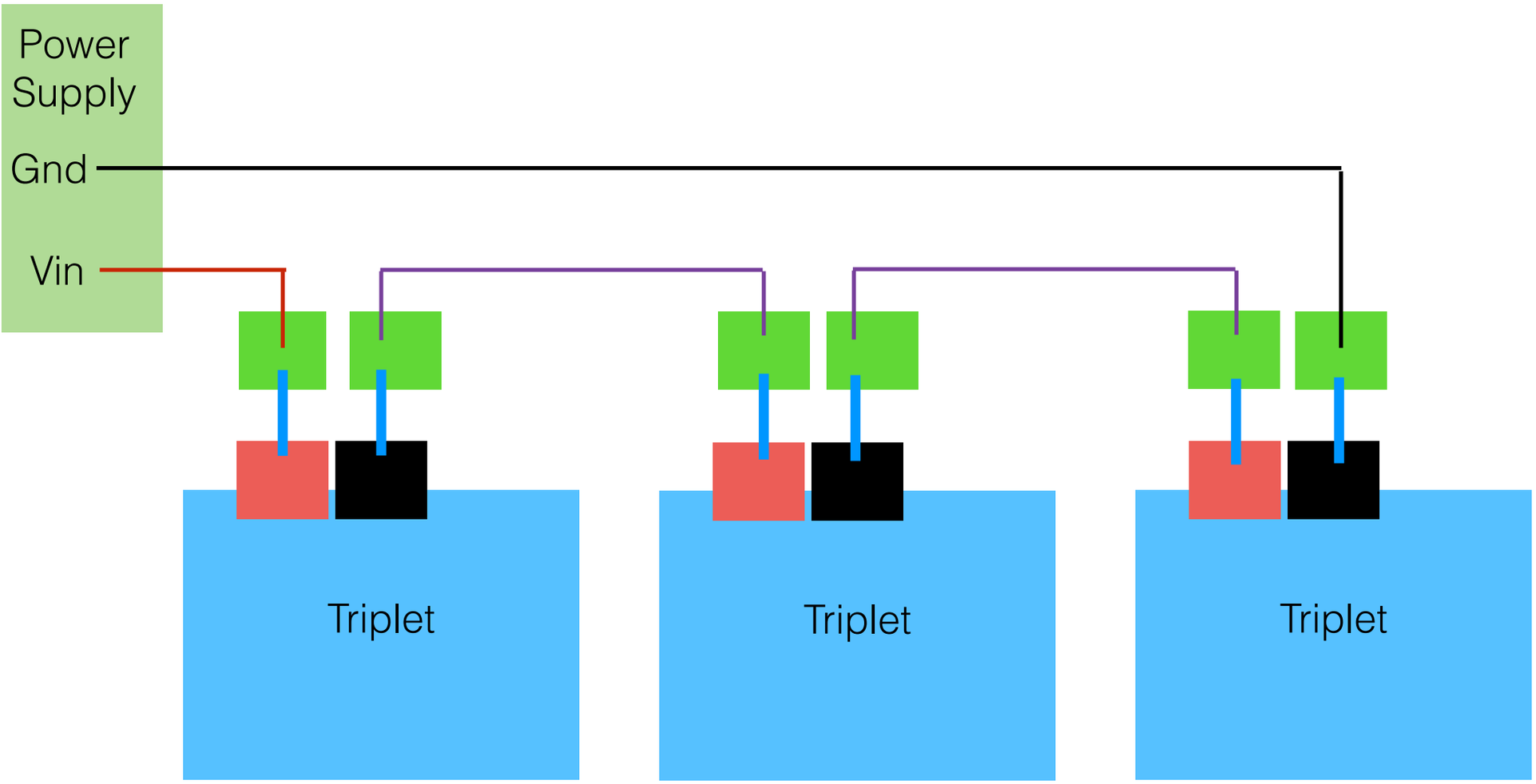
Preparing the flex before assembly

- Iref trim
  - On hybrid, default value is 8
  - Want to add/remove the 0Ω resistors to set Iref trim based on wafer probing data
- VDDA pull-up resistor
  - Compare **VREF_A_Trim** at DAC count 16 with VDDA on hybrid after power-up
  - For the chip to start up, VDDA > 1.14 V
  - If this is lower, you need to add a pull-up resistor

Measured Start-up VDDA [Volts]	Pull-up Resistor Required?	Pull-up Resistor Value [kΩ]	Expected increase in Start-up VDDA [Volts]
<= 1.09	**Yes**	150	0.1
>1.09 and <= 1.14	**Yes**	300	0.05
> 1.14	**No**	n/a	N/a

D. Antrim slides

LV powering of SP chain



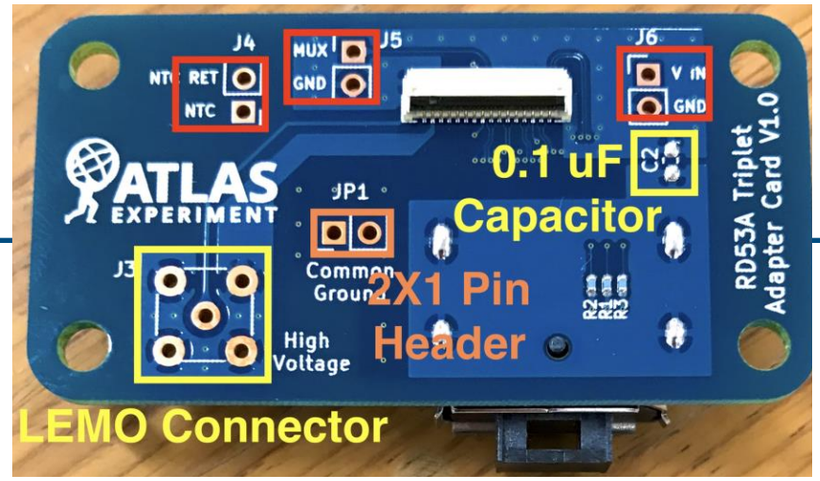
- To connect SP chain: ground of one triplet connected to power of other triplet
  - LV connector: Phoenix contact 0.200” pitch, 12-24 wire gauge
- SP chain operated at 3.3A with 5.5V voltage protection

Testing setup: DAQ

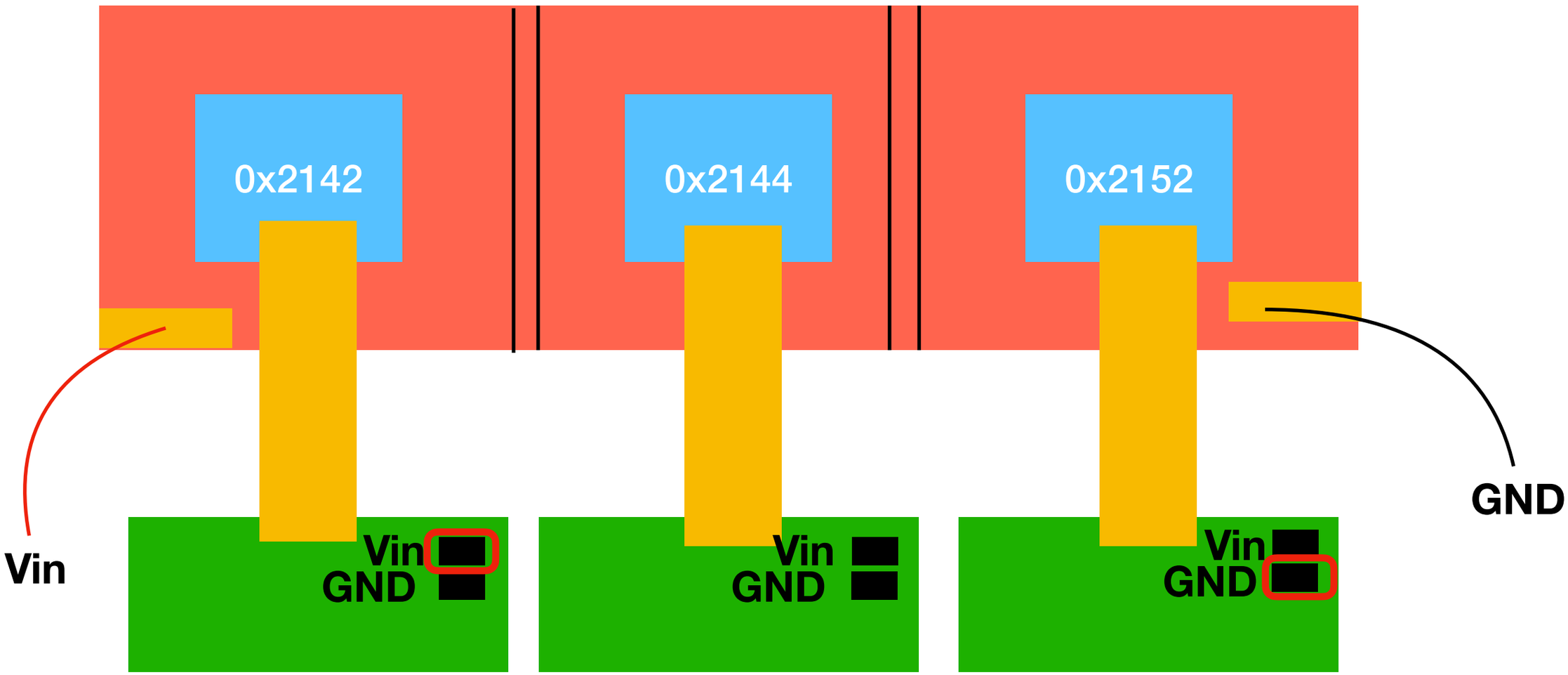
- Firmware: YARR-FW
  - Trenz TEF1001_R2
  - RX speed: 640 Mbps
  - Channel configuration: 4 DP adapter card (4x4)
- Readout: triplet adapter card
  - For easier routing, polarity of lines reversed
  - Need to make change in software
- Software: YARR (master branch)
  - configs/controller/specCfg.json

```
"txPolarity" : 15,
"rxPolarity" : 65535
```

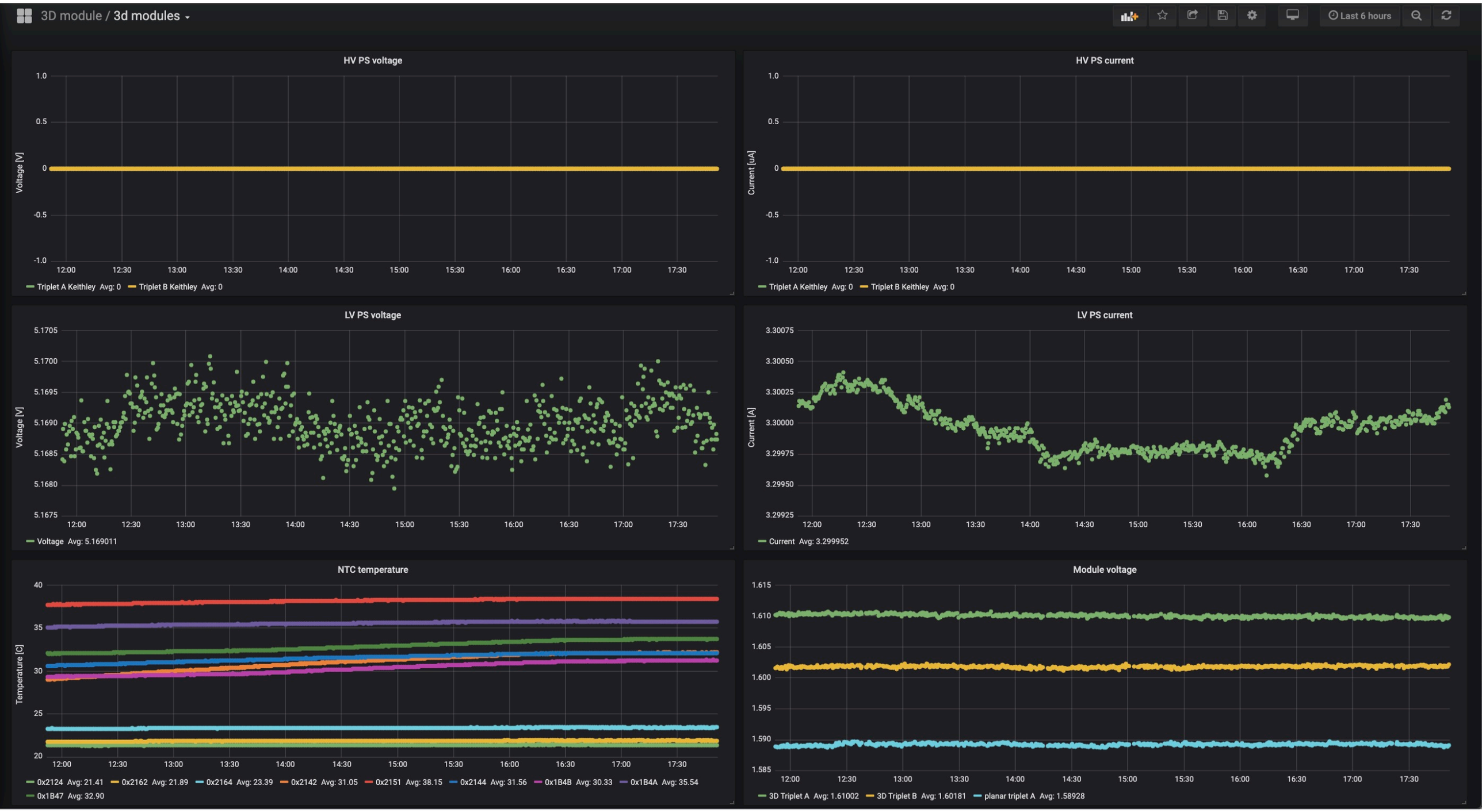
Environmental monitoring



- LV and HV PS voltage and current
- FE temperature:
  - measure NTC on triplet adapter card
- Module voltage: measure Vin and GND on adapter card



SP chain monitoring

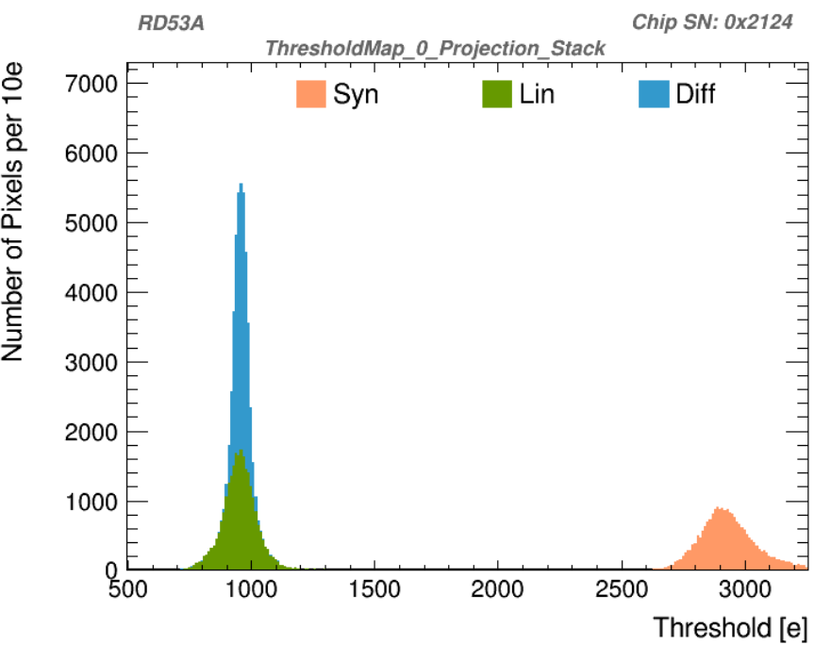


- Software interlock on FE temperature, module voltage, HV PS current

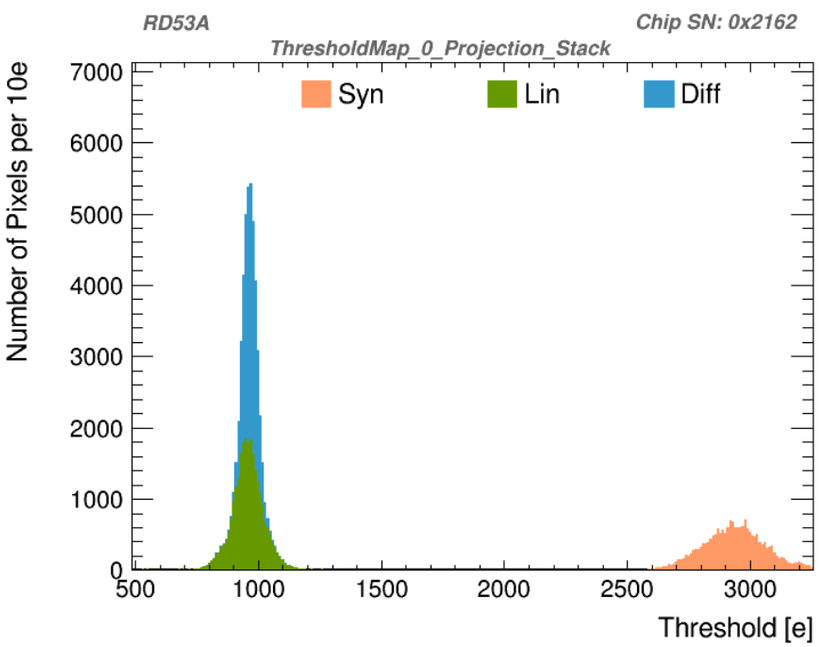
FE electrical tests

- FE chips were tested in SLDO
- We have successfully run scans: digital, analog, threshold
- Tuning: 1000e for digital and linear FEs, 3000e for synchronous FE
  - Sync FE has higher threshold to minimize noise on diff/lin FE
- Tests summarized in our [testing document]

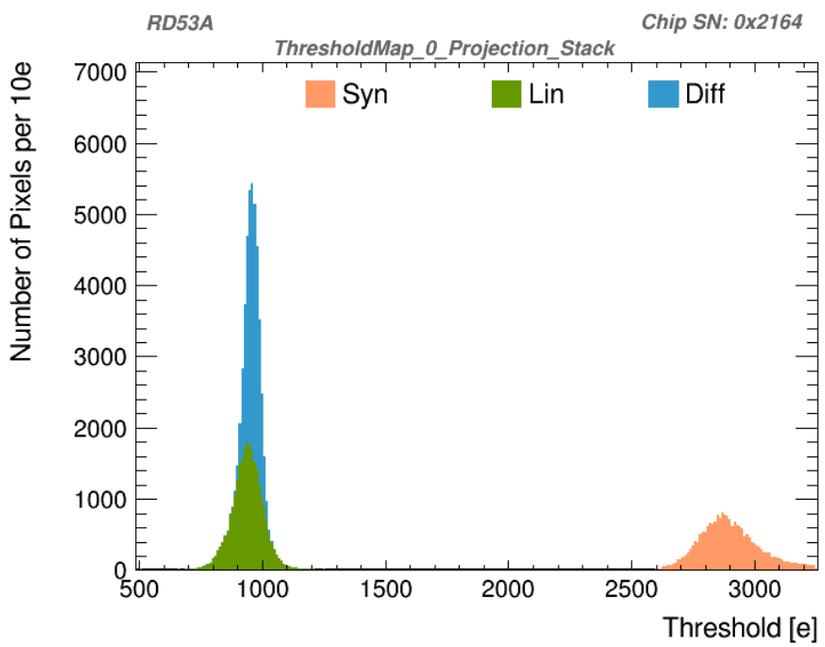
0x2124



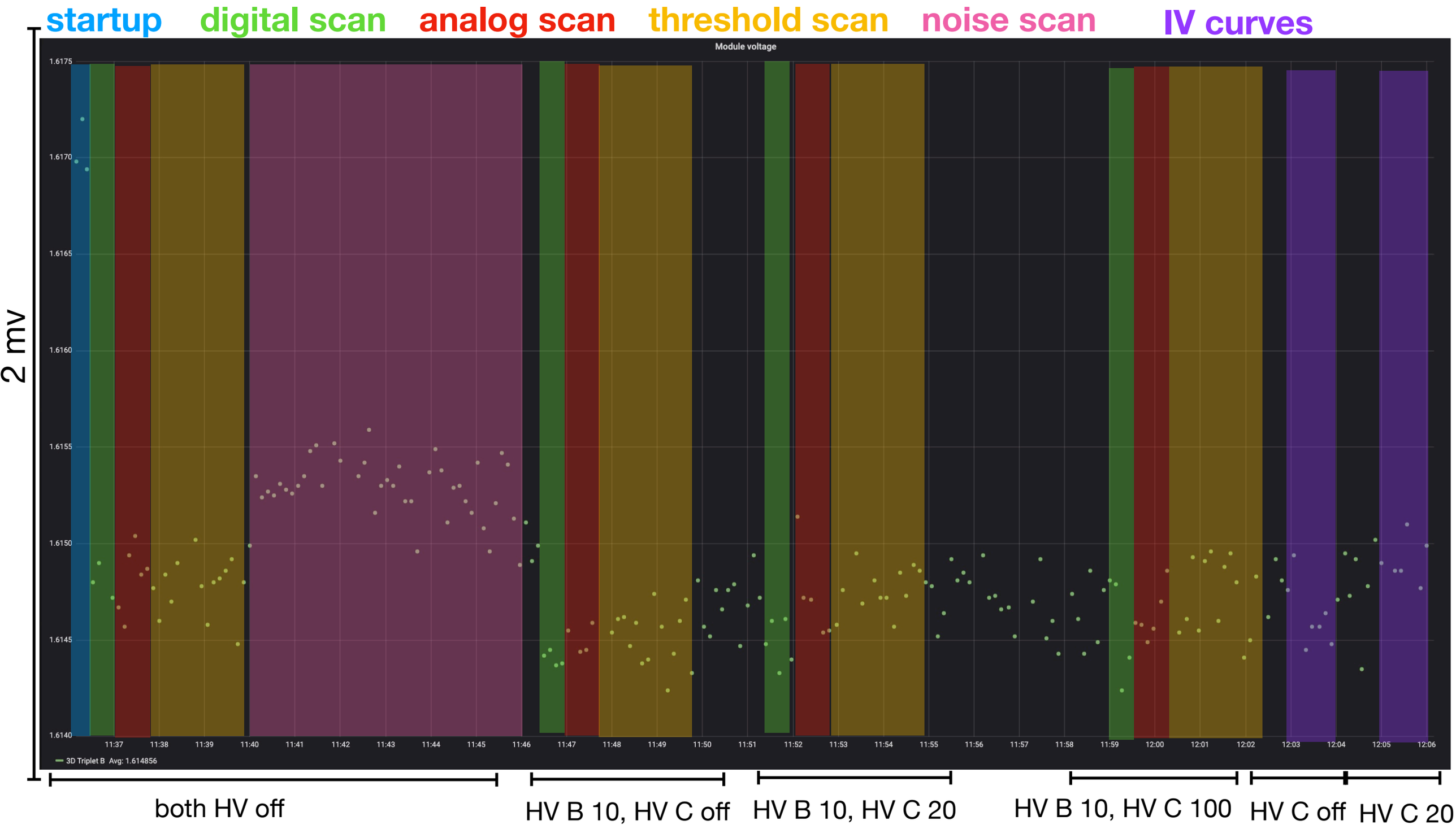
0x2162



0x2164

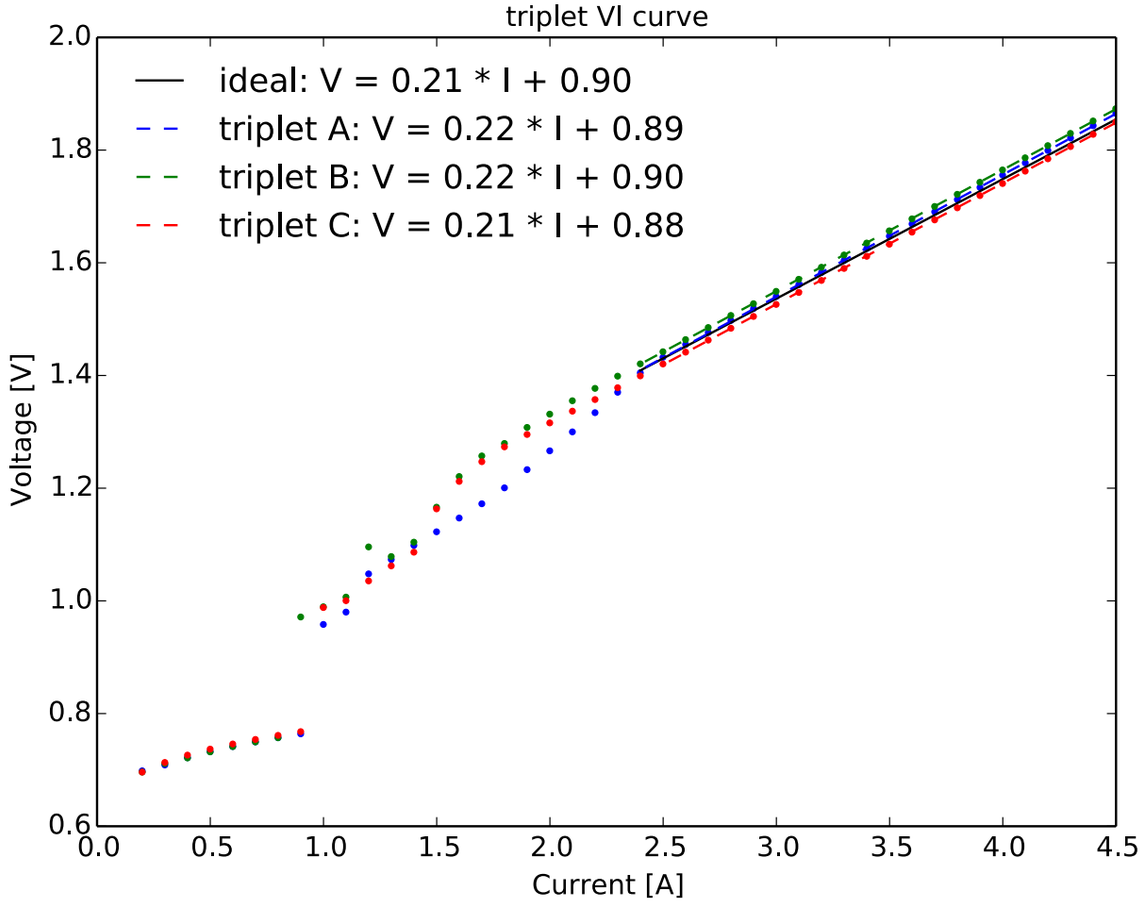


Impact on FE module voltage



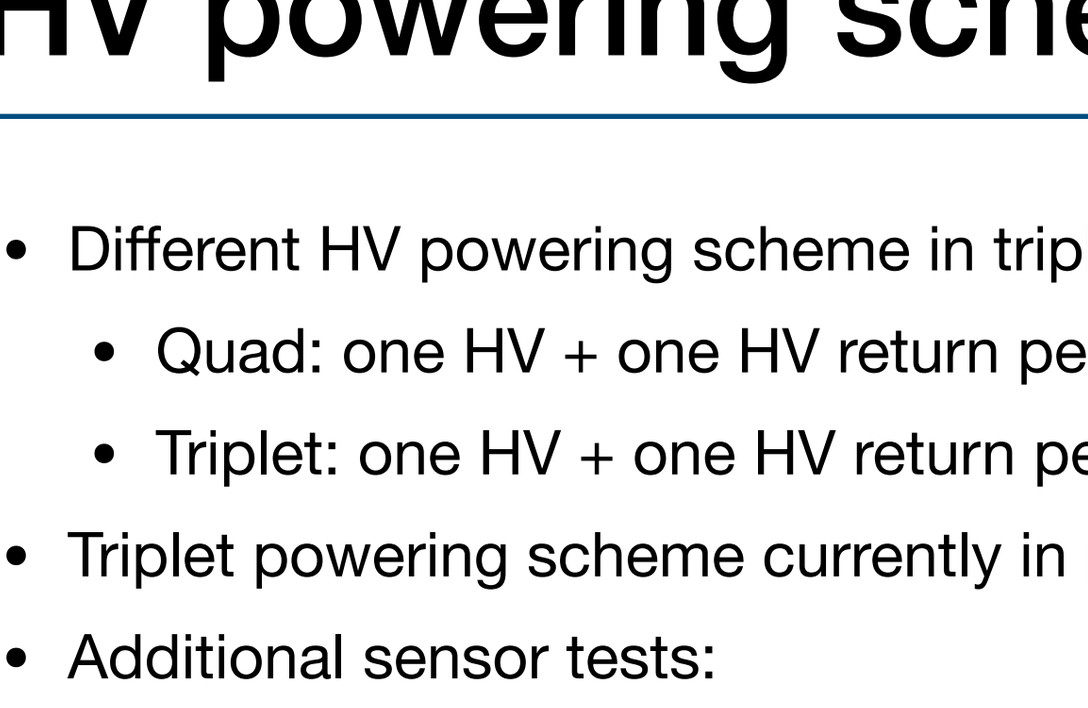
Triplet VI curves

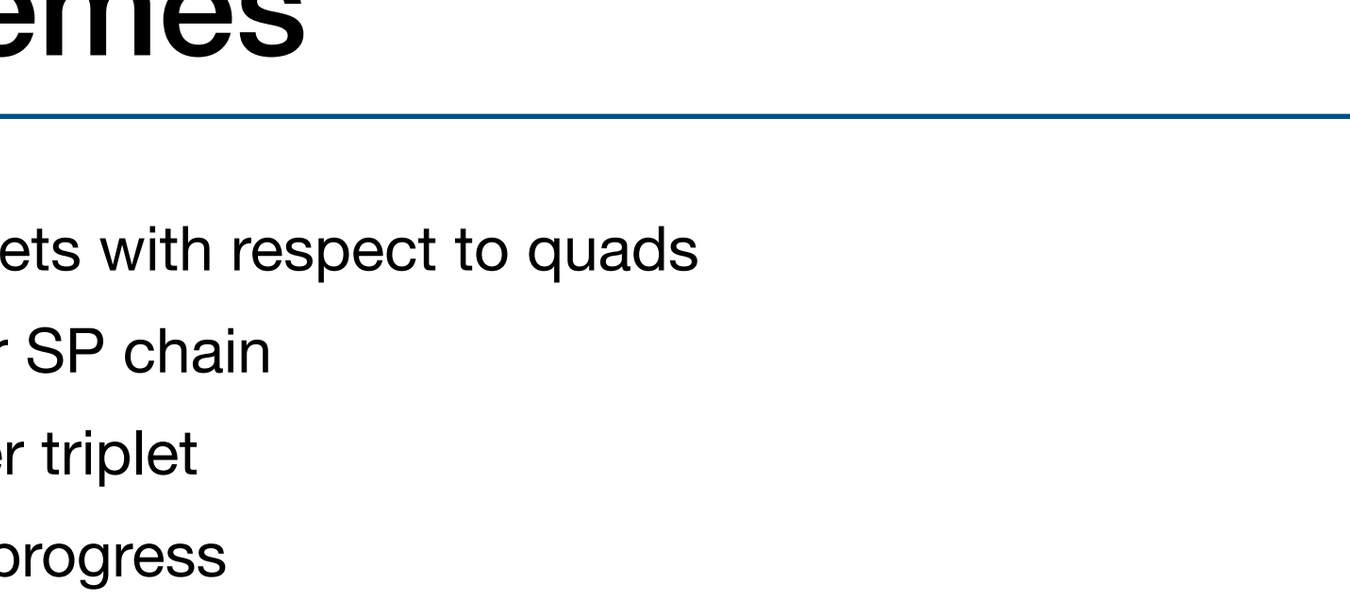
- Voltage measured on triplet adapter card, current is measured on PS
- Ramp down from 4.5 A to 0.1 A in 0.1 steps with power cycle
- Theoretical curve also shown: offset is 0.9V, slope calculated as 0.21 Ω from operational point 1.6V at 3.3A
- Triplet and theoretical VI curves compatible



HV powering schemes

- Different HV powering scheme in triplets with respect to quads
  - Quad: one HV + one HV return per SP chain
  - Triplet: one HV + one HV return per triplet
- Triplet powering scheme currently in progress
- Additional sensor tests:
  - disconnected bump scan
  - source scan with AM 241

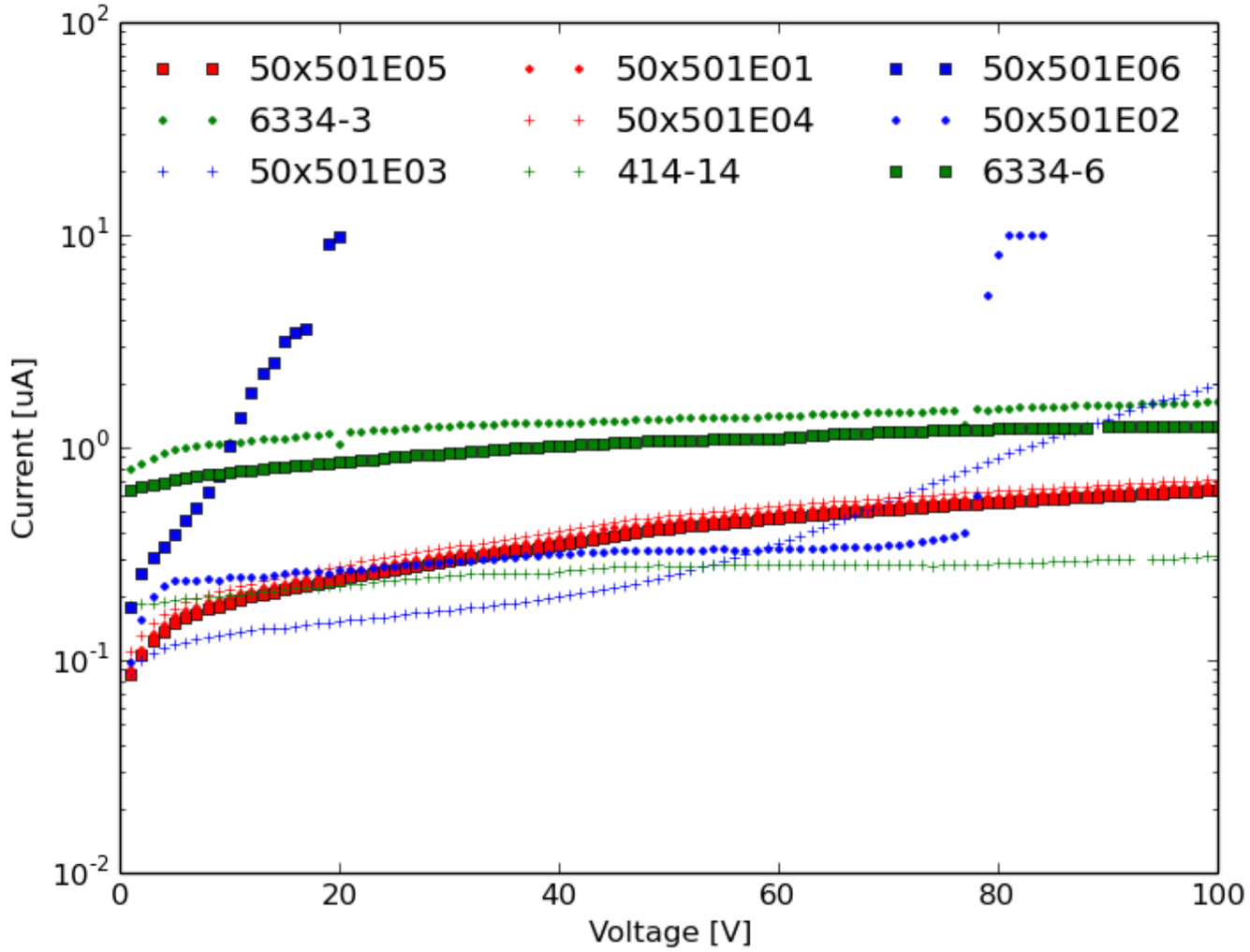




M. Hamer ITk Pixel Services PDR

Module HV IV curve

- 3D sensors shown in red and blue, planar sensors in green
- One of the 3D sensors reaches breakdown such earlier than others
- Nominal HV is 20 V but for the one that breaks down early, will operate at 10 V

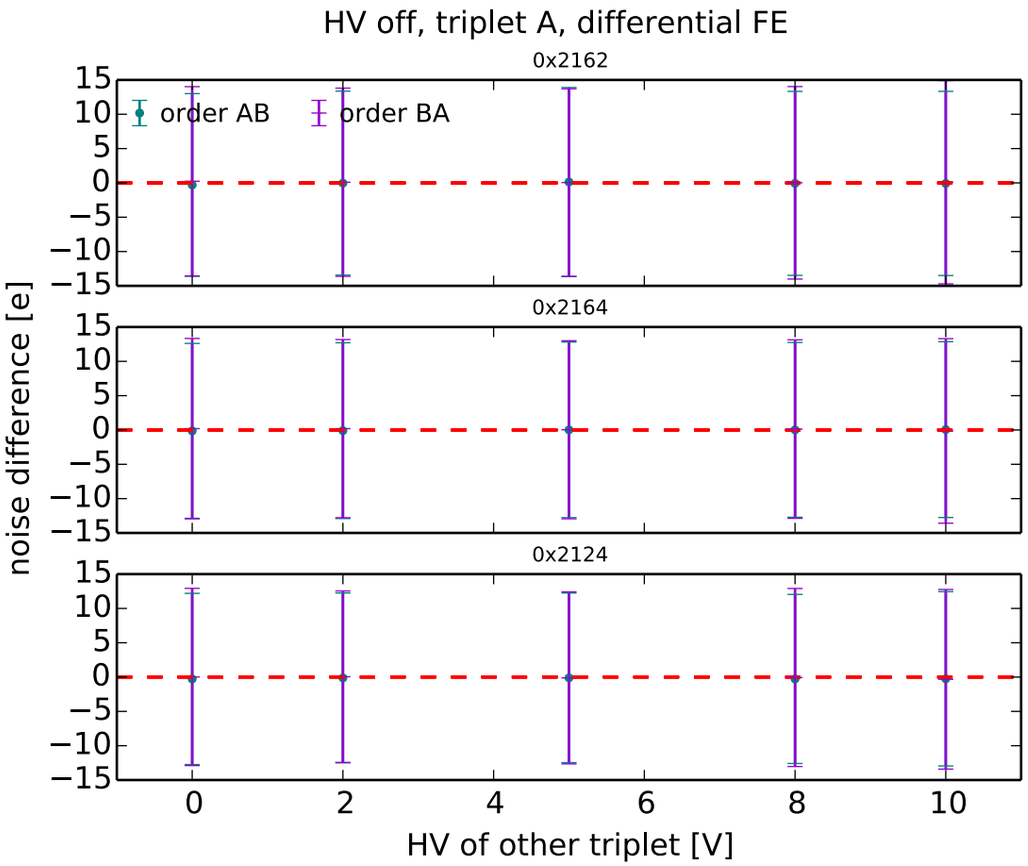


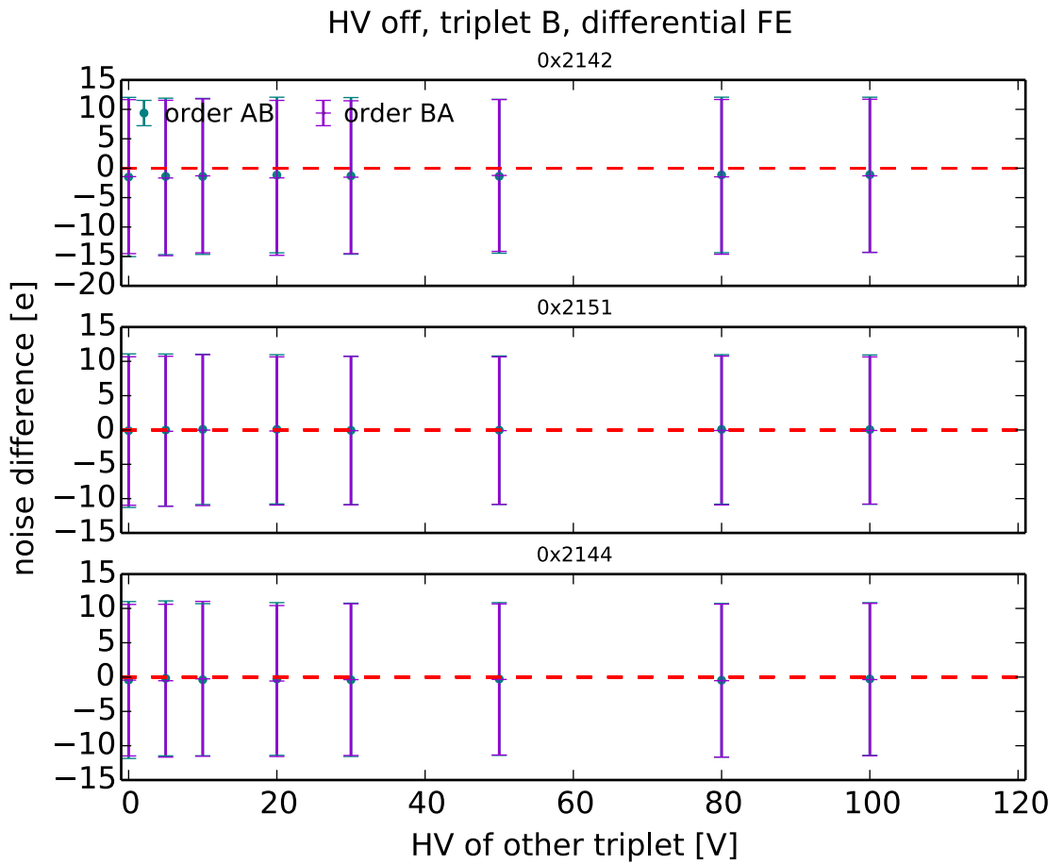
SP chain tests with HV

# triplets	LV status	HV of other triplets
1	off	N/A
1	on	N/A
2	off	off
2	off	on at constant V
2	off	vary V
2	on	off
2	on	at constant V
2	on	vary V

- Add additional triplets
- Vary position in the chain
- Additional figure of merit: threshold noise

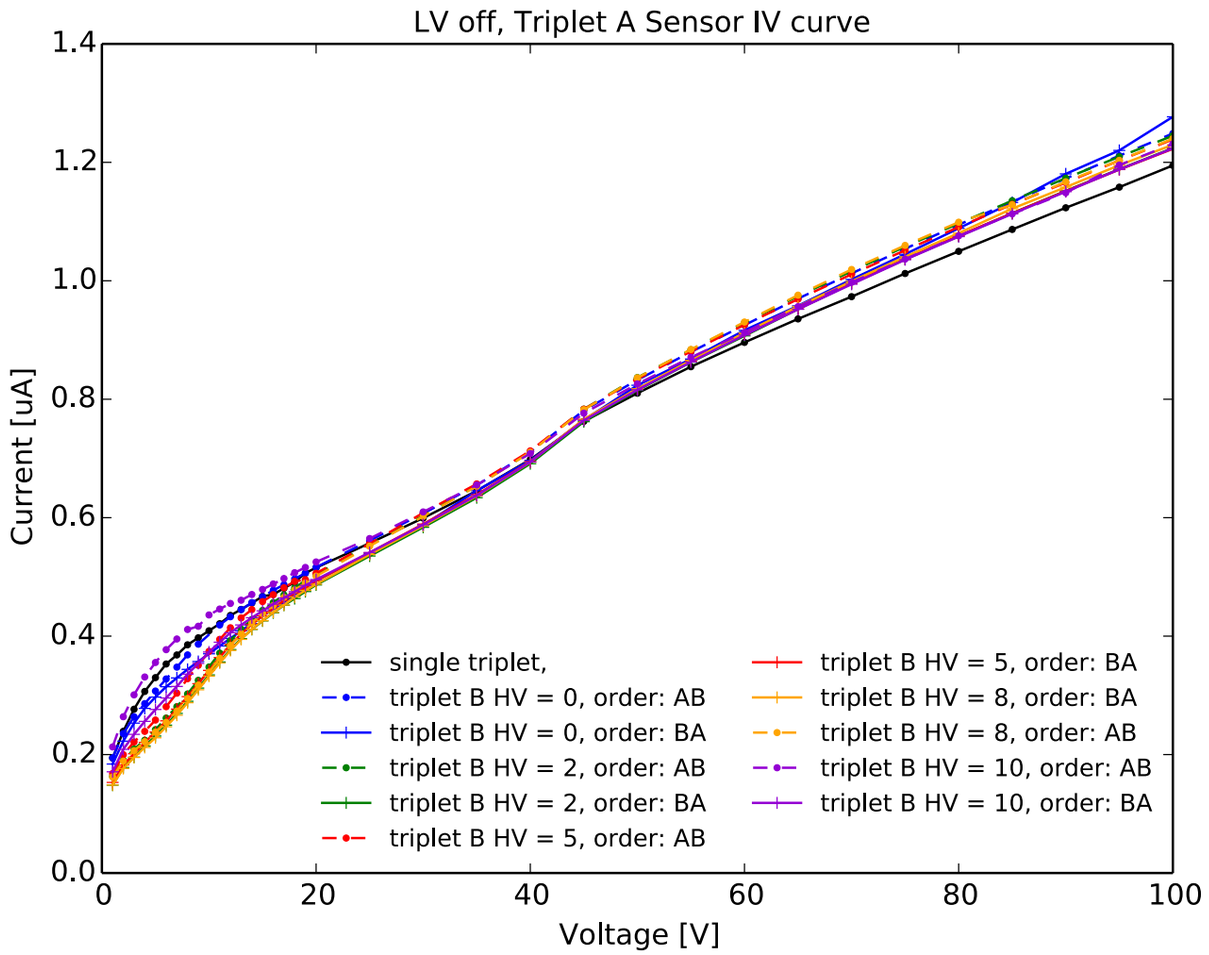
SP test results with HV





- Compare pixel-by-pixel noise when triplet is by itself or in chain
  - Vary other triplet HV
- Order of triplet does not impact pixel noise difference
- No trend as function of HV of other triplet

IV curves



- Take IV curve when changing HV of other triplet
- Shown when Triplet A is first in chain, and second
- No trend currently seen

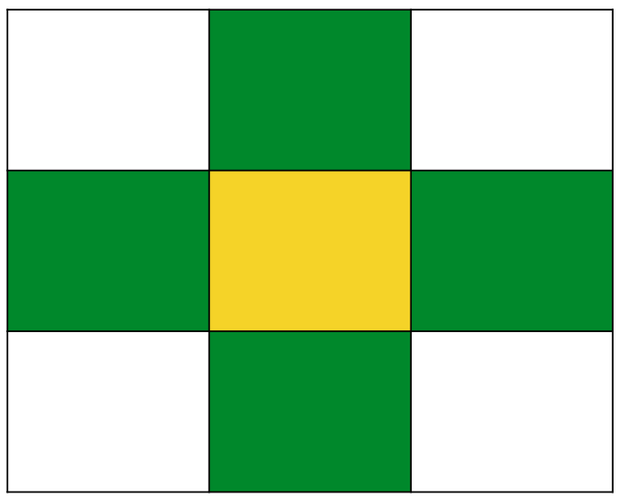
Conclusion

- We have assembled 3 triplets: 2 with 3D sensors, 1 with planar sensors
- Able to successfully run scans
- We have done additional tests on sensors
  - source scan, disconnected bump scan
- HV testing currently in progress
- Next steps:
  - Finalize 2 and 3 module HV tests
  - Assemble 2 additional triplets: 1 with planar, 1 with 3D sensors

Backup

Sensor tests

- Some of the tests we conducted are:
  - Disconnected bump scan
    - Check cross-talk between neighboring pixels
    - Inject charge in neighboring pixels and measure threshold in central pixel
  - Source scan
  - HV IV curves



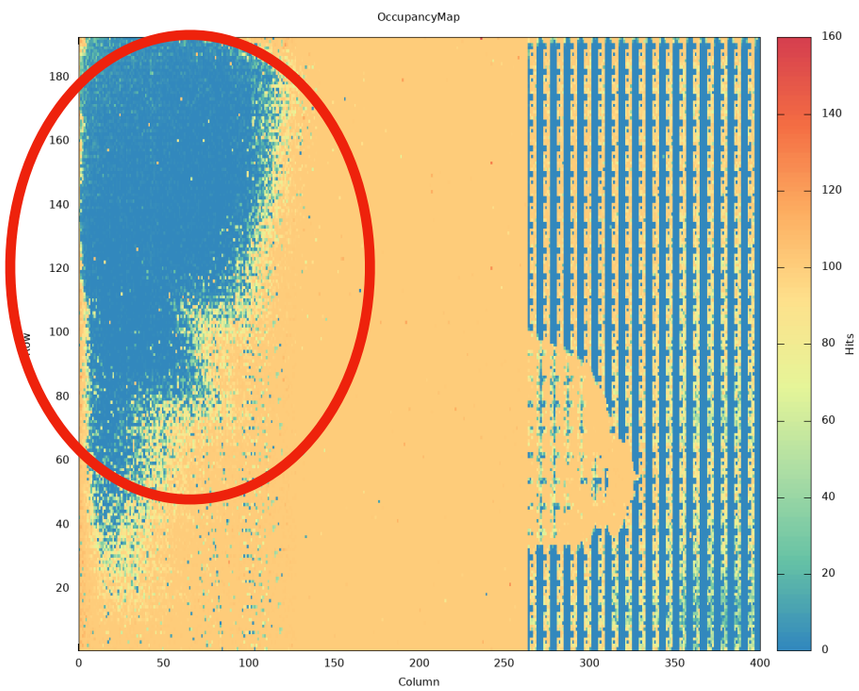
Method:
Inject charge in neighbouring pixels
Measure threshold for central pixel

Charge injected in each neighbor for which 50% of the injections results in a hit in the central pixel

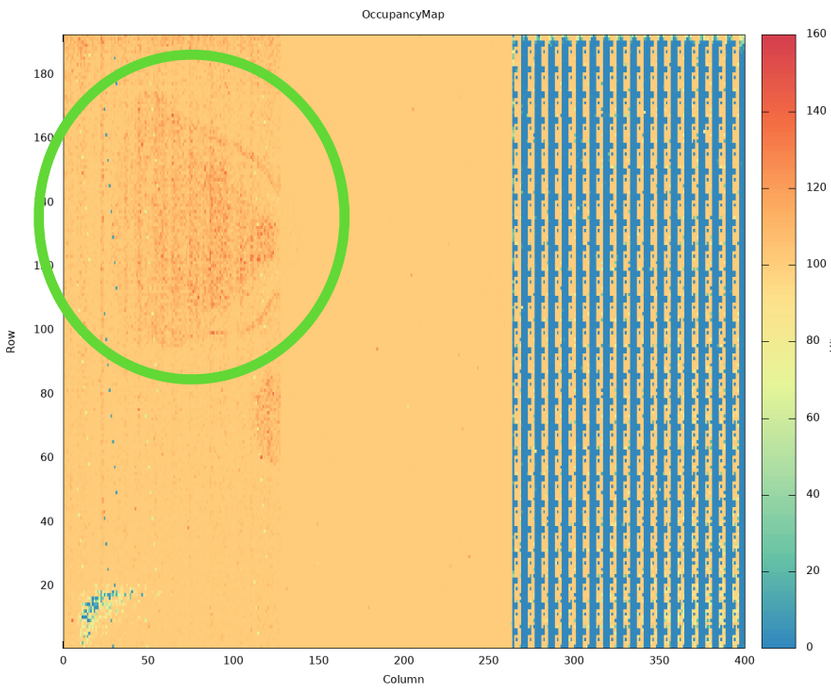
E.Pianori

Disconnected bump scan results

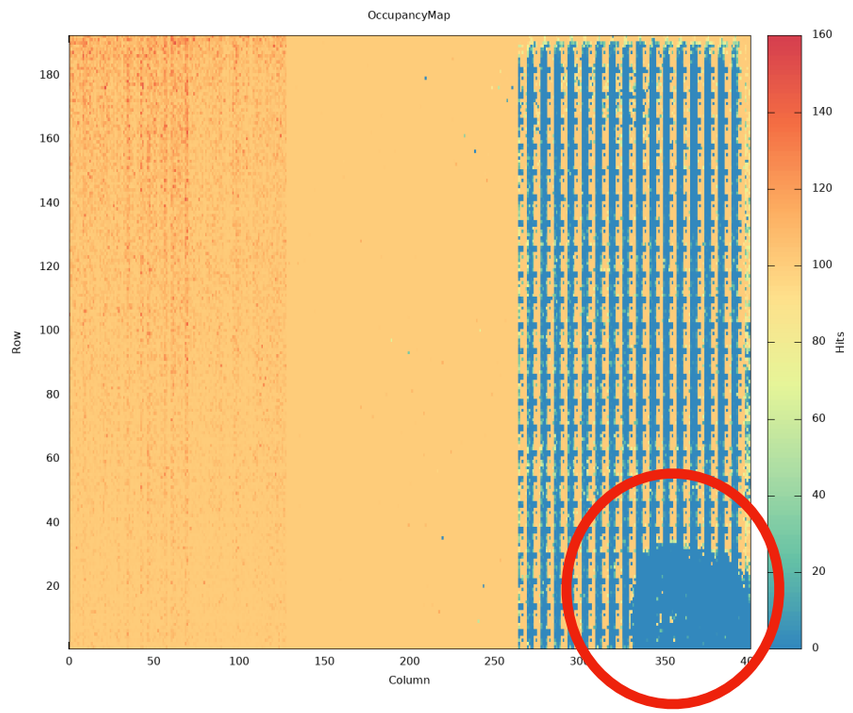
0x2162



0x2164



0x2124

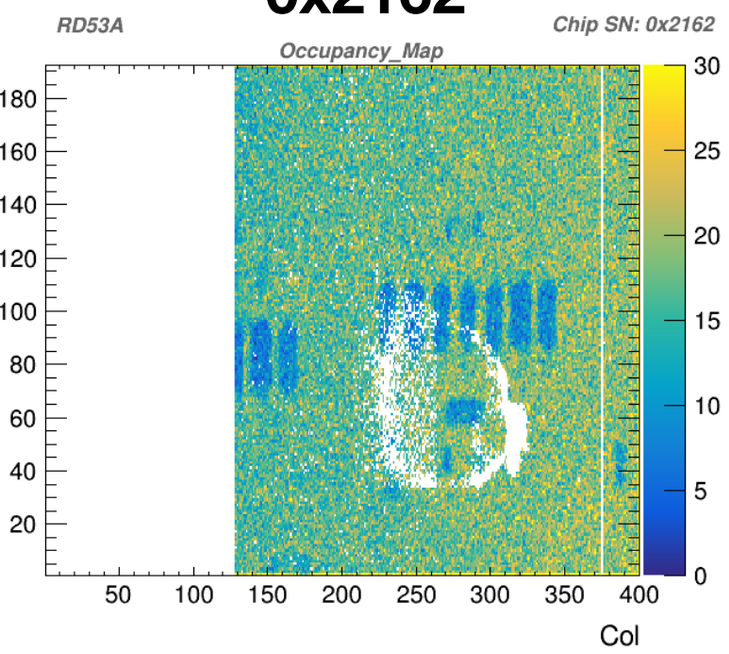


- Scan performed in SLDO at 3.3A CC for LV
- Injection is 4000 DAC in each pixel
- See some disconnected pixels
  - Diff FE in 0x2124
  - syn FE in 0x2162

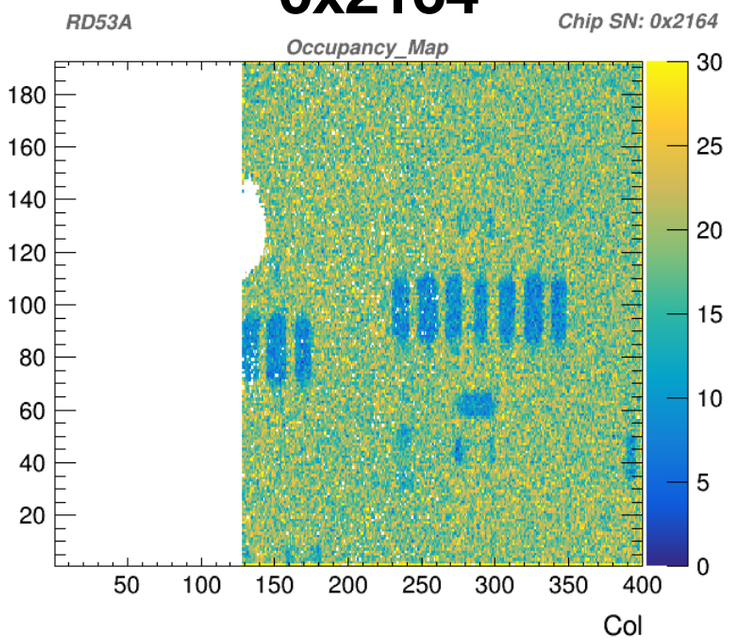
Source scan results

- Scan performed in SLDO at 3.3A CC for LV, and at 20V for HV
  - Chips did not have active cooling during this scan
- Disabled synchronous FE because of read errors
- Ran for 5 hours at 30k trigger frequency, HV at 20V
- Source: Am-241

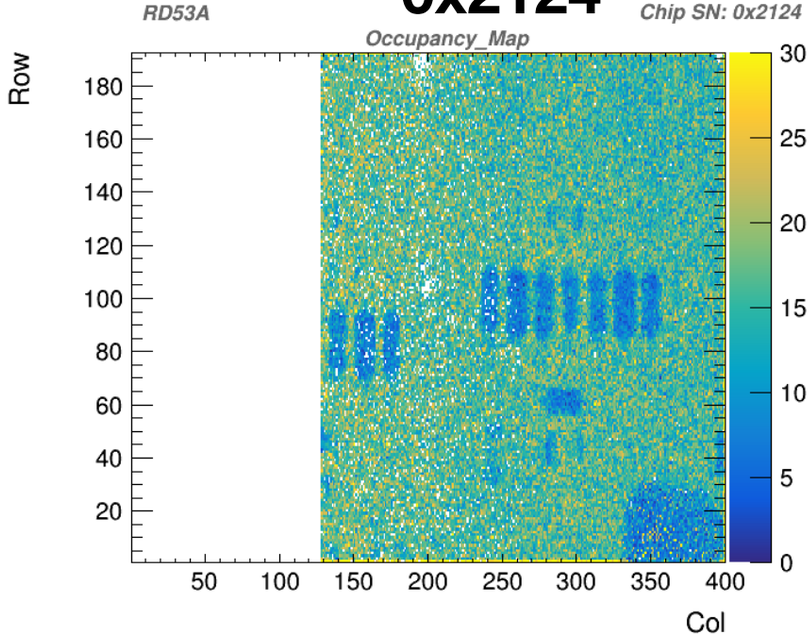
0x2162



0x2164



0x2124

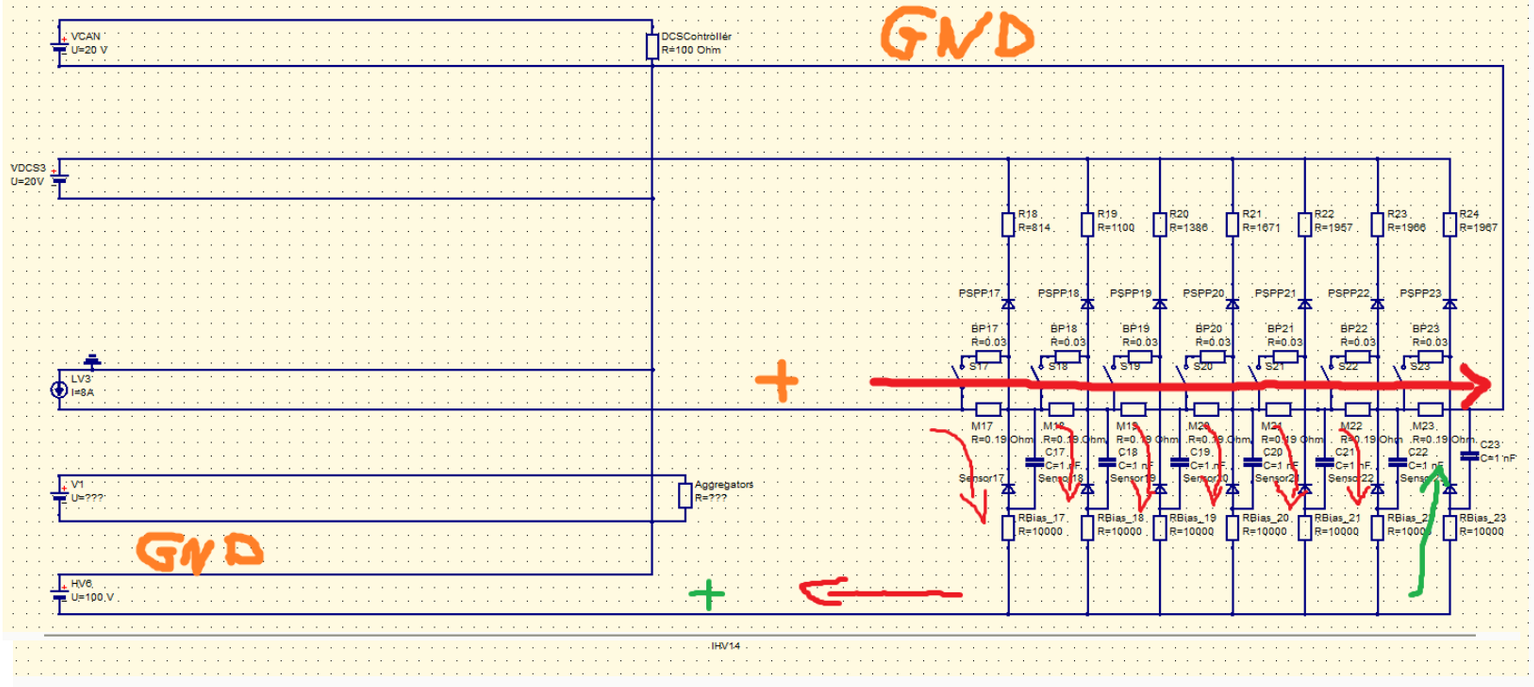


Tests from FEI4

UNIVERSITÄT BONN

HV DISTRIBUTION TESTS

- so far we could only test with two separate HV lines
  - our HV power supply is high-ohmic when off - O(MOhms)
  - this generates a forward bias on the sensors with the lowest local module ground (several 100mV)
  - voltage drop should depend on radiation levels – might become an issue for irradiated sensors



VDCS [V]	LV [V]	RHV [Ohms]	VHV57 [V]	VHV14 [V]
20,0	0,0	6,8M	0,0064	0,032
20,0	12,9	6,8M	7,0000	0,336
20,0	0,0	10k	0,0005	0,0058
20,0	12,9	10k	0,0460	0,0705
20,0	0,0	open	0,1930	0,032
20,0	12,9	open	9,0000	0,337
0,0	0,0	any	0,0000	0

Tests from FEI4

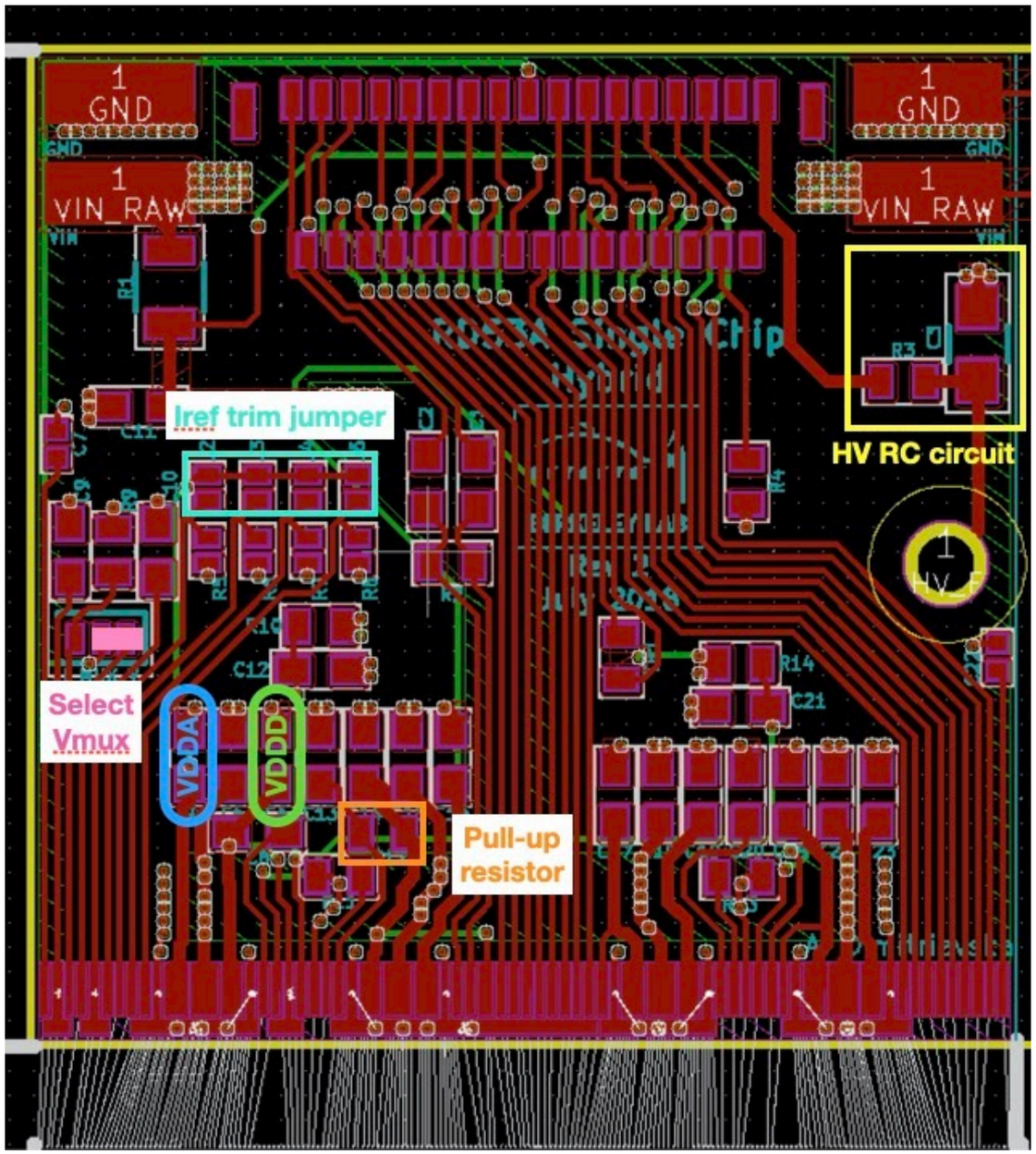
UNIVERSITÄT BONN

HV DISTRIBUTION TESTS

- significant forward current through module with lowest ground potential
  - on our prototype: **> 95% of the leakage current** generated through LV is returned through last sensor
  - up to 30uA with our sensors but only 5 modules connected
- extrapolation to final detector: < **2.2mA** per sensor, up to 7 modules per HV lines
  - forward current through last sensor: < **15mA**

Module	Voltage Drop [V]	R_HV [Ohms]	Vglobal [V]	Vsensor [V]	Drop over R_HV [V]	ISensor [uA]
BM1	2.12	11000	0.701	0.368	0.333	30.27272727
BM2	1.78	10000	0.701	0.724	-0.023	-2.3
BM3	1.95	11000	0.701	0.92	-0.219	-19.90909091
BM4	1.99	11000	0.701			
BM5	2	11000	0.701			
BM6	2	11000	0.701	0.742	-0.041	-3.727272727
BM7	2.01	11000	0.701	0.754	-0.053	-4.818181818

Regulator and start-up checks



- Before testing the triplet, you want to check wafer probing data:
  - Iref trim
  - Regulator voltages (digital and analog)
- Regulator voltages are also measured on the hybrid after powering-up the triplet across capacitors
- To use the MUX, need to add solder jumper to select either Vmux or Imux
- Link
  - Hybrid design
  - Wafer probing data

Wafer probing data: Iref trim

- Each wafer probing directory contains *yaml files for each chip
- For Iref trim, we want to select the value that gives a current closest to 4 μA
- Because we operate in shunt mode, it was found that chip performs better if we add 1 to the Iref trim

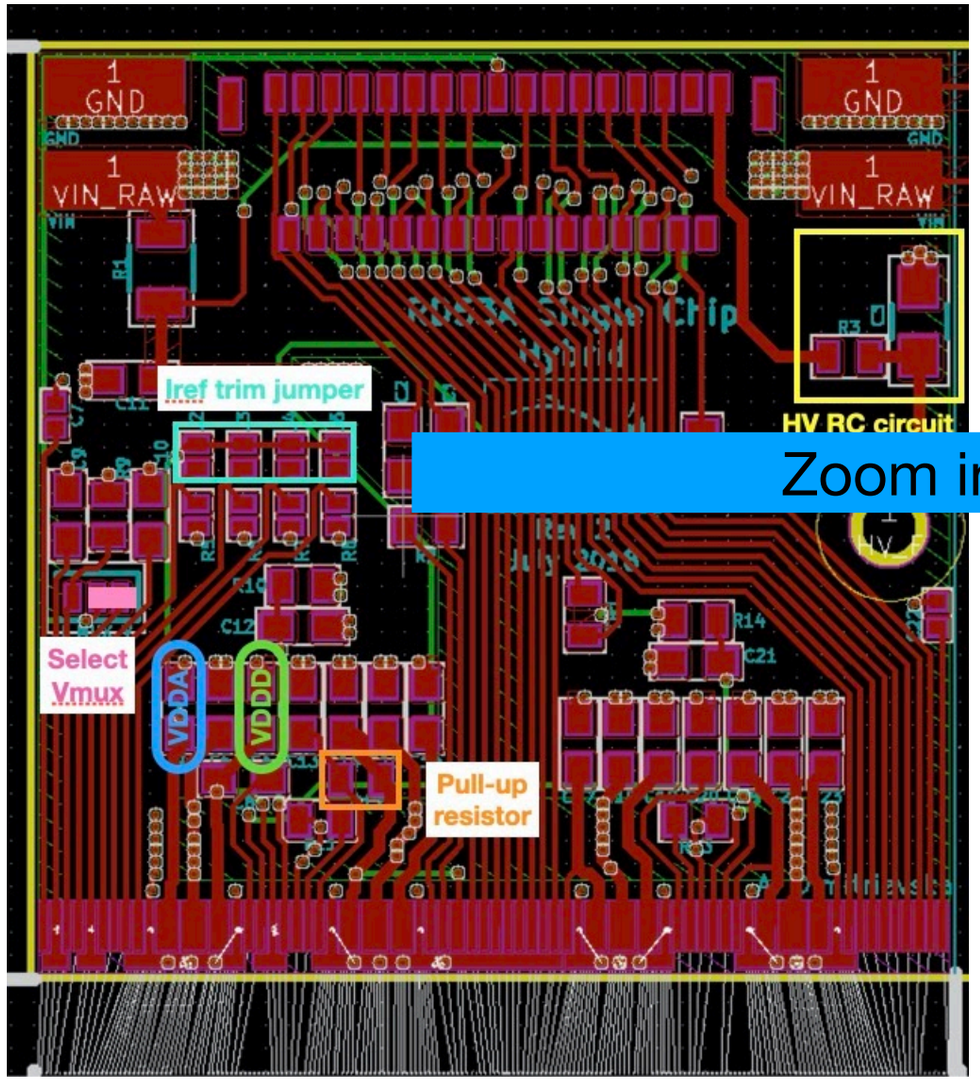
number correspond to Iref trim values →

```
IREF Trims:
  0: {IREF: 3.144045e-06, V_IREF: 0.6669227}
  1: {IREF: 3.253034e-06, V_IREF: 0.666787}
  2: {IREF: 3.369074e-06, V_IREF: 0.666815}
  3: {IREF: 3.481429e-06, V_IREF: 0.6669157}
  4: {IREF: 3.631095e-06, V_IREF: 0.6668966}
  5: {IREF: 3.74201e-06, V_IREF: 0.6671047}
  6: {IREF: 3.855746e-06, V_IREF: 0.6670694}
  7: {IREF: 3.969401e-06, V_IREF: 0.6664958}
  8: {IREF: 4.106614e-06, V_IREF: 0.6667546}
  9: {IREF: 4.219549e-06, V_IREF: 0.6661047}
 10: {IREF: 4.336516e-06, V_IREF: 0.6664795}
 11: {IREF: 4.444127e-06, V_IREF: 0.666697}
 12: {IREF: 4.591172e-06, V_IREF: 0.6663485}
 13: {IREF: 4.700222e-06, V_IREF: 0.6661149}
 14: {IREF: 4.821267e-06, V_IREF: 0.6663284}
 15: {IREF: 4.933665e-06, V_IREF: 0.6667639}
```

Iref trim value with current value closest to 4 μA is 7.
On the hybrid, we'll want to use 8 for Iref trim

Setting Iref trim on hybrid

- On hybrid, default value is 8
- Want to add/remove the 0Ω resistors to set Iref trim based on wafer probing data
  - Trim bit values are in binary



Zoom in

Wafer probing data: regulator voltages

- At power-on, the RD53a chip has its SLDO in it's default configuration with the digital and analog SLDO having default trim bits of **16**
- In YARR, the SLDO trim bits correspond to the configuration parameters **SldoAnalogTrim** and **SldoDigitalTrim**
- In the wafer probing *.yaml files, the measurements of the analog and digital SLDO output for each trim setting are reported under **VREF_A_Trim** and **VREF_D_Trim**, respectively:

number correspond to DAC values →


```
VREF_A Trim:
  0: {VDDA: 1.018533, VOFF_A: 0.9070324, VREF_A: 0.5103052}
  1: {VDDA: 1.022953, VOFF_A: 0.9070191, VREF_A: 0.5125597}
  2: {VDDA: 1.030369, VOFF_A: 0.9070505, VREF_A: 0.5164187}
  3: {VDDA: 1.035326, VOFF_A: 0.9066169, VREF_A: 0.5189075}
  4: {VDDA: 1.04507, VOFF_A: 0.906543, VREF_A: 0.523919}
  5: {VDDA: 1.049288, VOFF_A: 0.9067903, VREF_A: 0.5262678}
  6: {VDDA: 1.057514, VOFF_A: 0.9063674, VREF_A: 0.5301982}
  7: {VDDA: 1.062641, VOFF_A: 0.9058853, VREF_A: 0.5328553}
  8: {VDDA: 1.077309, VOFF_A: 0.9059466, VREF_A: 0.5401213}
  9: {VDDA: 1.082902, VOFF_A: 0.9060893, VREF_A: 0.5432163}
  10: {VDDA: 1.091954, VOFF_A: 0.9054234, VREF_A: 0.5478457}
  11: {VDDA: [illegible] 0.5504239}
  12: {VDDA: [illegible] 0.5567517}
  13: {VDDA: [illegible] 0.5598487}
  14: {VDDA: 1.125608, VOFF_A: 0.9062269, VREF_A: 0.5648918}
  15: {VDDA: 1.131922, VOFF_A: 0.9056846, VREF_A: 0.5675926}
  16: {VDDA: 1.154496, VOFF_A: 0.9057477, VREF_A: 0.5790662}
  17: {VDDA: 1.161619, VOFF_A: 0.9055507, VREF_A: 0.5828208}
  18: {VDDA: 1.173328, VOFF_A: 0.9049987, VREF_A: 0.5888944}
  19: {VDDA: 1.180744, VOFF_A: 0.9054824, VREF_A: 0.5924013}
  20: {VDDA: 1.197525, VOFF_A: 0.9052626, VREF_A: 0.6008514}
  21: {VDDA: 1.205692, VOFF_A: 0.9055315, VREF_A: 0.6050378}
  22: {VDDA: 1.219769, VOFF_A: 0.9046063, VREF_A: 0.6122254}
  23: {VDDA: 1.227727, VOFF_A: 0.9053088, VREF_A: 0.6162809}
  24: {VDDA: 1.254337, VOFF_A: 0.904568, VREF_A: 0.6297991}
  25: {VDDA: 1.263878, VOFF_A: 0.9052342, VREF_A: 0.634298}
  26: {VDDA: 1.279223, VOFF_A: 0.9057688, VREF_A: 0.6429804}
  27: {VDDA: 1.289526, VOFF_A: 0.9047325, VREF_A: 0.647708}
  28: {VDDA: 1.31278, VOFF_A: 0.9045956, VREF_A: 0.6591957}
  29: {VDDA: 1.323432, VOFF_A: 0.9047868, VREF_A: 0.6648428}
  30: {VDDA: 1.342647, VOFF_A: 0.9048601, VREF_A: 0.6746827}
  31: {VDDA: 1.354556, VOFF_A: 0.9050272, VREF_A: 0.6804764}
```

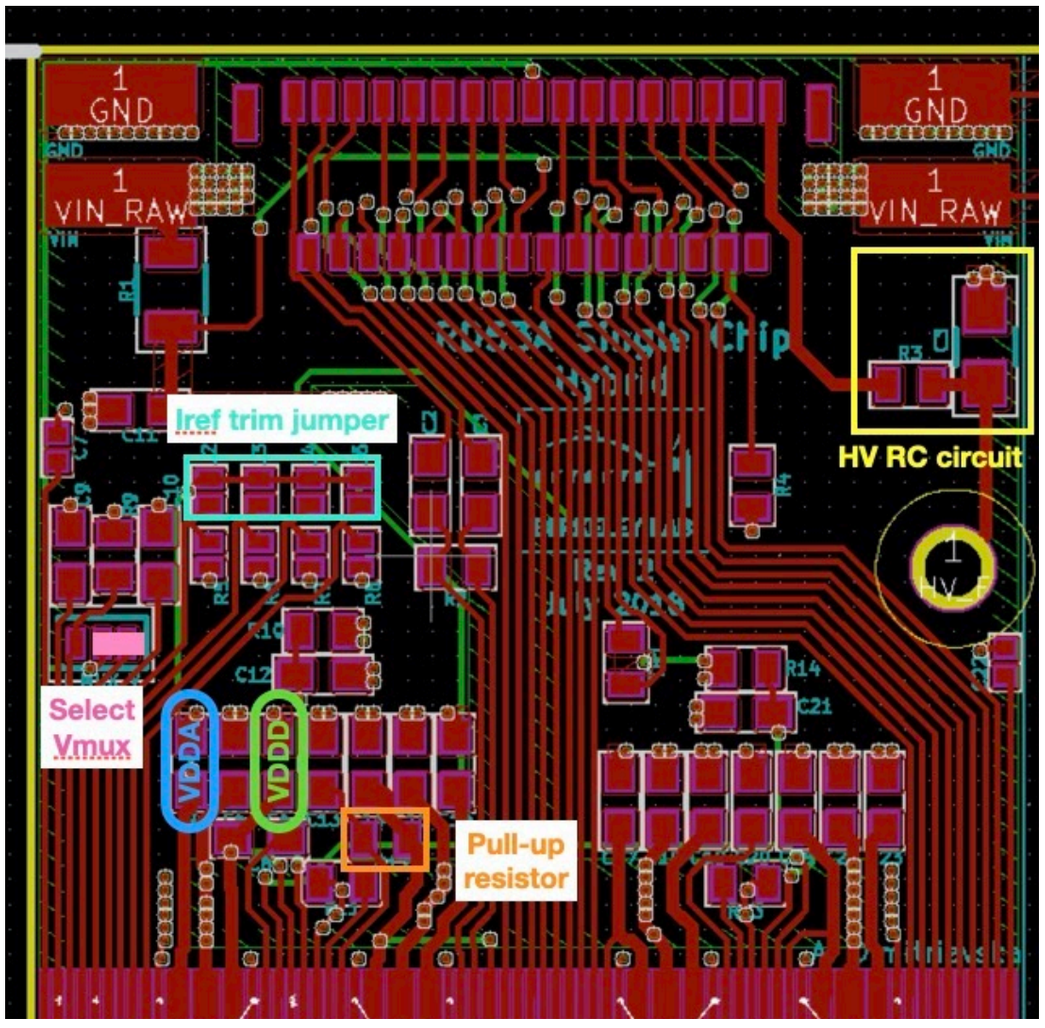

startup value for VDDA


```
VREF_D Trim:
  0: {VDDD: 0.9934641, VOFF_D: 0.9990975, VREF_D: 0.4951289}
  1: {VDDD: 0.9972245, VOFF_D: 0.9986598, VREF_D: 0.4970863}
  2: {VDDD: 1.004494, VOFF_D: 0.9984533, VREF_D: 0.5006848}
  3: {VDDD: 1.008257, VOFF_D: 0.9983525, VREF_D: 0.5027463}
  4: {VDDD: 1.017864, VOFF_D: 0.9987476, VREF_D: 0.5075653}
  5: {VDDD: 1.022657, VOFF_D: 0.9982619, VREF_D: 0.510017}
  6: {VDDD: 1.030928, VOFF_D: 0.9985507, VREF_D: 0.5138711}
  7: {VDDD: 1.035493, VOFF_D: 0.9989482, VREF_D: 0.5162954}
  8: {VDDD: 1.049754, VOFF_D: 0.9988426, VREF_D: 0.5234905}
  9: {VDDD: 1.054414, VOFF_D: 0.9988818, VREF_D: 0.5263705}
  10: {VDDD: 1.064243, VOFF_D: 0.9989094, VREF_D: 0.5305927}
  11: {VDDD: [illegible] 0.5333377}
  12: {VDDD: [illegible] 0.5396748}
  13: {VDDD: [illegible] 0.5424991}
  14: {VDDD: 1.097448, VOFF_D: 0.9983519, VREF_D: 0.5474769}
  15: {VDDD: 1.103397, VOFF_D: 0.998573, VREF_D: 0.5509237}
  16: {VDDD: 1.125662, VOFF_D: 0.9985086, VREF_D: 0.5617649}
  17: {VDDD: 1.131983, VOFF_D: 0.9987863, VREF_D: 0.5652292}
  18: {VDDD: 1.143922, VOFF_D: 0.9984263, VREF_D: 0.571155}
  19: {VDDD: 1.151066, VOFF_D: 0.9983381, VREF_D: 0.5749587}
  20: {VDDD: 1.168113, VOFF_D: 0.9982512, VREF_D: 0.5831398}
  21: {VDDD: 1.175663, VOFF_D: 0.9976604, VREF_D: 0.5869958}
  22: {VDDD: 1.189629, VOFF_D: 0.9976473, VREF_D: 0.5941311}
  23: {VDDD: 1.198125, VOFF_D: 0.9975035, VREF_D: 0.5981321}
  24: {VDDD: 1.223857, VOFF_D: 0.9968192, VREF_D: 0.6115186}
  25: {VDDD: 1.233103, VOFF_D: 0.9972466, VREF_D: 0.616147}
  26: {VDDD: 1.248985, VOFF_D: 0.9973035, VREF_D: 0.6243595}
  27: {VDDD: 1.259705, VOFF_D: 0.9976007, VREF_D: 0.6292886}
  28: {VDDD: 1.28264, VOFF_D: 0.9974106, VREF_D: 0.6409526}
  29: {VDDD: 1.294902, VOFF_D: 0.9972229, VREF_D: 0.6468256}
  30: {VDDD: 1.313034, VOFF_D: 0.99708, VREF_D: 0.6567827}
  31: {VDDD: 1.324937, VOFF_D: 0.9964672, VREF_D: 0.6624079}
```


startup value for VDDD

Regulator voltage: pull-up resistor

- Compare **VREF_A_Trim** at DAC count 16 with VDDA on hybrid after power-up
  - VDDA is measured across a capacitor, circled in blue
- For the chip to start up, VDDA > 1.14 V
- If this is lower, you need to add a pull-up resistor

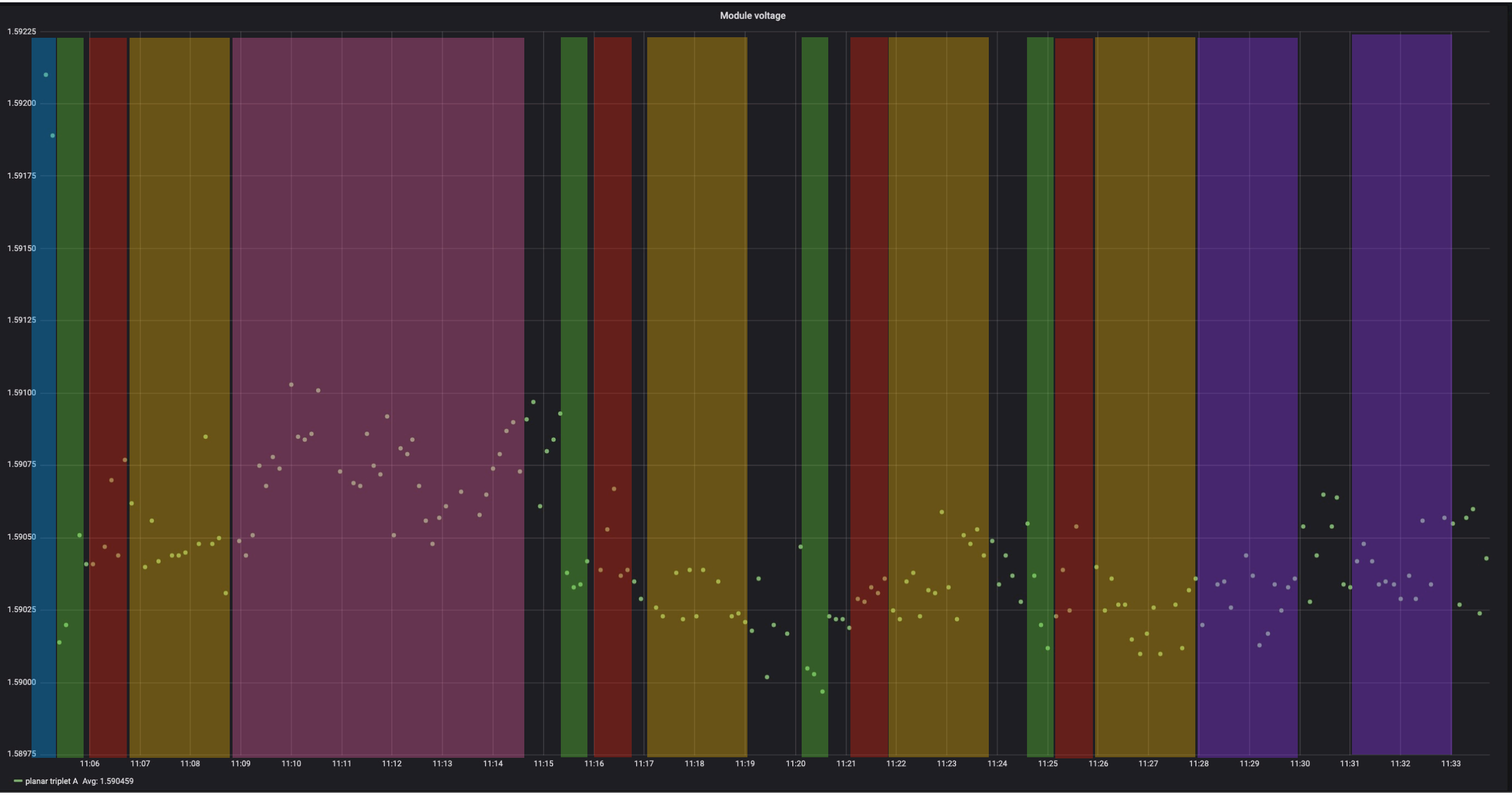


Measured Start-up VDDA [Volts]	Pull-up Resistor Required?	Pull-up Resistor Value [kΩ]	Expected increase in Start-up VDDA [Volts]
<= 1.09	**Yes**	150	0.1
>1.09 and <= 1.14	**Yes**	300	0.05
> 1.14	**No**	n/a	N/a

D. Antrim slides

Triplet C with planar sensor

startup digital scan analog scan threshold scan noise scan IV curves



both HV off

HV C @20
HV B off

HV C 20
HV B 10

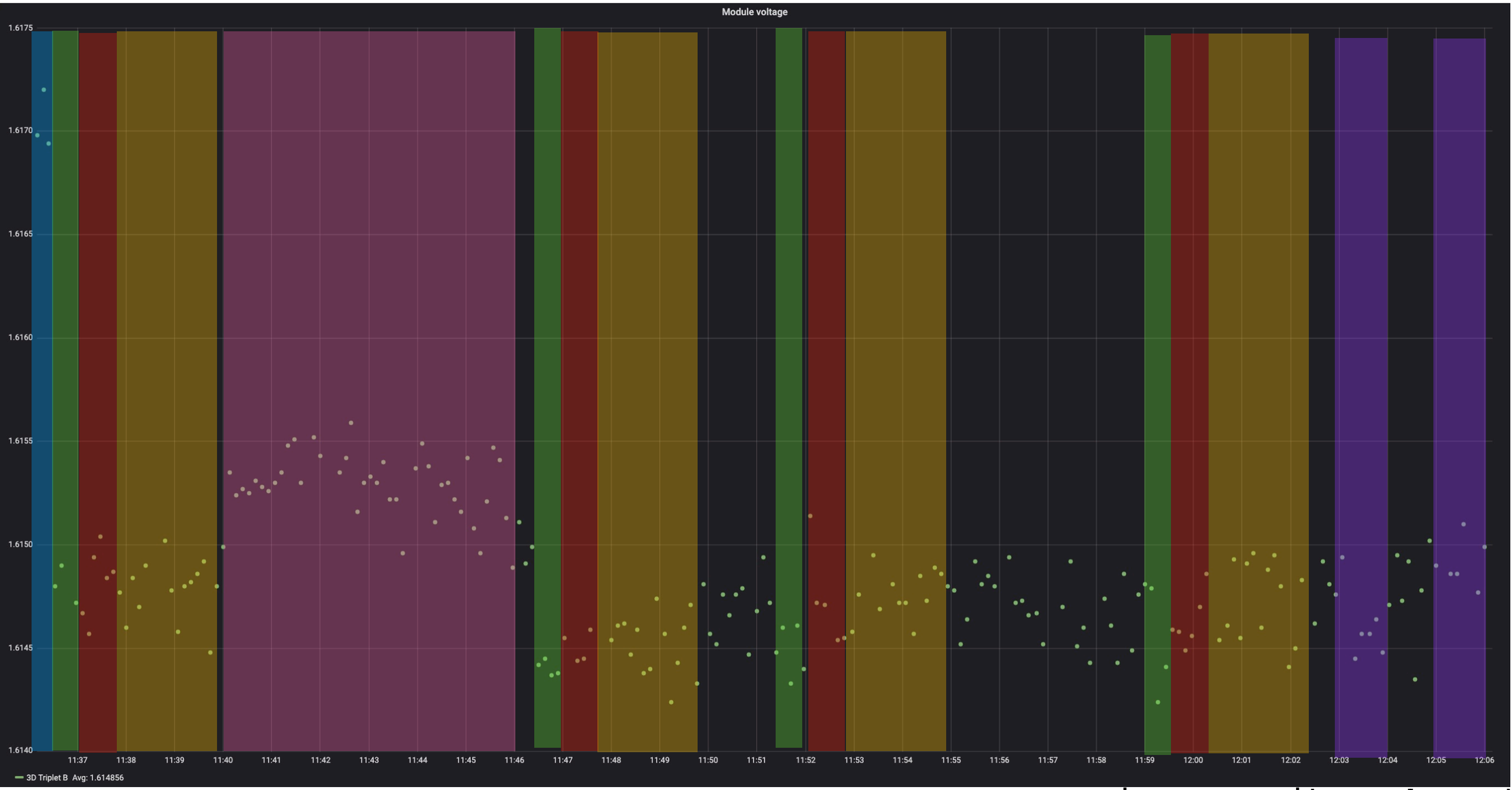
HV C 20
HV B 5

HV B off

HV B 10

Triplet B with 3D sensor

startup digital scan analog scan threshold scan noise scan IV curves



both HV off

HV B @10
HV C off

HV B 10
HV C 20

HV B 10
HV C 100

HV C
off

HV C
20