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Office of Science

# ITkPixV1.1 Quad SP Chain @ Berkeley

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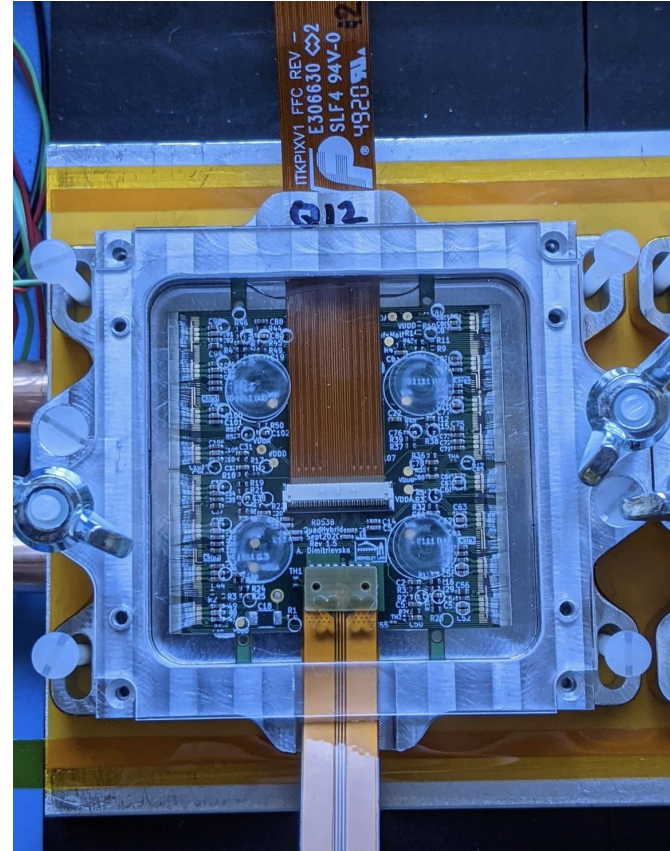
RD53b Testing Meeting

Wednesday, May 19<sup>th</sup> 2021



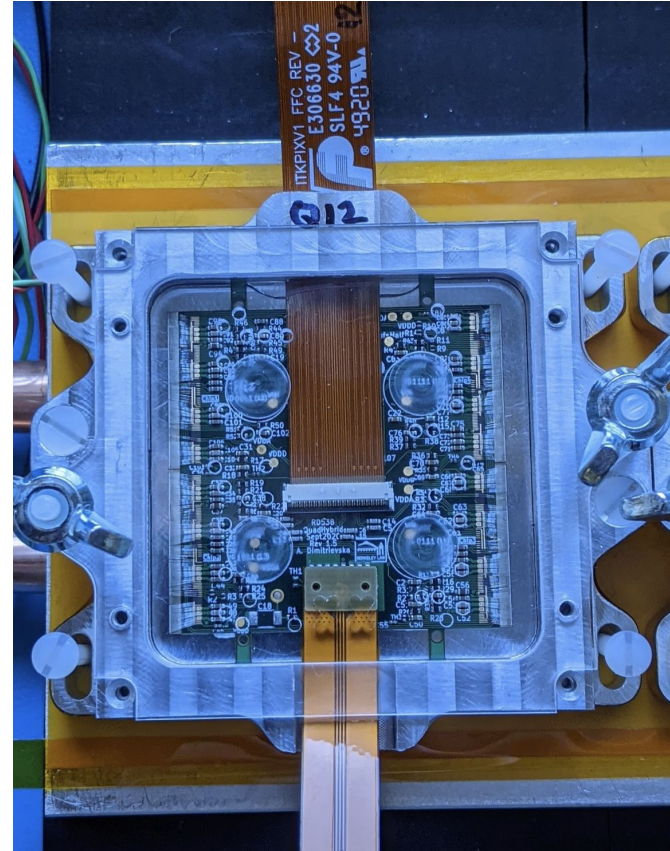
# ITkPix Quad SP Chain

- Over the past few weeks I have set up the first half of what we plan to be an 8 pixel module serial power chain
- Pixel quad modules
  - Digital modules
  - ITkPixV1.1 (wafer 0x162)
  - All green chips, except for 2 (in the current ITkPixV1.1 modules)
- Each module is in the usual quad carrier



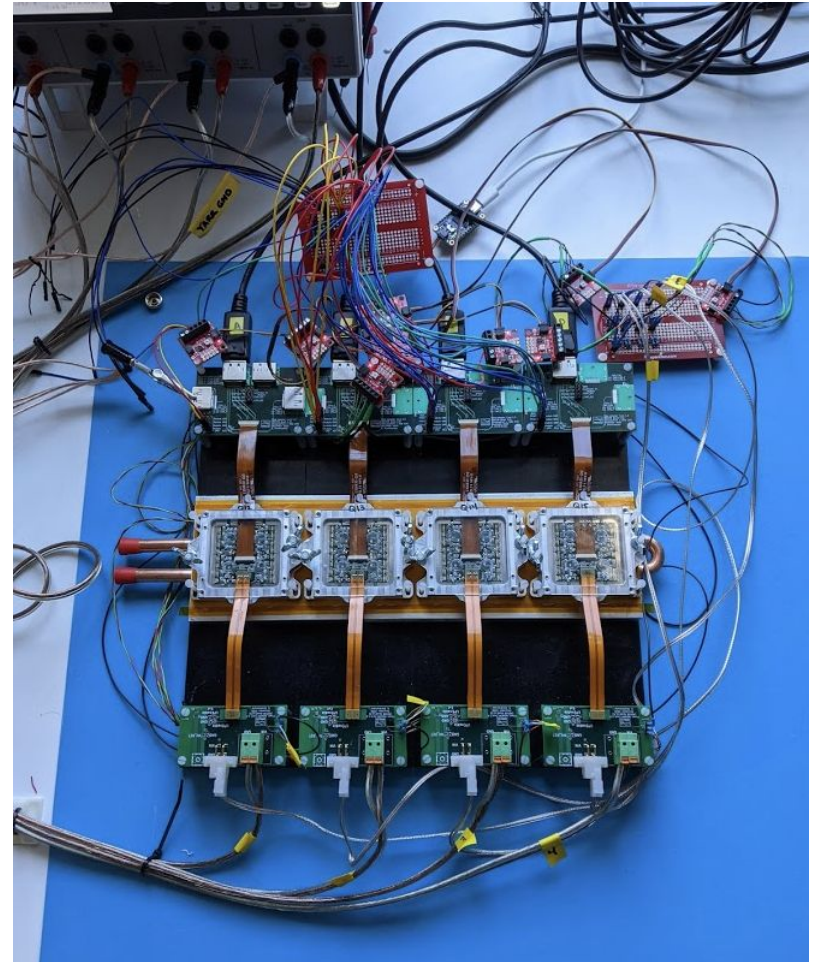
# ITkPix Quad SP Chain

- Designed by Aleksandra:
  - Quad flexes [\[v1.5 link\]](#)
  - Data and LV/power pigtails
    - [\[power pigtail link\]](#)
    - [\[data pigtail link\]](#)
  - Data (1DP and 4DP) and power adapter cards
    - [\[data adapter link\]](#)
    - [\[power adapter link\]](#)
- Further information in AUW slides by Aleksandra [\[link\]](#)



# ITkPix Quad SP Chain

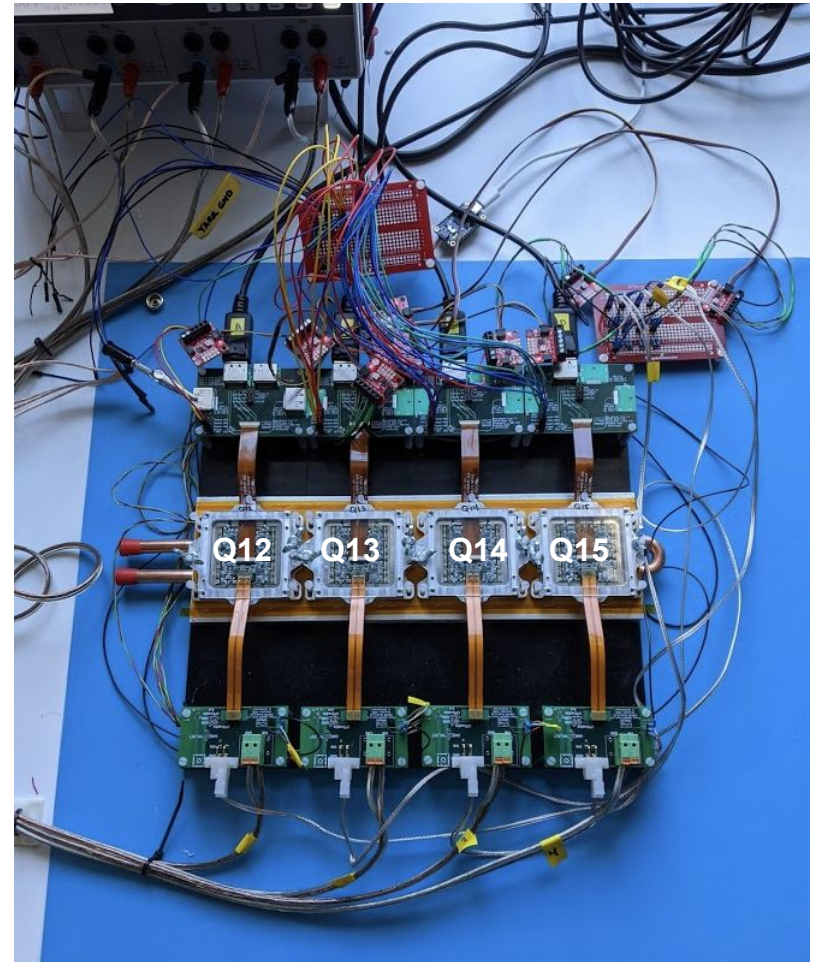
- Currently we are powering all 4 modules in parallel
  - R&S HMP4040, 4-channel power supply
  - Each module powered via separate channel
- DAQ is YARR via DP-to-miniDP
- The idea is to first properly & fully characterize the modules when powered in parallel (i.e. individually) and take this as baseline
- Once full suite of tests and characterizations are done, we can then move to serial powering





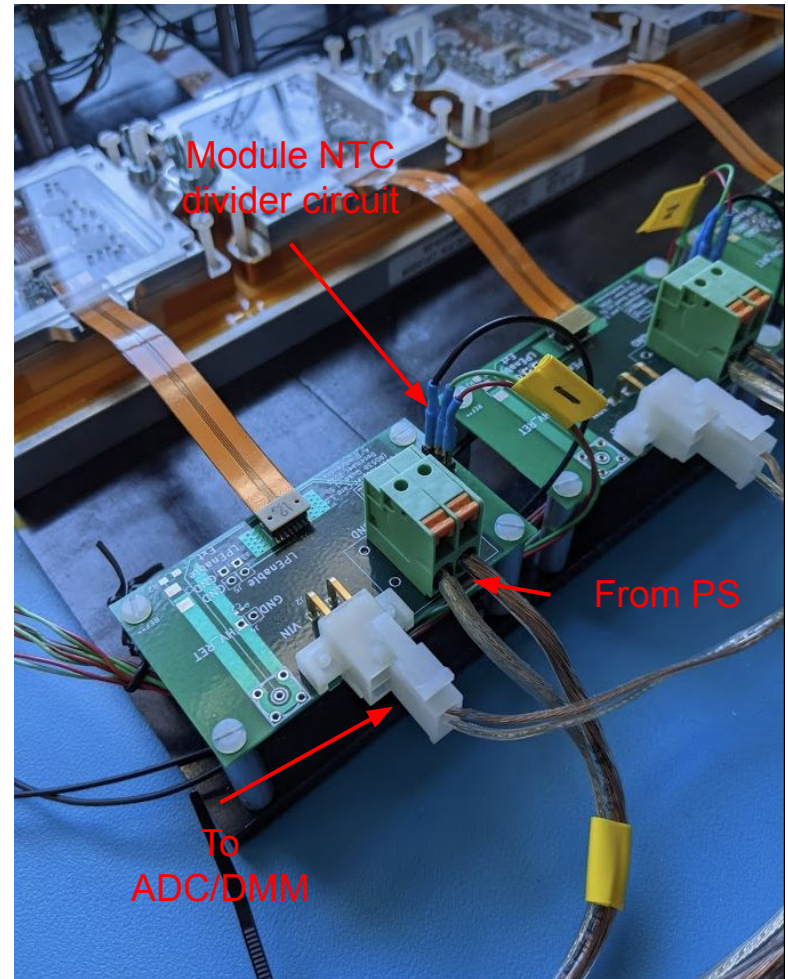
# ITkPix Quad SP Chain

- Modules labelled Q12, Q13, Q14, & Q15
- Further information about these modules (e.g. specific chip IDs) can be found [\[here\]](#)



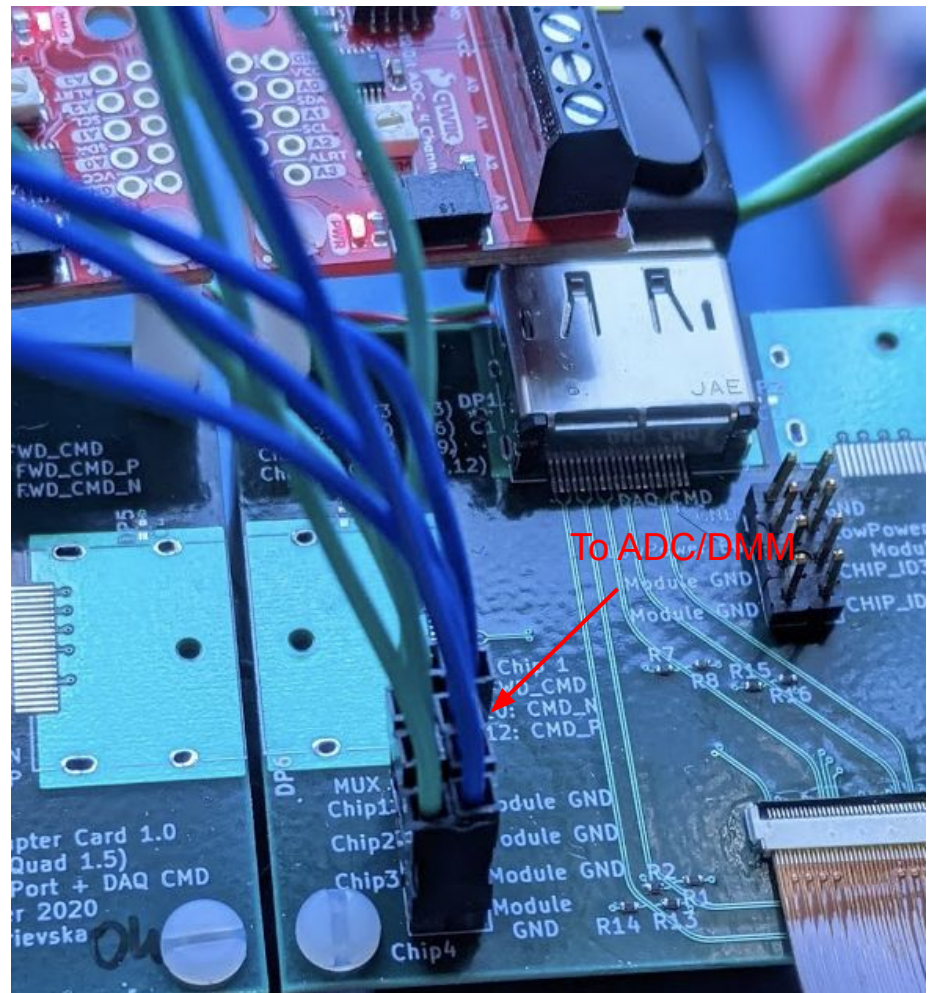
# ITkPix Quad SP Chain

- LV is provided via screw terminal inputs on power adapter
  - Additional Molex connector provides ability to monitor Module Vin
- Module NTC is monitored via pin headers on power adapter



# ITkPix Quad SP Chain

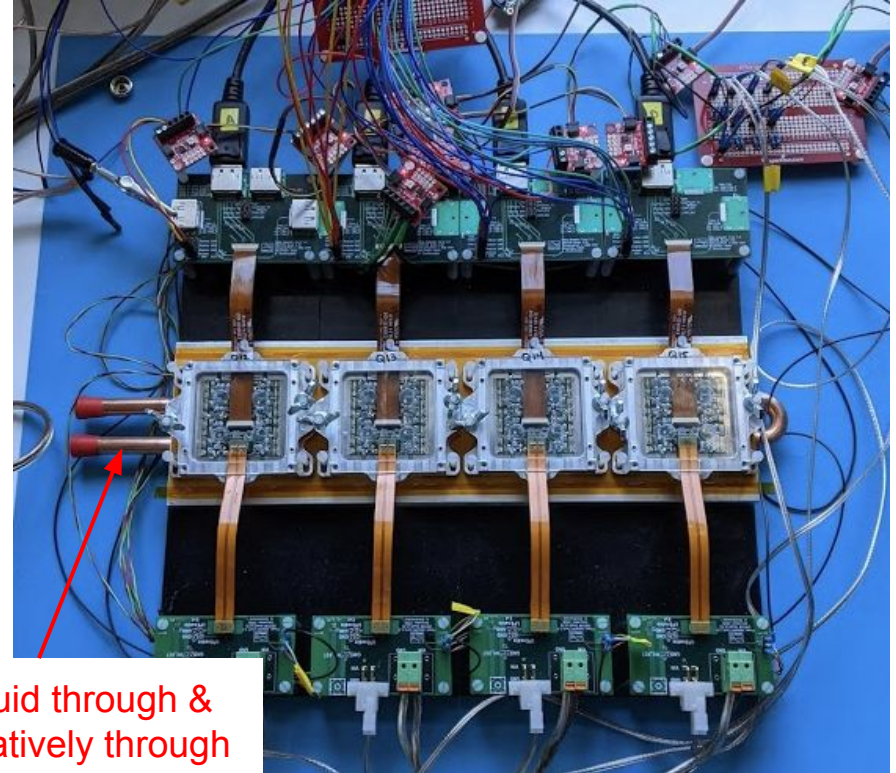
- Every chip on a module has its VMUX routed to pin headers on the data adapter card
- Allows for easily monitoring the chip internals





# ITkPix Quad SP Chain

- Aluminum cooling chuck
- Working on cooling solution using radiative cooling
- Right now (without cooling), I only power a single module at a time
  - Monitor the temperature via labRemote (grafana)
  - Ensure that modules are  $<40$  deg-C



Pump fluid through & cool radiatively through fans & fins to room temperature



# Configuration

Currently targeting the “L2 configuration”, 3.5 $\mu$ A analog current

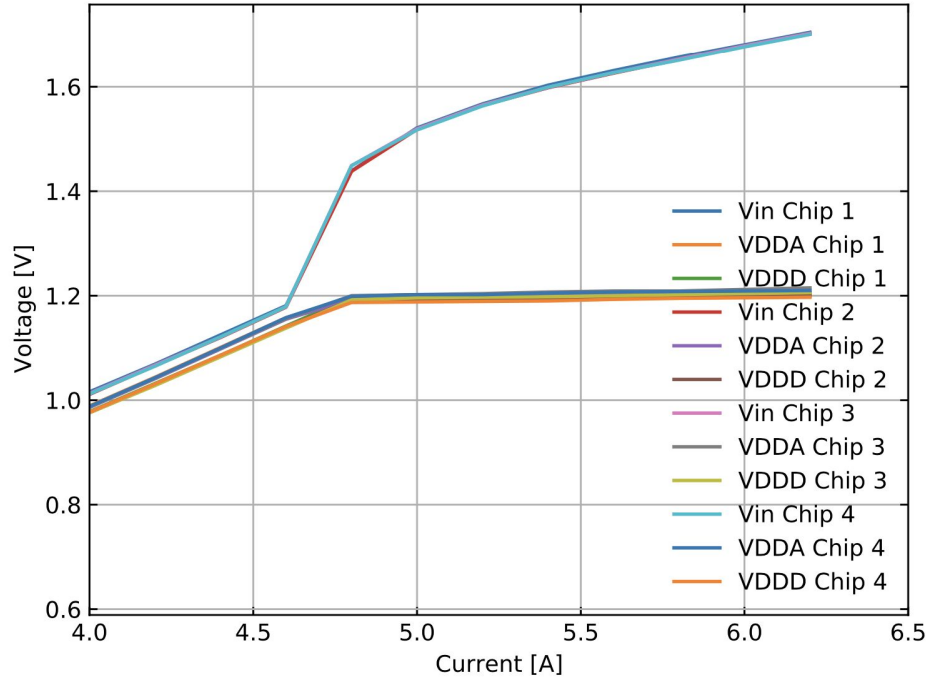
	L0	L1	L2	L3-L4
DAC	4.5 $\mu$ A setting	4 $\mu$ A setting	3.5 $\mu$ A setting	3.0 $\mu$ A setting
DiffPreampM	900	730	550	400
DiffPreComp	300	300	300	300
DiffComp	500	500	500	500
DiffTh2	0	0	0	0
DiffVff	150	150	60	60
Threshold	1000e	1000e	1000e	1000e
DiffLcc	500	500	500	500
DiffLccEn	0	0	0	0
DiffFbCapEn	0	0	0	0

# Plans

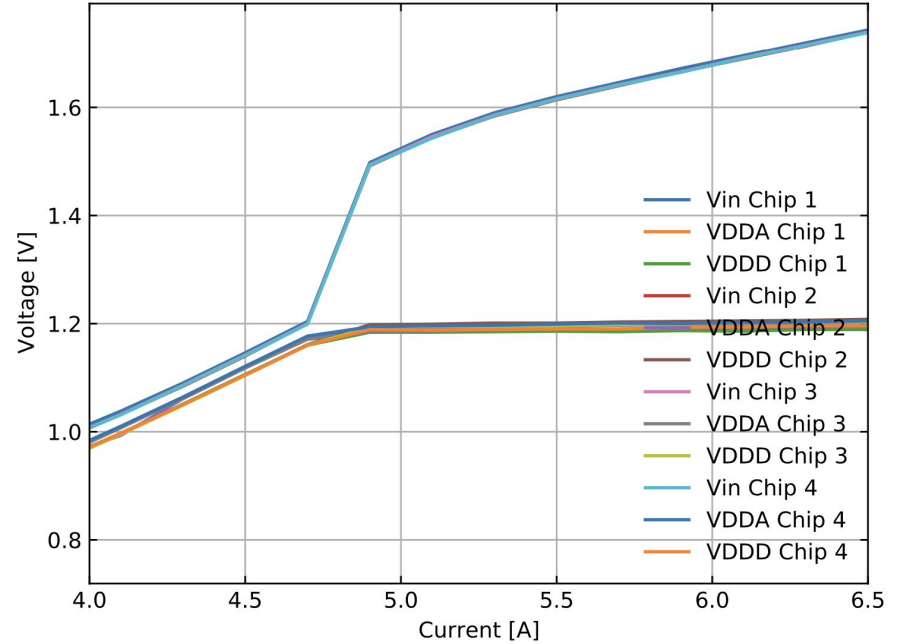
- Now that we have an initial setup with 4 modules, we are planning to begin performing characterization studies on the modules, and then on the chain as a whole
  - Currently doing initial studies (SLDO tuning, module VI, etc...)
- ... and move to serial powering
- We have additional ITkPixV1.1 at LBL for an additional 4 modules, to make an 8-module SP chain in total

# Module VI

Module Q12



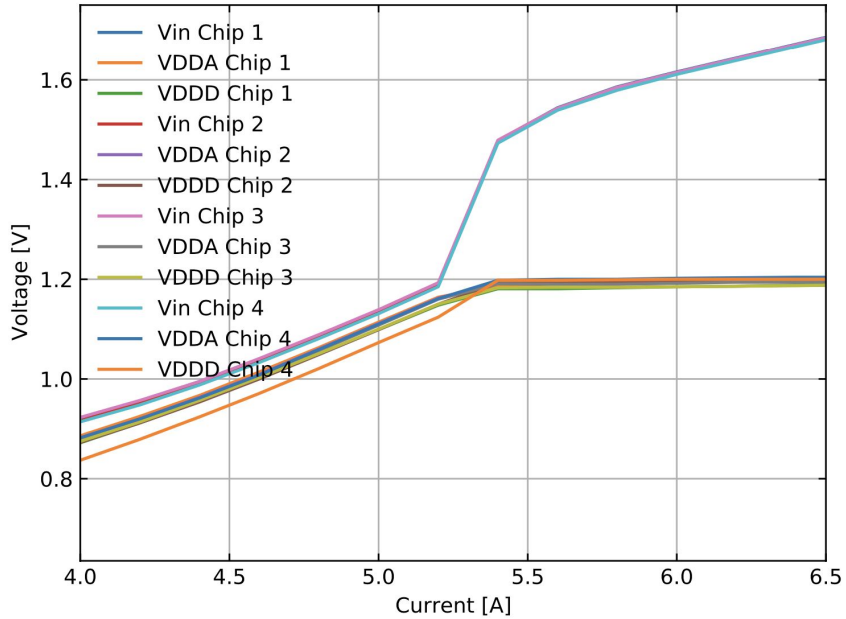
Module Q13



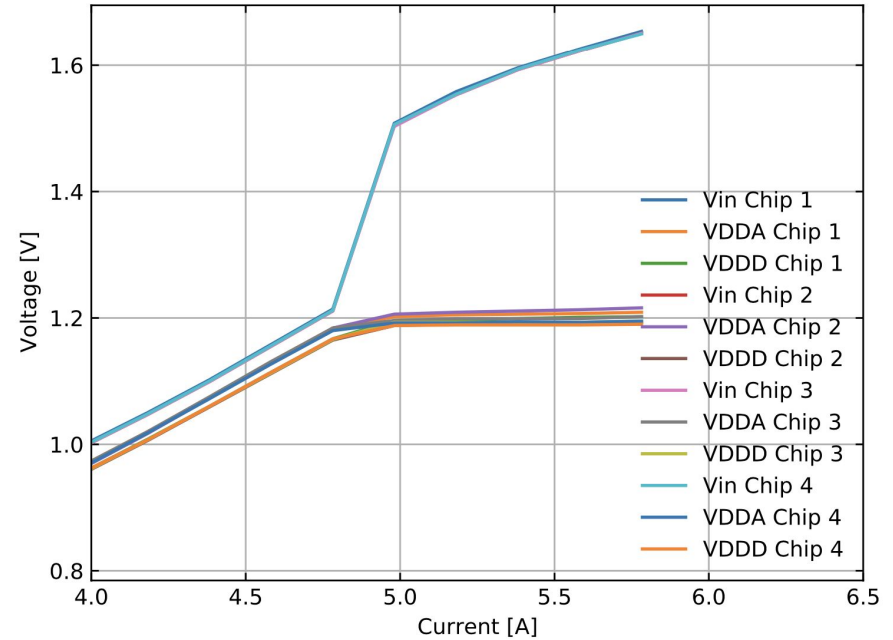


# Module VI

Module Q14



Module Q15



# Measurements List (preliminary)

- Module/chip VI
  - Measurements as function of module input current for ( $V_{in}$ ,  $V_{DDA}$ ,  $V_{DDD}$ ,  $V_{Offs}$ ,  $I_{inA}$ ,  $I_{inD}$ ,  $I_{shA}$ ,  $I_{shD}$ , ...)
- Threshold distributions (baseline vs serial)
- Noise distributions (baseline vs serial)
- Tuning performance (baseline vs serial)
- Threshold vs noise (baseline vs serial)
- Low power mode
- Link sharing testings
- Measure module/chip  $V_{in}$ 
  - For various configurations (powering configuration)
  - Sending random bit patterns
- Undershunt protection tests
- Over-voltage protection tests

**back up**