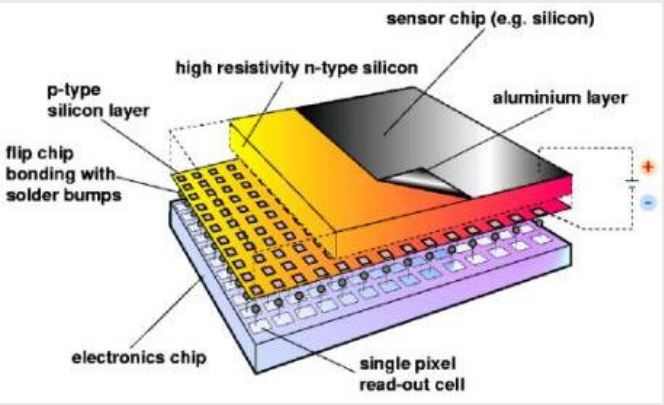
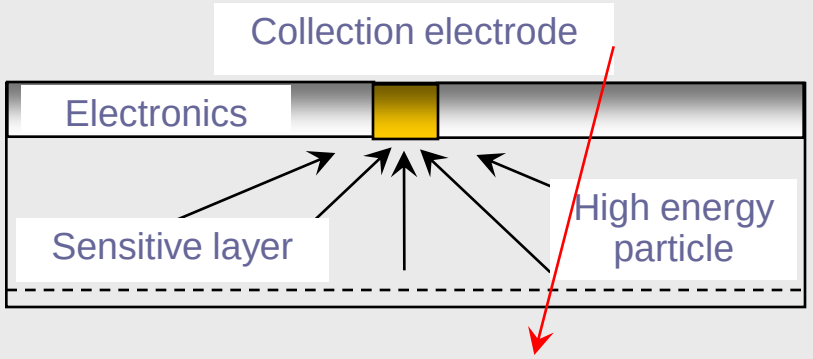
LePIX: monolithic detectors in advanced CMOS





- Scope:
  - Develop monolithic pixel detectors integrating readout and detecting elements by porting standard 90 nm CMOS to wafers with moderate resistivity.
  - Reverse bias of up to 100 V to collect signal charge by drift
- Key Priorities:
  - Develop and optimize the sensor
  - Design low power (~ 1uW/pixel) front end electronics using low detector capacitance
  - Assessment of radiation tolerance
  - Assessment of crosstalk between circuit and detecting elements (may require special digital circuitry
- Need to carry development to a large matrix for correct evaluation

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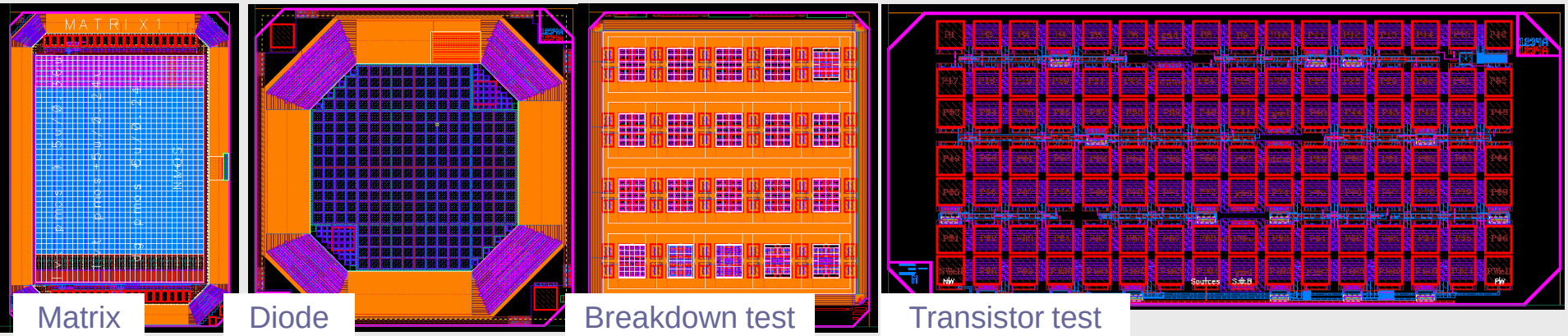
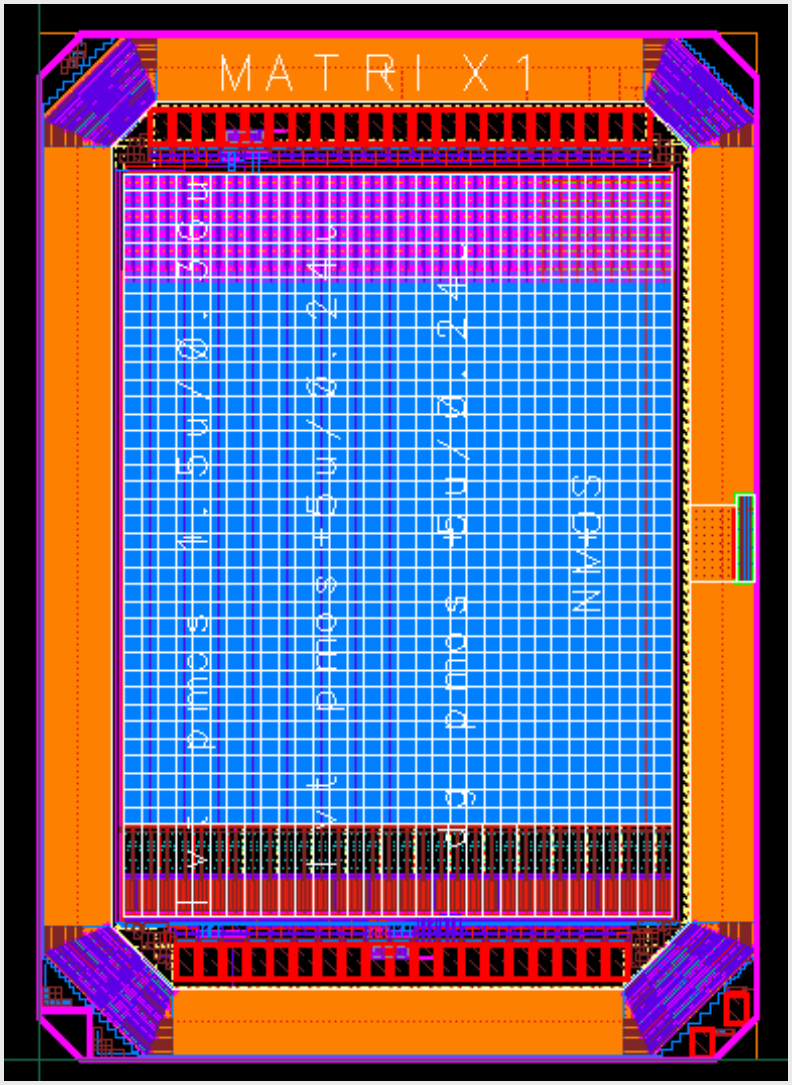
- Submission for fabrication
  - Non-standard: ESD protection, special layers and mask generation, guard rings
  - Received chips on standard substrate with short (~80 ohms) in the guard ring, fix discussed with IBM for special lot on high resistivity, in the mean time measuring to learn as much as possible from the chips on standard substrate
- 7 chips submitted :
  - 4 test matrices
  - 1 diode for radiation tolerance
  - 1 breakdown test structure
  - 1 transistor test: already submitted once in test submission
- Significant testing effort (measurement setup, test cards…)

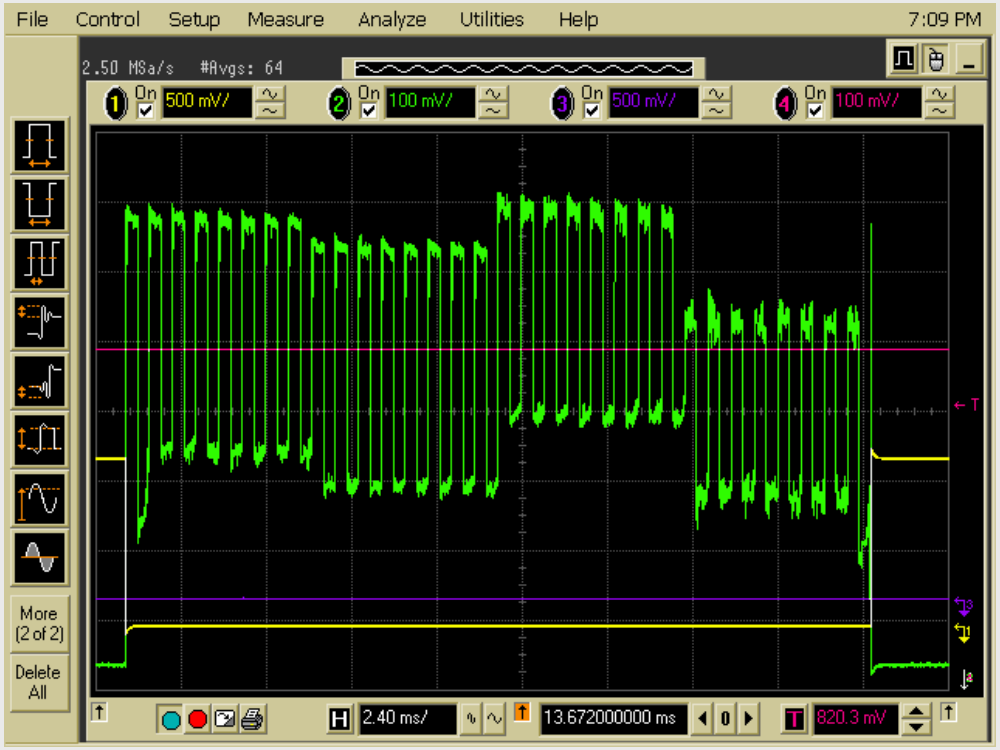


Matrix 1 | Diode | Breakdown test | Transistor test

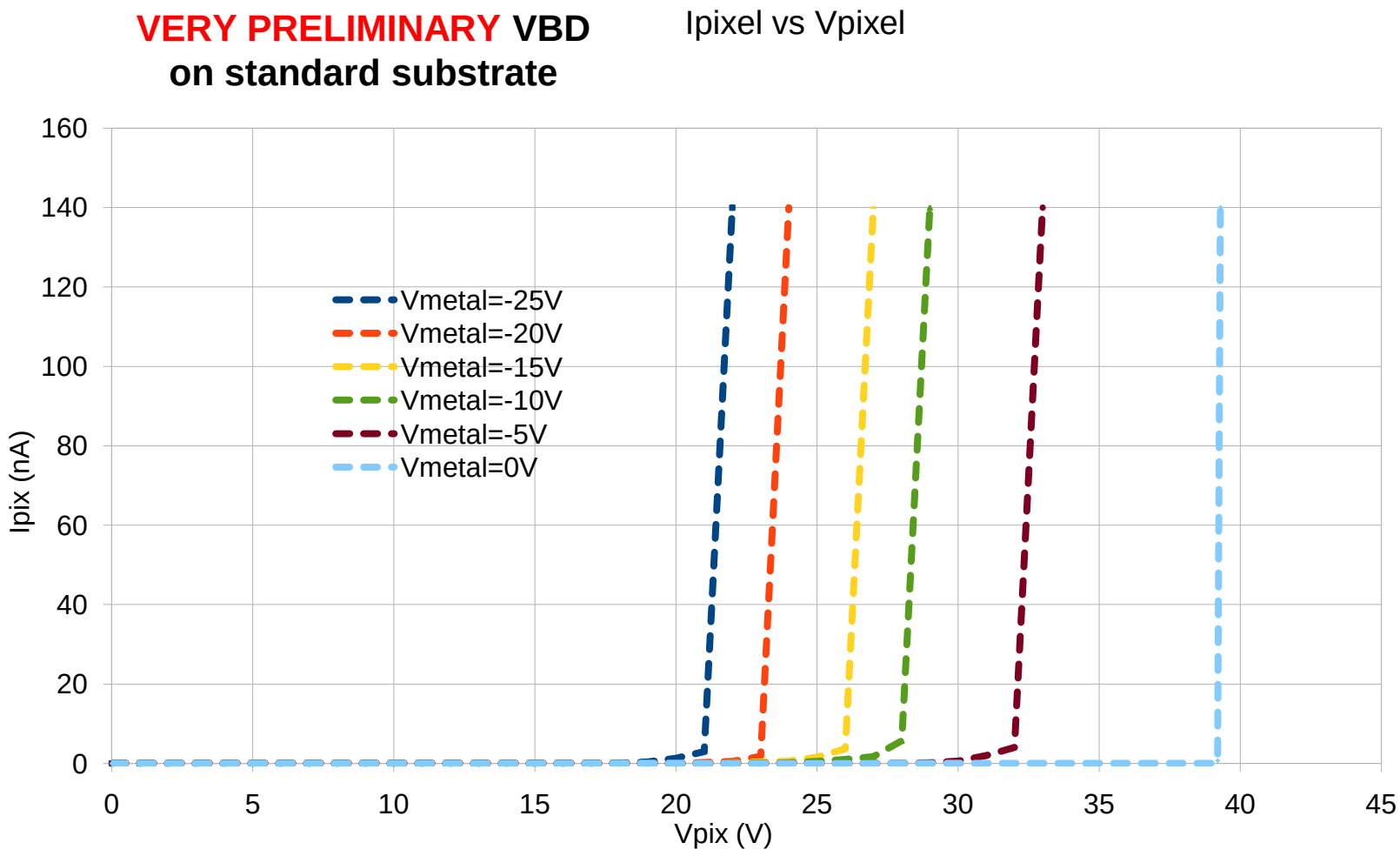
Circuitry of first matrix operational



- 4 zones of 8 columns with different input transistor
- Top part with buffers to read analog signal as it is collected
- Rest with sequential readout, top 16 rows with active reset (pulse), bottom 16 rows with diode reset

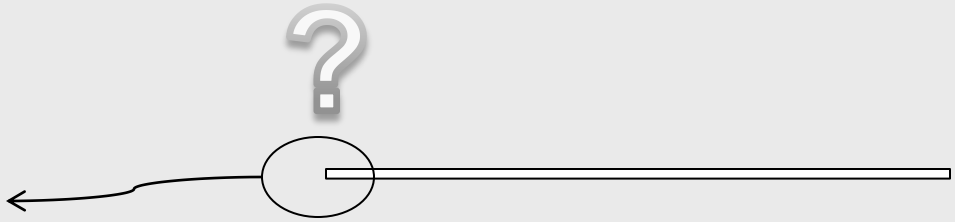


Pixel also needs some correction, but not shorted



Geometry

- Power is key !
- For tracking 10-15 cm by 1-2 cm device to be obtained by stitching
  - “Infinite” connectivity ~ 10 metal layers at ~ 0.xx micron pitch *IF power kept low* !!
  - Aiming at ~10-20 mW/cm2
  - Connection on one side : vbias, vdda, vddd, in, out (ex lvds)… => ~ 10 connections to pads
  - Options: wire bond or connector on the edge or special package (a la memory card)
  - How far do you need to go before one can put reasonably standard electronics ?



- For W Calo have to investigate practical geometry (is overlap allowable to generate wedge?)

LePIX: monolithic detectors in advanced CMOS: future 2012-2016

- Promising but challenging development (cfr mask generation issues).
- Key point is maintaining power consumption low ~10-20mW/cm2
- “infinite” connectivity on-chip, key technology is connection at the end (!)

- Several groups are contributing, planning several submissions in the next years. Updating planning in view of interest.

- Alice is seriously considering LePIX for 2016 upgrade
- CMS groups (including CERN CMS) are very interested in LePIX for tracker upgrade
- Contact/interest from RAL (ATLAS)
- Interest from TOTEM
- Calo ?

THANK YOU