Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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on behalf of the ATLAS Liquid Argon Calorimeter Group

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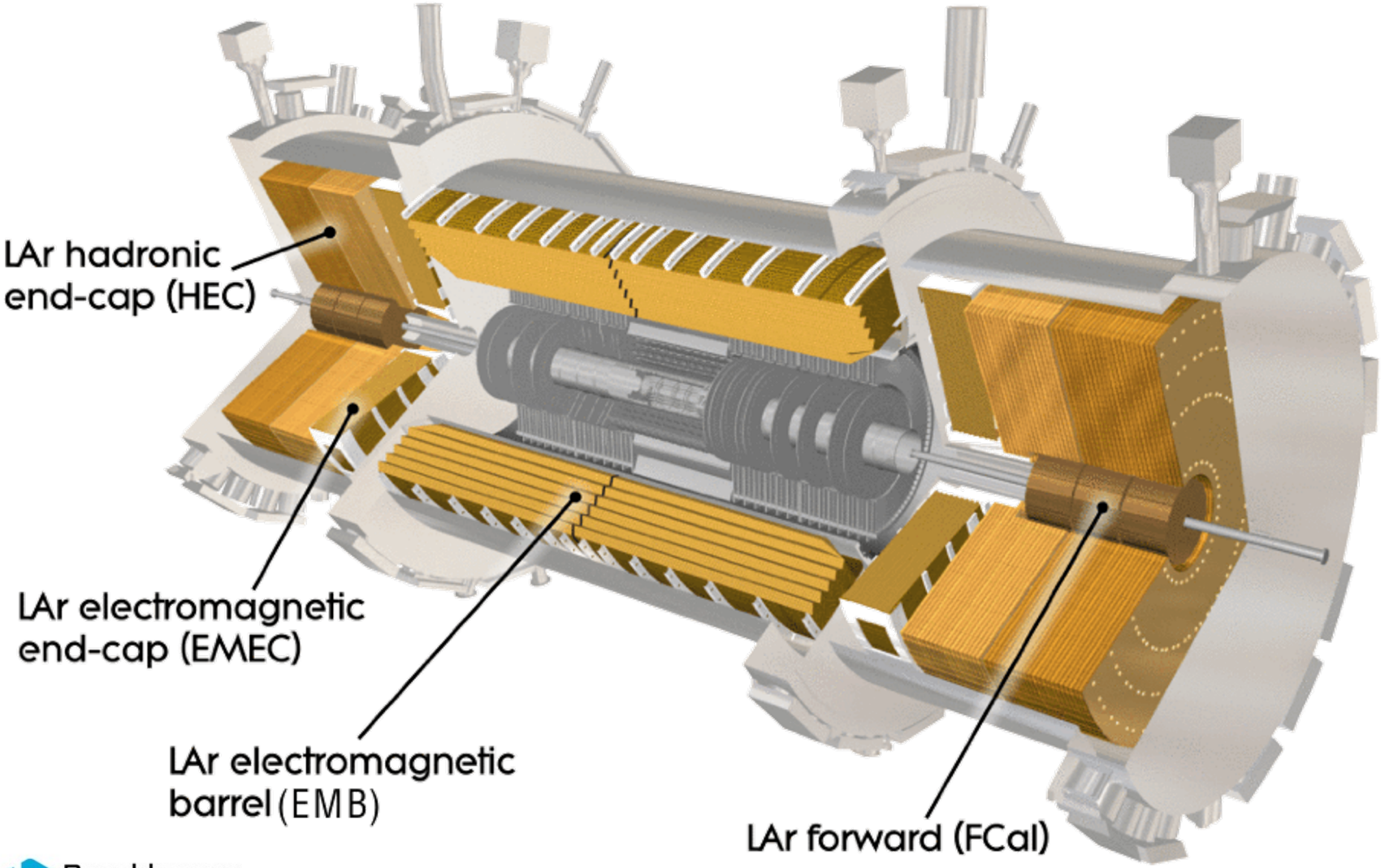
The ATLAS LAr Calorimeter



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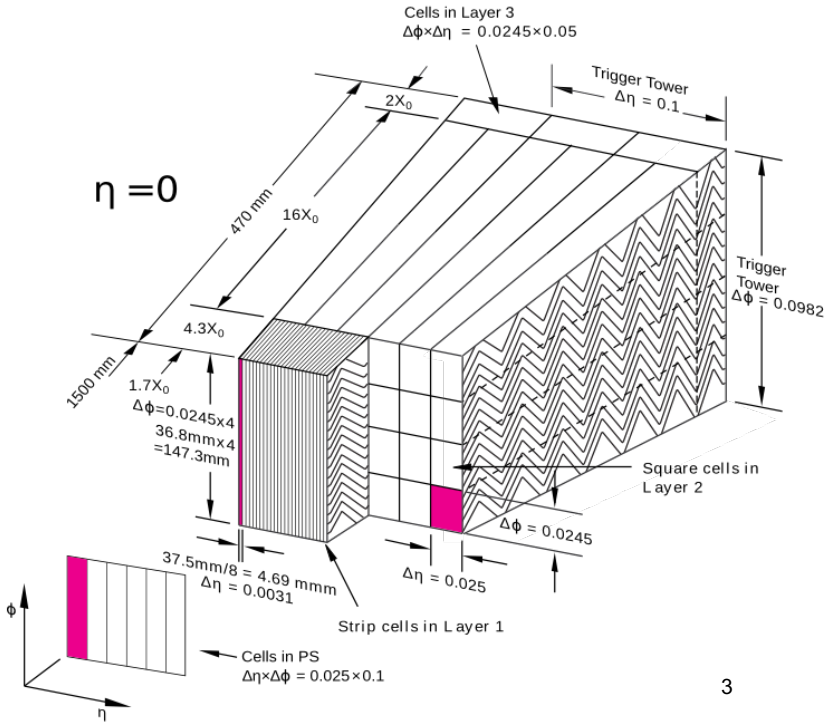
The ATLAS LAr Calorimeter

- Two calorimeters: electromagnetic (LAr) + hadronic (LAr + scintillating tiles)
- Readout electronics system samples the calorimeter cells current at the LHC collision frequency of 40 MHz and sends the information off-detector for further processing (Triggering) and storage

- High Luminosity LHC (HL-LHC:
  - Up to 7x design luminosity (~200 simultaneous collisions)

- LAr calorimeters themselves are reliable throughout HL-LHC

- The entire on- and off-detector readout electronics chain will however be replaced to provide more information from the calorimeter for trigger decision in increased collision rate and pile-up

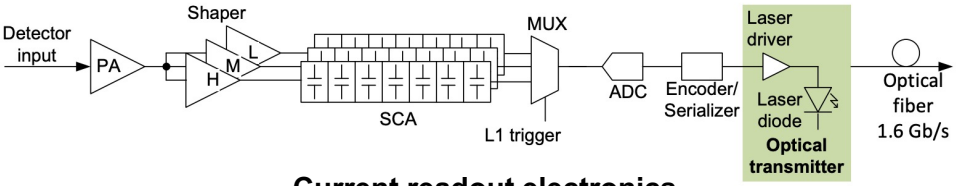


The ATLAS LAr Calorimeter Upgrade

The calorimeter must remain performant for 10 years (4000 fb^{-1}) of HL-LHC, while providing more granular information to the trigger system and DAQ

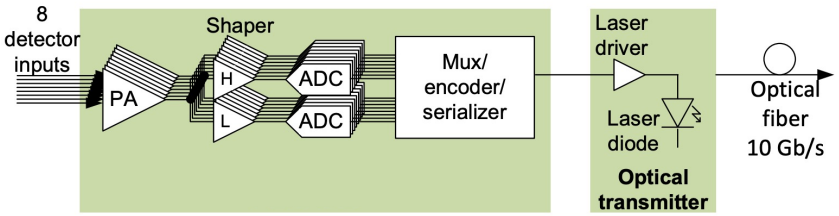
- Wide dynamic range: **16 bits**
- Quantization noise < intrinsic LAr resolution
  - (10% / √E + 0.7%)

- Radiation tolerance:
  - TID (14 x 10^2 Gy)
  - NIEL (4.1 x 10^{13} n_{eq}/cm^2)
  - SEE (10.5 x 10^{12} h/cm^2)



Current readout electronics

- Fully digitized readout of the entire Calorimeter at 40 MHz with two gains for the Trigger and DAQ systems
  - 1524 Front-end boards, 128 LAr Calorimeters channels (256 digitized)
  - 250 Tb/s, 163.84Gb/s per board of raw data via 10Gb/s Optical links

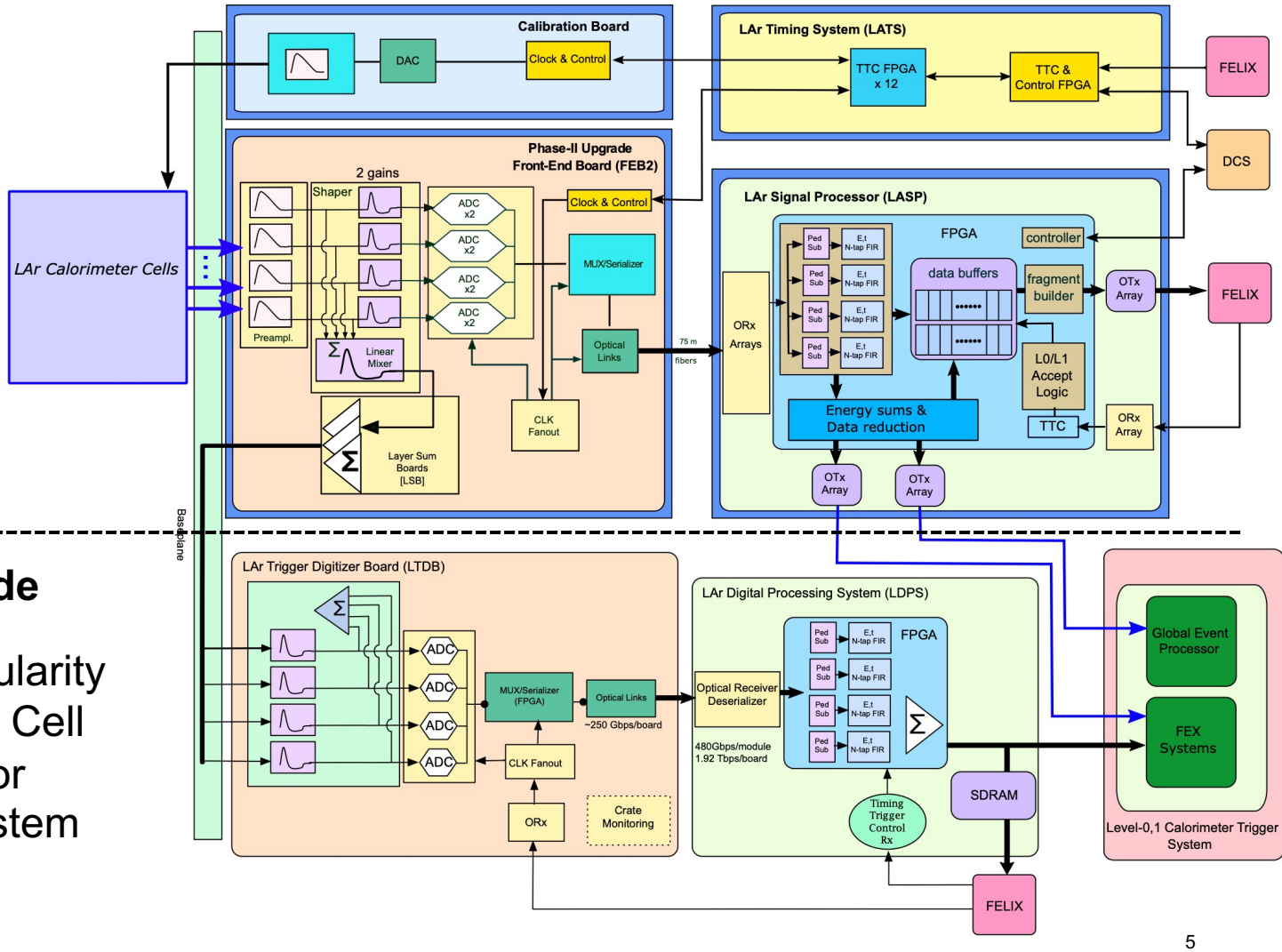


Upgrade readout electronics

The HL-LHC LAr Calorimeter Readout

Phase-II Upgrade

Digitize and readout the full calorimeter, at 40 MHz and provide the information to Level-0 trigger systems



Phase-I Upgrade

Increase the granularity of the Calorimeter Cell sum information for Level-1 trigger system (In-installation)

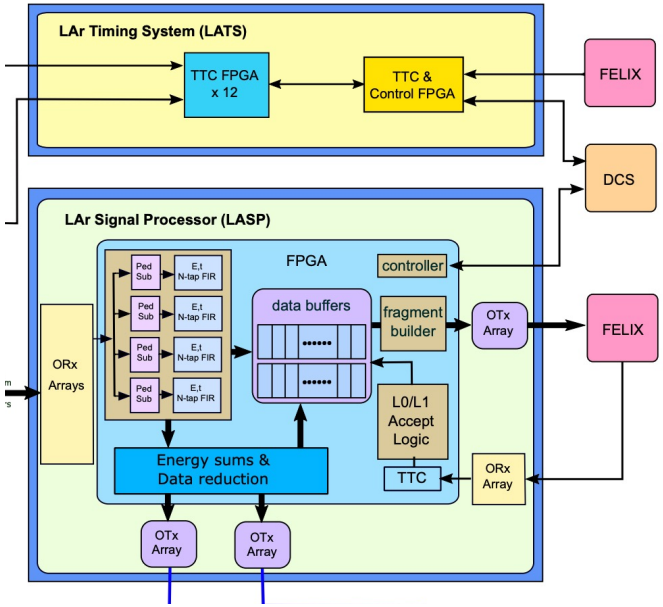
Off-Detector Control and Readout

LAr Timing System (LATS)

- 26 x boards
- Configuration, monitoring and Trigger Timing and Control (TTC) distribution for on-detector boards (FEB2)

LAr Signal Processor (LASP)

- 190 x ATCA Blade with two FPGA
- Data from FEB2, ~1024 channels / LASP
- Digital filtering and calibration of signal energy
- Compute and provide signal's energy and time information
- Feed the data to the trigger system and buffer them until L0-Accept to send them to TDAQ



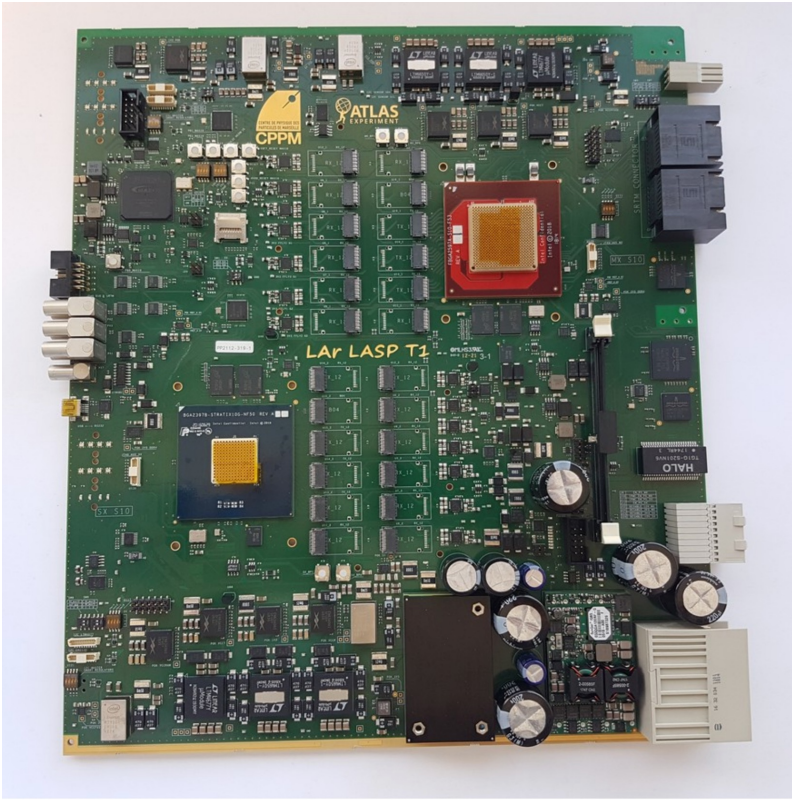
LASP developments

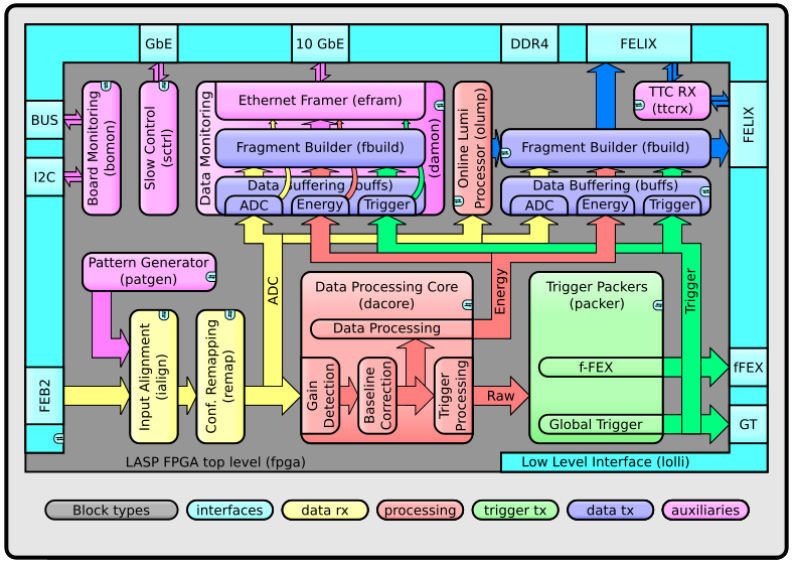
A test board version of the LASP has been produced to validate the functions required for the final prototype

- DC/DC Converters and regulators
- I2C Communication with sensors and IC on board
- FPGA Configuration and operation
- Board received and currently being tested (prior to mounting FPGAs)

The LASP firmware development is well under way

- Modular firmware allow for independent development of important block
- Blocks integrated and validated via Continuous integration

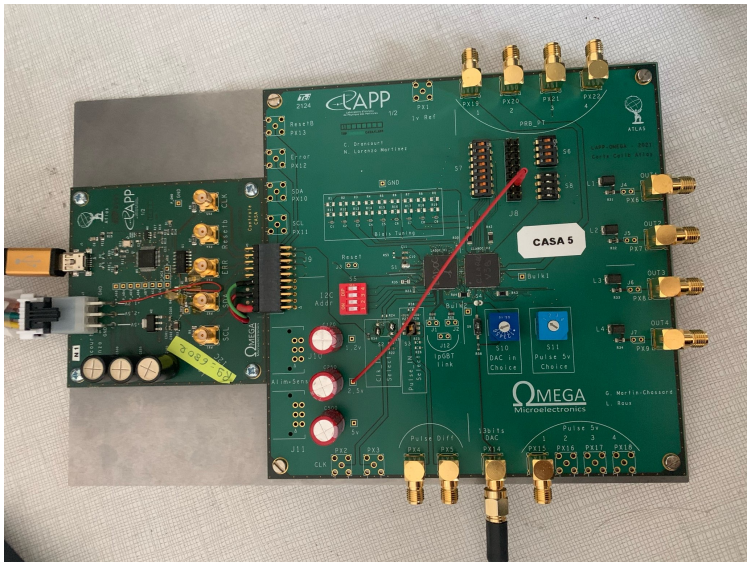




On-Detector Readout and Calibration

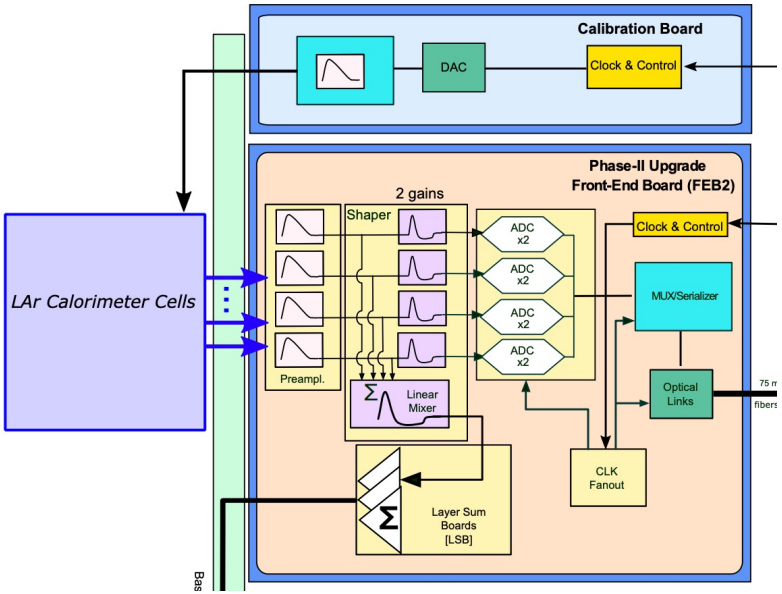
Calibration Board

- 130 boards with 128 output channels
- Provides pulses with well known amplitude and shape for the calibration and testing of the Readout board channels
- 16-bit dynamic range, < 0.1% Linearity
- Radiation hard up to 14 kGy
- Solution based on custom ASIC for High-Frequency Switching and Digital-to-Analog Conversion (CLAROC,LADOC)



Front-End Board (FEB2)

- 1524 boards with 128 input channels
- Sample the signals over two gains and digitize on 14 bits at 40 MHz
- Provide input signal analog sum to Layer Sum Boards
- Serialize data via 10Gbps lpGBT links
- Solution based on lpGBT, custom ASICs
  - **ALFE (LAUROC)** for preamplification, shaping and analog summing
  - **COLUTA ADC** for digitization



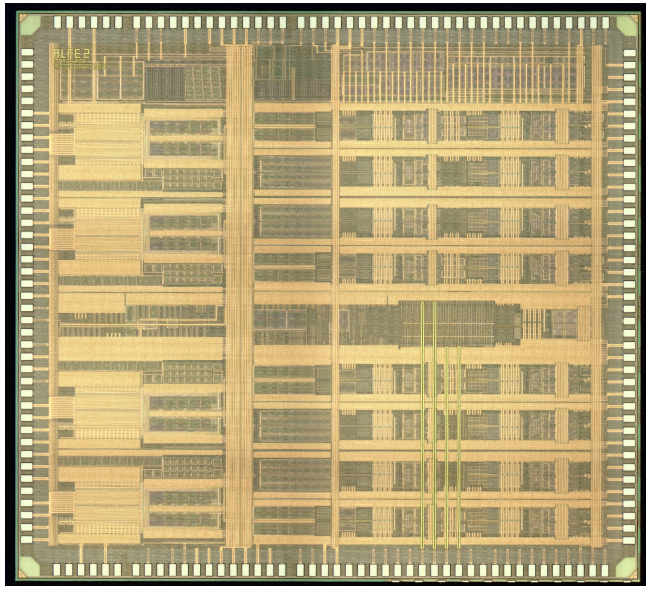
The FEB2 Preamplifier/Shaper

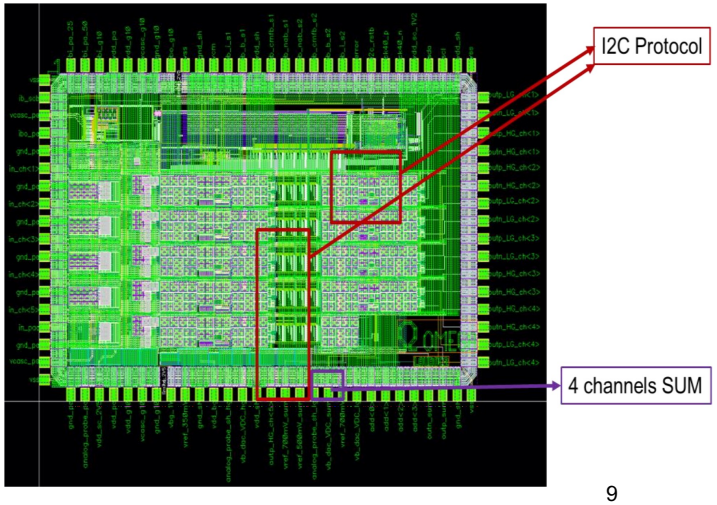
The FEB2 Preamplifier and shaper will be integrated in a single custom ASIC. To adapt to the input signal from various parts of the calorimeter, the requirements are:

- 4 Channel input, 9 Channel output (4 x LG/HG + Trigger sum of 4 channels)
- Input impedance and Dynamic range programmability (25 Ohm 10 mA, 50 Ohm 2mA)
- Input impedance tuning < 2.5 % steps
- Peaking time tuning (15 ± 5 ns, 1 ns steps)
- Preamplifier DC level tuning 200, 2.3 V ± 50 mV
- DC output tuning, 600 mV ± 360 mV, 30 mV steps

- Multiple prototype produced in TSMC 130nm
  - HLC, ALFE/ALFE2
  - LAUROC0/1/2
- Both prototypes meet requirements, ALFE2 selected for better noise performance

ALFE2





LAUROC2

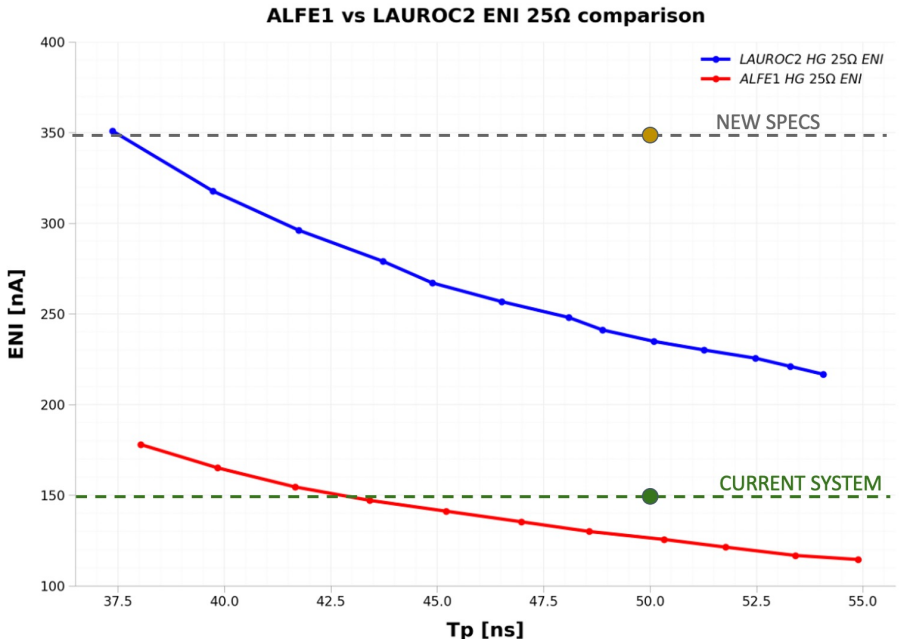
The FEB2 Preamplifier/Shaper : ALFE

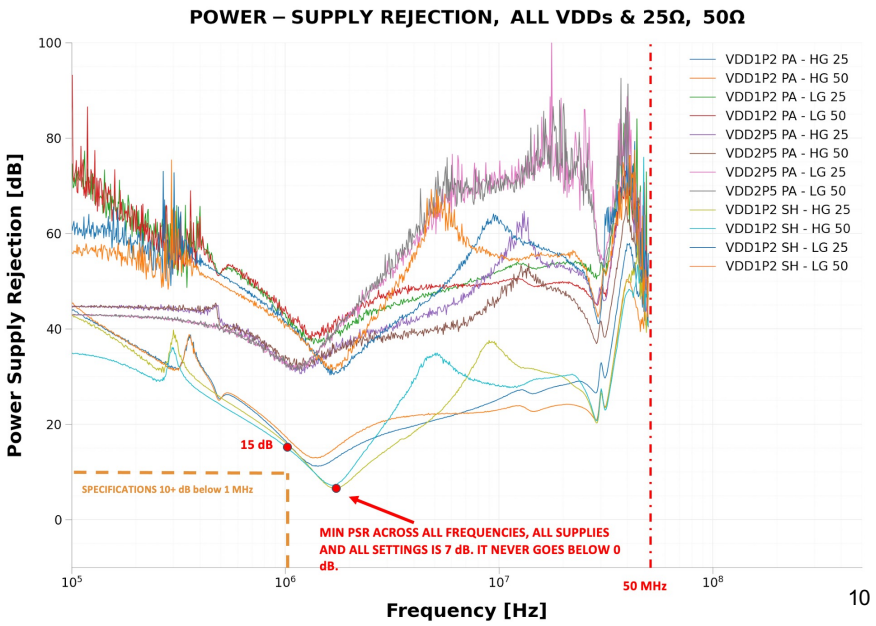
The ALFE preamp/shaper architecture was selected for the FEB2 dues to its excellent noise performance and power supply noise rejection, **Non-Linearity < 0.2 % (HG) over full Dynamic Range**

The ALFE prototype demonstrates no change in performance under irradiation up to **1 Mrad**, much beyond specifications

The ALFE2 prototype integrates the I2C configuration block from LAUROC, that has demonstrated in silicon a **SEE tolerance beyond specifications**

48 832 ASICs will be required to populate the LAr Calorimeter's FEB2





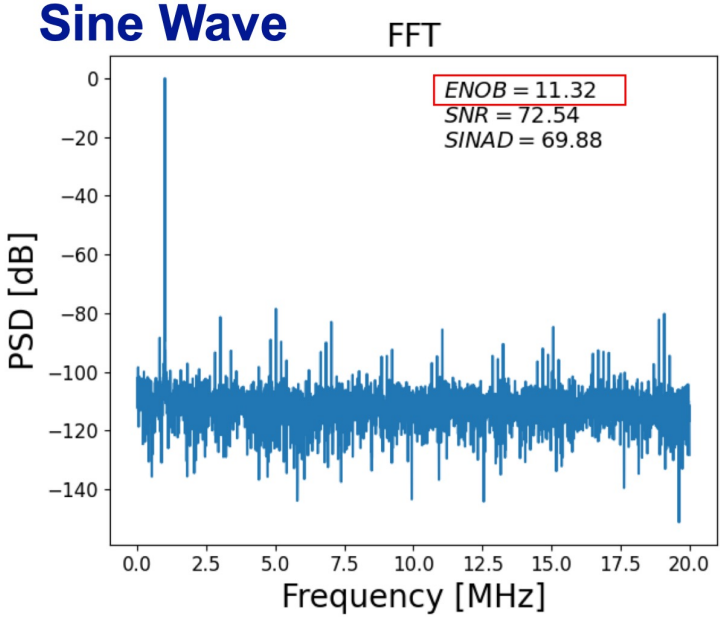
FEB2 Digitization ASIC : COLUTA

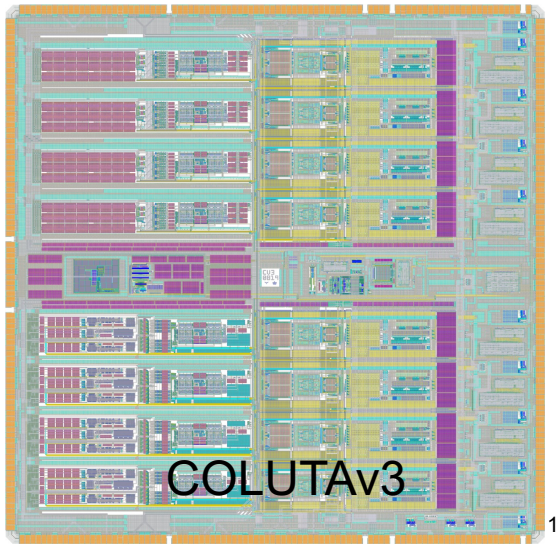
FEB2 ADC requirements:

- 14-bit dynamic range
- 11-bit ENOB
- 40 MSPS
- Low power < 100 mW / channel
- Radiation hardness

COLUTA ADC

- 65nm TSMC
- 14-bit (3.5 bit MDAC → 12-bit SAR), digitizes at 40 MHz with two gains
- 4 channels, 8 ADC/ASIC
- Low noise and good long-term stability
- Highly configurable via I2C
- Cross-talk <0.1%
- Coherent Noise < 0.2 LSB





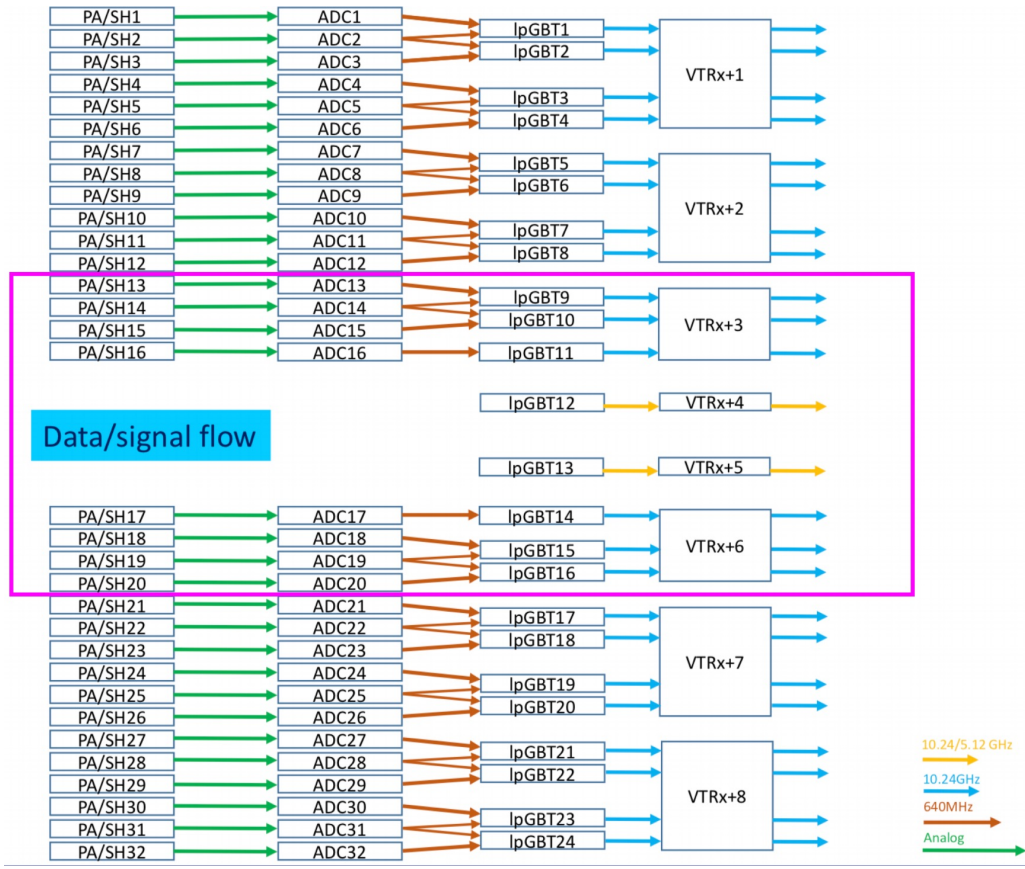
FEB2 Integration

The integration of the ASICs into the Front-End Board design is done with a succession of partially integrated board (slices) with increasing Complexity

- Analog Test Board (2019), 2 channels
- Slice Test Board (2020-21), 32 input channels
  - LAUROC + COLUTAv3 + lpGBT
- FEB2 Prototype (2022), full readout of 128 channels

The FEB2 Slow control makes use of the lpGBT I2C Master, ADC and GPIO to monitor board temperature, configure ASIC

The lpGBT implement a redundancy scheme against VTRx failure



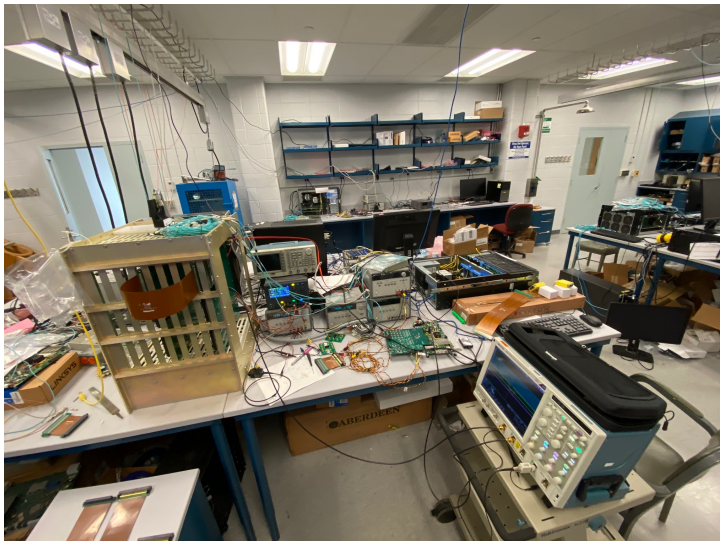
Slice Test Board

The Slice test board integrates the main components of the final system:

- Control and Data lpGBT for slow control and readout of 8 x COLUTAv3
- Powering network and Input protection network
- VTRx Module for optical transmission
- Signal Input via backplane connector for crate integration

The board can be used to prepare the integration of a test stand for the final production of the FEB2

- Study of Noise, Linearity, cross-talk for improvement to FEB2 Prototype
- Development of Software and Firmware for the Operation and Characterization of the production board



Test Calibration Carrier Board

A Carrier Board fitting the FEC has been designed, to integrate:

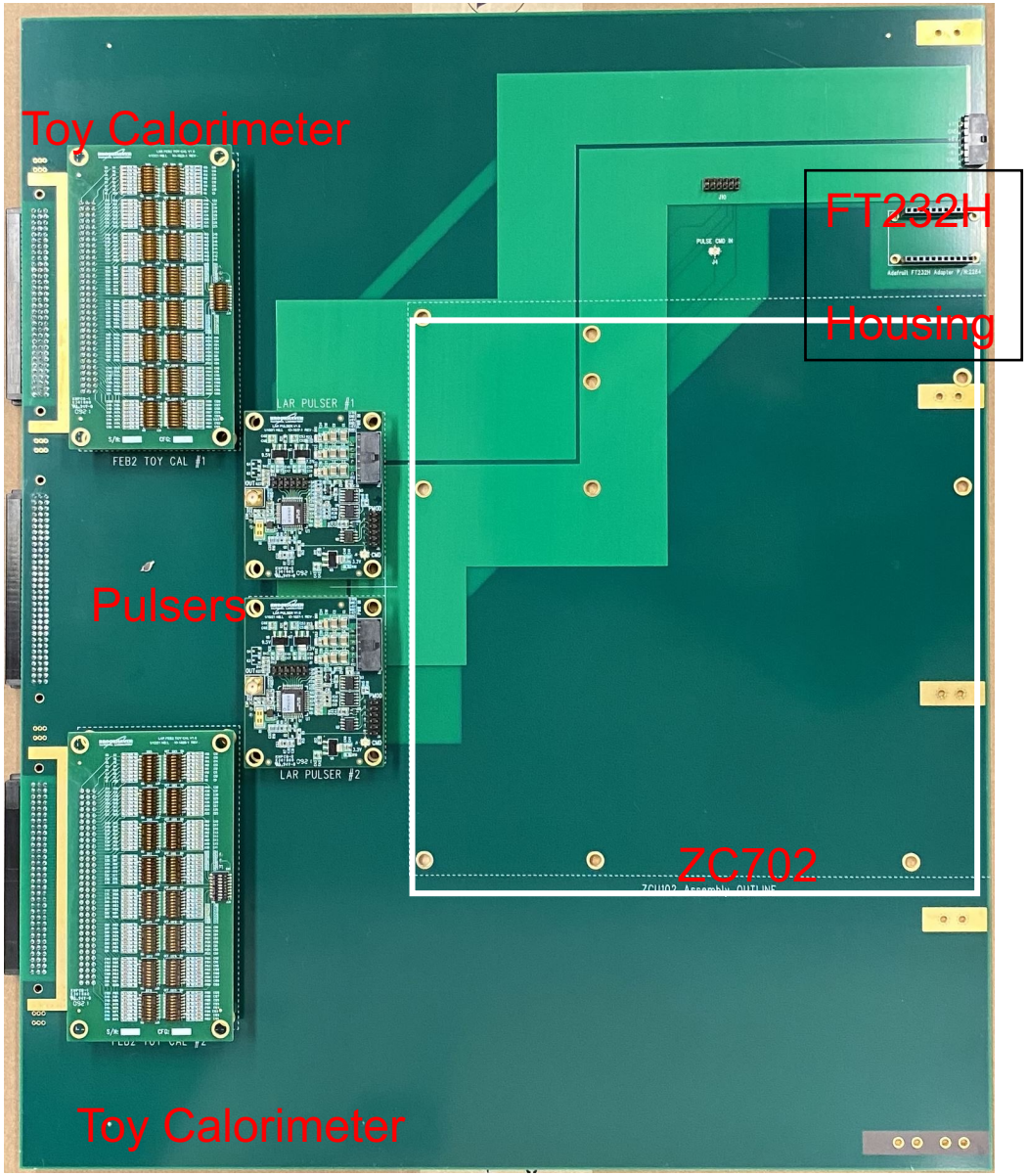
- The Toy Calorimeter modules (64ch)
- The Pulse Generator module
- FPGA Evaluation board to:
  - Receive the clock and trigger from the FELIX system
  - Control the pulser DAC

The Slice Test Board/FEB2 software can control the FPGA module (ZCU102) via the optical link or a parallel GbE Connection to perform injection tests and scan with the Slice Test Board and FEB2

The pulser can also be operated SPI dongle

Injection of external trigger can be fed by external pulse

Integration test will use these custom designs for initial development before the official board is available



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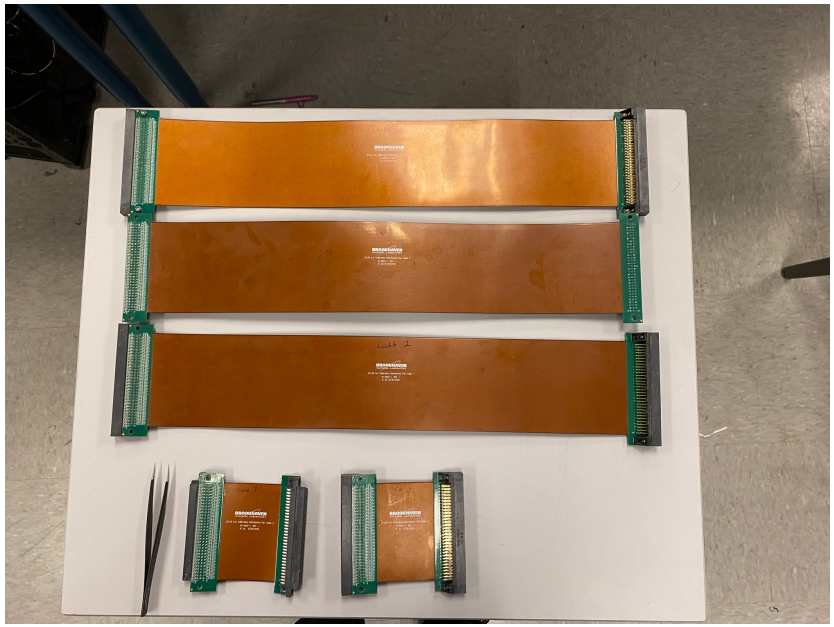
Calibration Distribution Board and Flex Cable Version

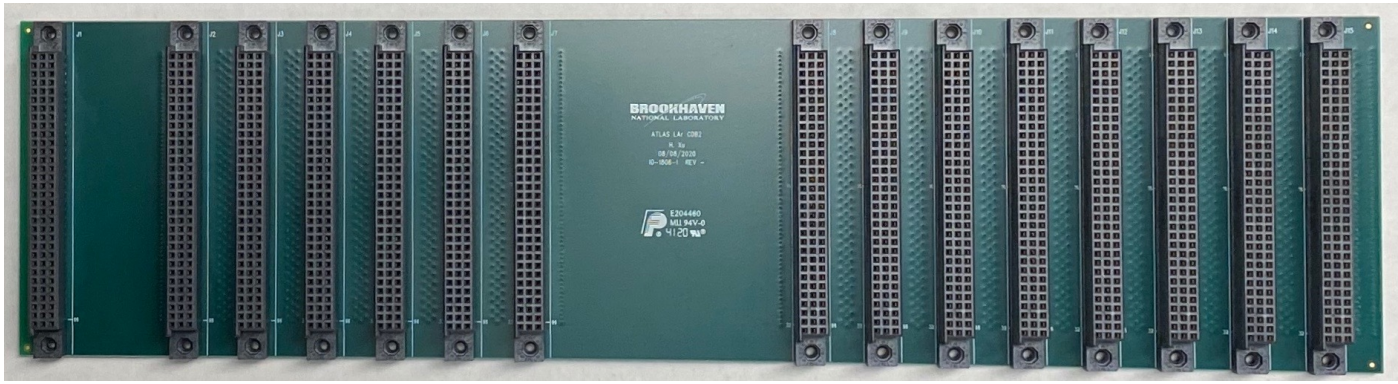
As the Slice Test Board and Calibration prototype card fit the the current FEC, we can use them to exercise and prepare the FEC Test Stand

Two types of design to accommodate interconnection needs:

- Calibration Distribution Board V2 for connection of multiple FEB2
- Flex Cable solution for direct Card-to-Card connection

Interconnection designed to mimic detector electrical properties





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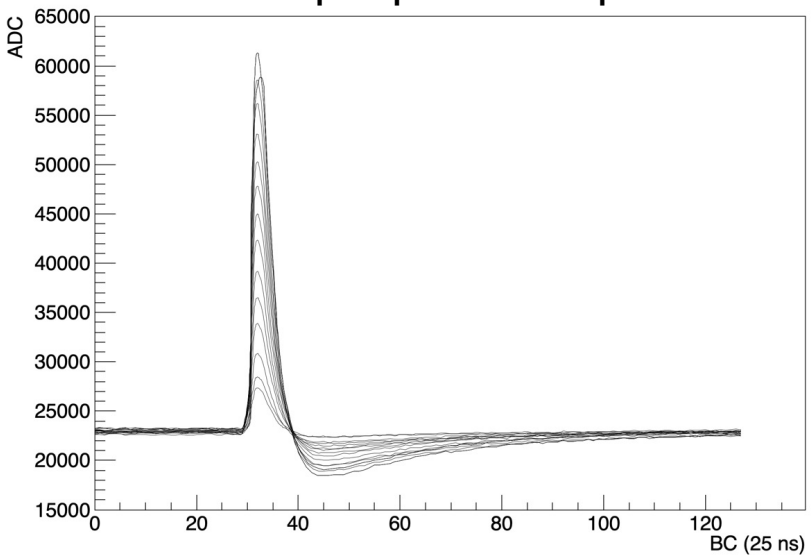
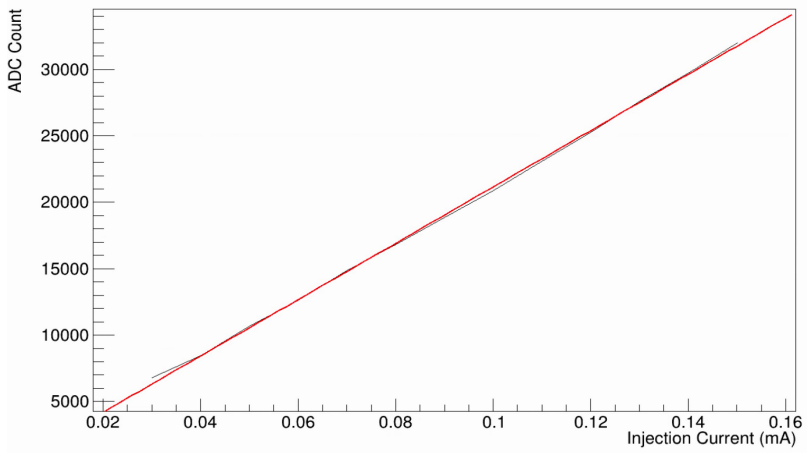
Selected Slice Test Board results

The Slice test board is used in our test stand to test the full characterization chain, develop the control and analysis software and identify bottlenecks for future test with multiple FEB2 in crate during production

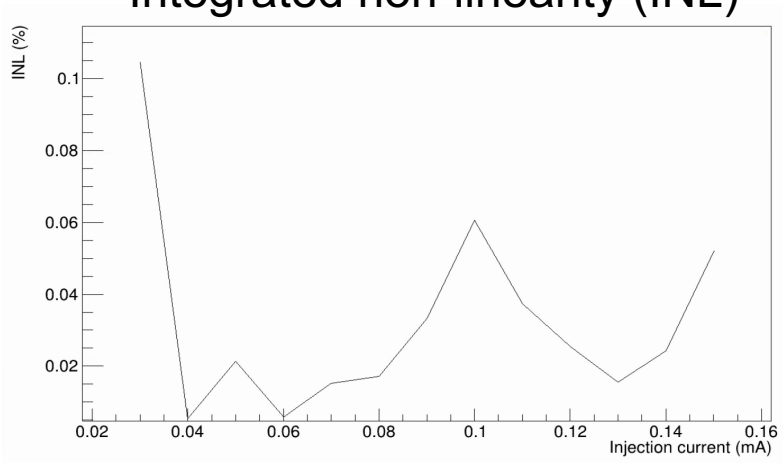
Example pulse shape



Linearity analysis



Integrated non-linearity (INL)



Approximated Current

Conclusion

The ATLAS LAr Calorimeter is undergoing an upgrade that will ultimately see the replacement of its entire readout electronics to cope with HL-LHC conditions and provide additional information to the trigger system

- Fully digitized readout upgrade aims at increasing the granularity of the calorimeter information to the level 1 trigger system
- Phase-II will replace all on-/off-detector electronics to provide full readout of the LAr Calorimeter at 40 MHz to the trigger and DAQ systems

The ASIC design work for the new on-detector readout is under way and mature prototypes of the preamplifier+ shaper and ADC ASIC have been tested and demonstrate the required performance for the Phase-II FEB2.

The Integration of the ASIC into the on-detector readout board takes place in multiple integration steps with increasing complexity, to exercise software and firmware, identify issues and prepare our infrastructure for the massive production required for FEB2. Off-detector work on timing system, signal processor and its firmware is also well on track.

Ευχαριστώ!