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Model of HgCdTe SWIR integration ramp for constant flux integration and persistence current

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For low flux Short Wave Infrared detection in astronomy, focal plane arrays are usually based on an HgCdTe detection layer flip-chipped onto a Silicon ROIC. To meet the low noise specification on these detectors, Source Follower per Detector (SFD) pixel architecture is maximizing the conversion gain, thus reducing the ROIC noise. However, this architecture gives intrinsically a non-linear conversion from accumulated charge to measured voltage during the integration. This non-linearity can be tedious to calibrate and leads to uncertainties on the estimated detected flux.

We propose a physical model to estimate such integration ramp from the initial voltage to its saturation. Applied on measurements performed on imagers manufactured at CEA and Lynred, we discuss on this approximation uncertainties and the way to constrain its physical parameters.

Based on this SFD pixel ramp modeling for a constant flux, we also address the persistence issue that plagues IR detectors for astronomy. The traditional hypothesis used to explain this phenomenon is based on trapping/emission processes from deep level defects in the space charge region (SCR) of the diode. Inspired from Deep Level Transiant Spectroscopy (DLTS) formalism, we developed a physical model describing trap emission current from the SCR of the diode in a SFD pixel. Reporting on point defect and extended defect, we found that this model can describe low persistence signal. However, the trap density has to be close to the doping density to account for higher persistence amplitude. This implies that the N region of the diode would be compensated, which is an extreme scenario out of the scope of this model.

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