Status of BNL Front End ASIC Design

V. Polychronakos

(On behalf of the Development team)

Outline

- Motivation/Requirements
- Example of existing IC – Model for the New Development
  - Some results – Proof of principle
- Effort to integrate both current and future IC tests to the SRS
- Status of the new IC development (Gianluigi de Geronimo)
  - Some general information on the BNL IC development process
  - Cost/Schedule for prototypes and production quantities
  - Status and schedule of the new chip

Some desirable features for muon upgrade detectors

- Data Driven System
- Real Time Peak Amplitude and Time Detection
  - Automatic, on-detector zero suppression
  - Dramatic reduction of data bandwidth
- Neighbor channel enabling circuitry (allows relatively high thresholds without losing small amplitudes)
- On-chip ADC (10-12 bits?)
- Simultaneous read/write with built-in Derandomizing Buffers
- 64 or 128 Channels/chip to match detector element size
- Able to provide Trigger Primitives for possible on-detector track segment finding logic
- Appropriate for a variety of detectors (mMegas, TGC, TPC, GEM, etc) requiring amplitude and time measurement
- Detailed Specifications to be finalized soon

Example of a BNL TPC ASIC

- Has some key features, peak detector with time stamp but otherwise not suitable for LHC
- Useful to demonstrate the principle
- Technology: CMOS *0.25μm – 2.5 V*
  - MiM capacitor and silicide block resistor options
- Power *43 mW*
- Front-End Channels 32
  - charge preamplifier
  - 2nd order shaping amplifier
  - peak detector
  - timing detector
  - Integrated calibration capacitor *250 fF* (σ=0.1%)
  - Shaping time *600 ns*
  - Channel gain *15mV/fC* to *32mV/fC*

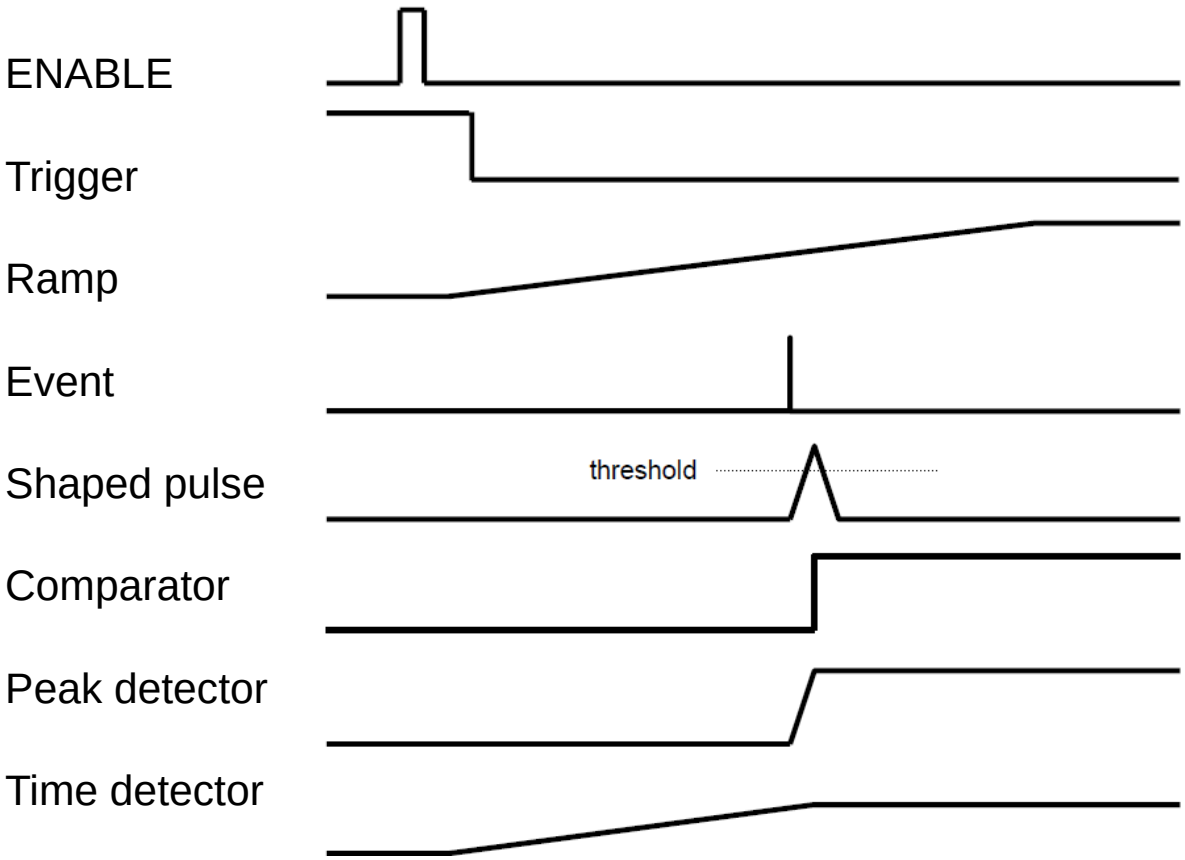
ASIC IC85 Time and Amplitude Measuring Chain

When an event occurs above threshold the discriminator fires and the peak and timing detectors are enabled

At the same time the peak and timing detectors of the two neighbor channels are enabled

The events in the three channels are processed for peak amplitude and peak timing

The two corresponding voltages are stored for each channel



On-chip zero suppression

Amplitude Time

Trigger ID

Strip addresses

Empty event

```
3263
13  0.210266  0.424957
14  0.370636  0.437927
15  0.225220  0.412750
3264
3265
0  0.284119  0.457306
1  0.435333  0.418854
2  0.313873  0.450287
3266
3267
…
3281
18  0.206909  0.261841
19  0.902252  0.404968
20  1.113892  0.397491
21  0.597534  0.394440
22  0.304718  0.355682
3282
13  0.225525  0.369110
14  0.406952  0.401764
15  0.382996  0.368195
16  0.225372  0.379486
…
```

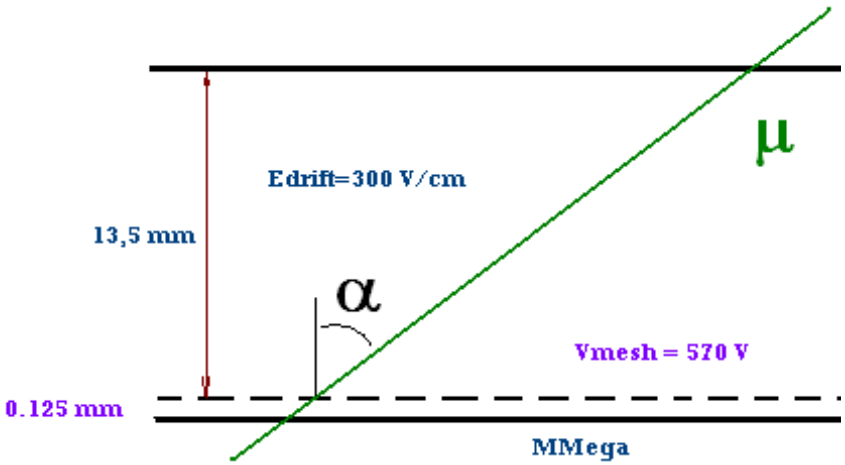
Automatic recording of neighbor strips when a channel exceeds hardware threshold

Testbeam data file run26

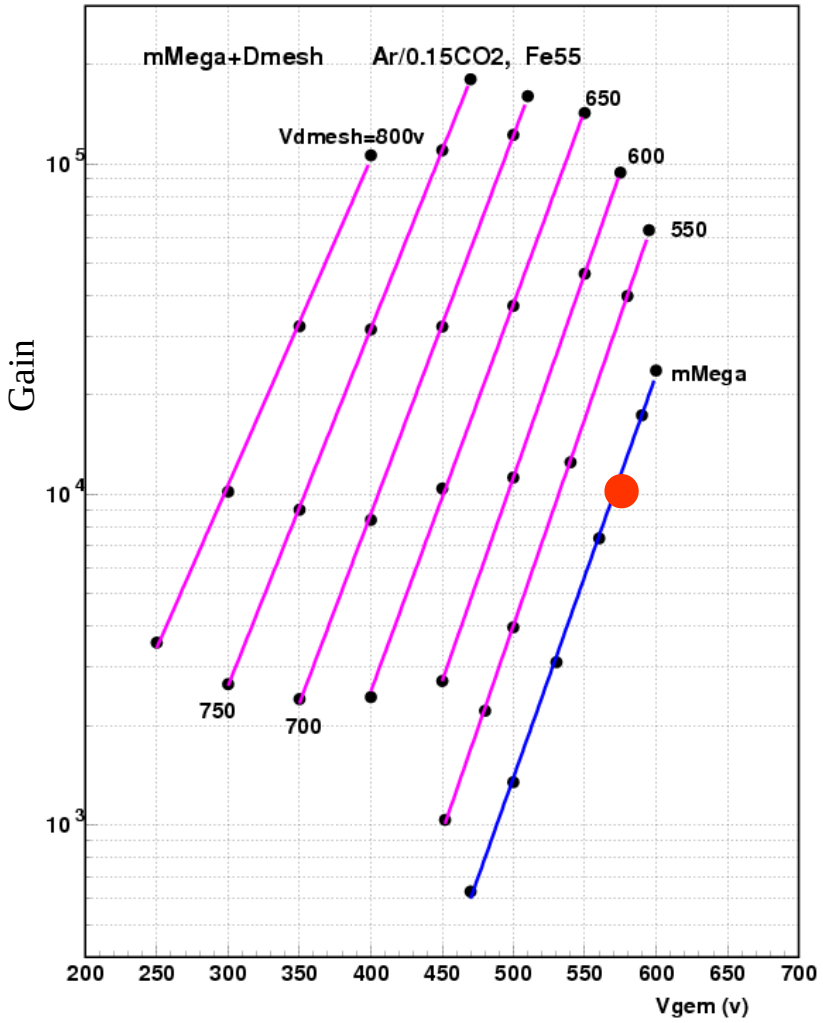
- **136K triggered events**
- **7.5 Mb ascii**
- **would be much smaller in binary**

"MicroTPC" Operation of mMegas Detector

E_{drift} 300V/cm V_{drift} ~2cm/μs
V_{mesh} 570 V

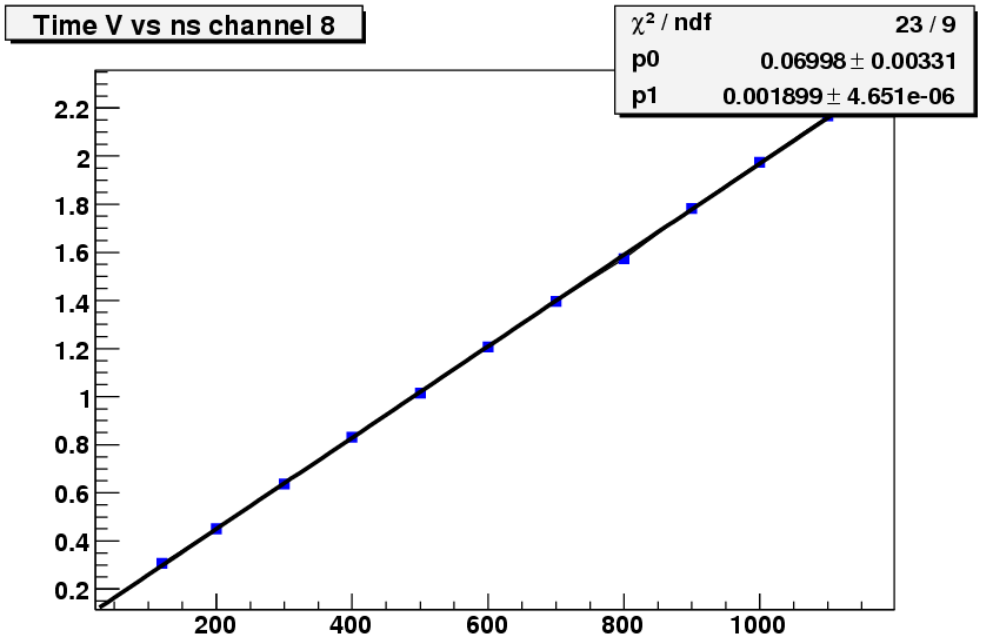


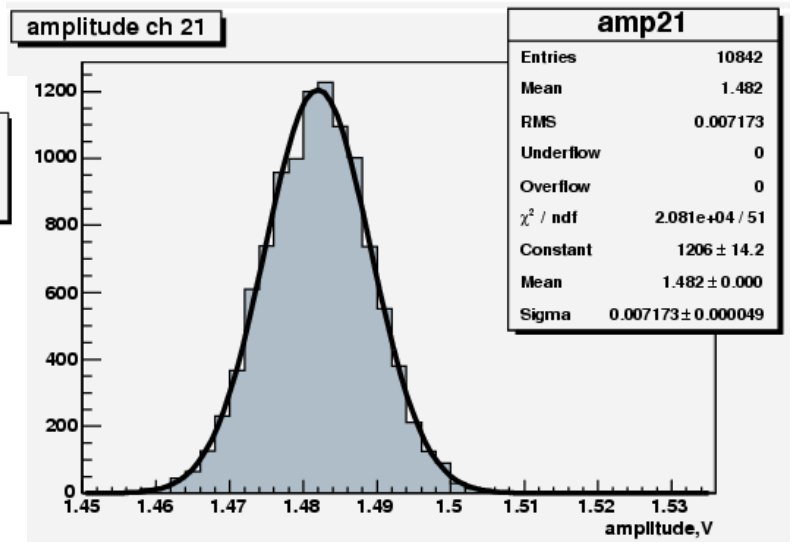
Gain $4 \cdot 10^3$

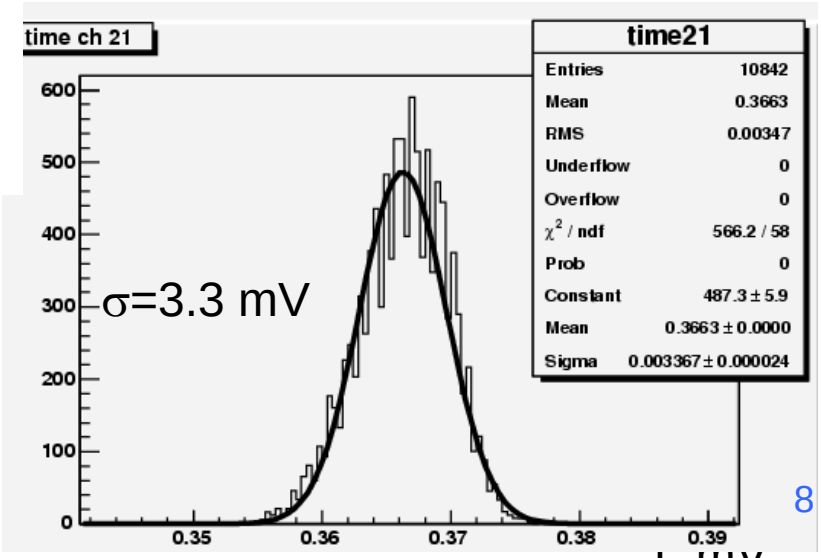


Timing Resolution

Shown for T_{delay} = 150 ns

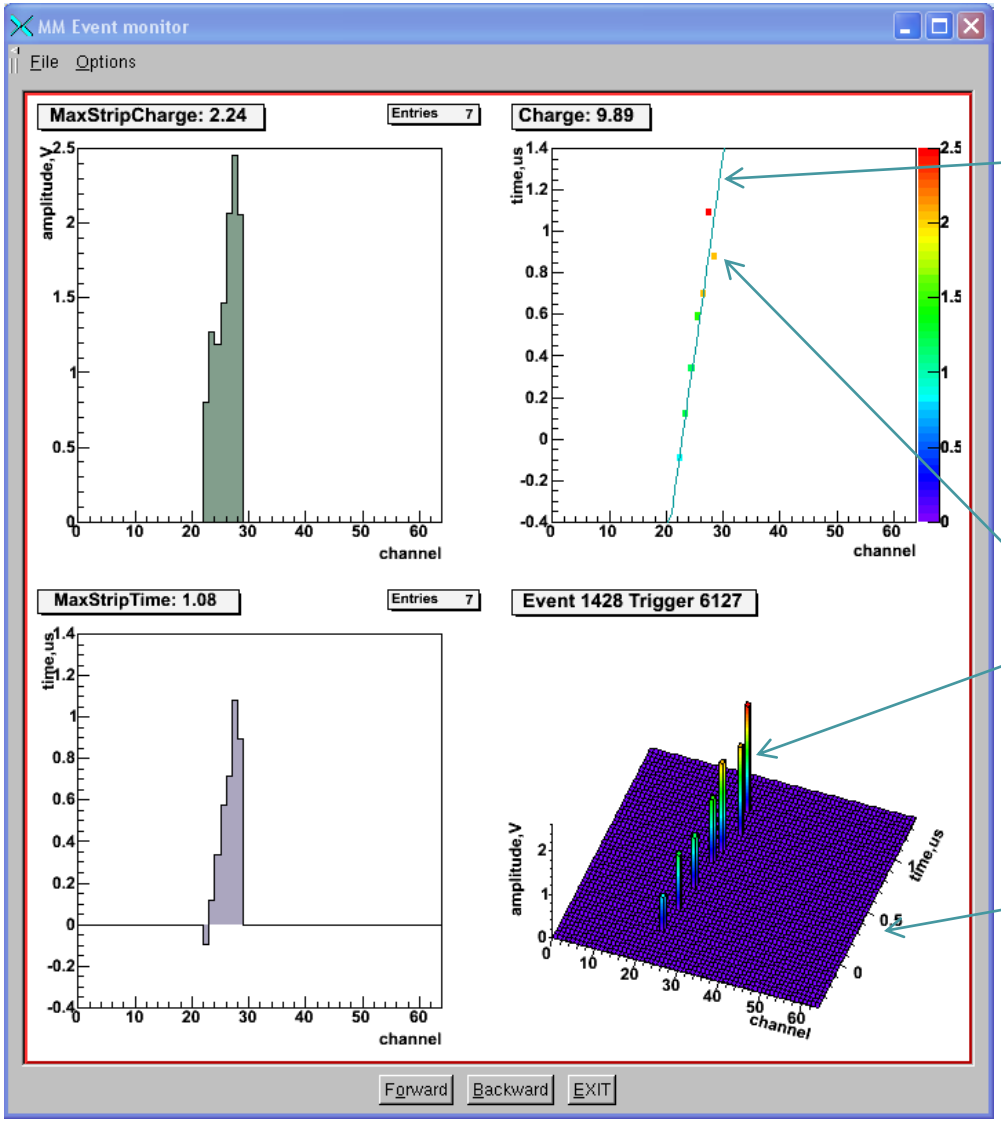




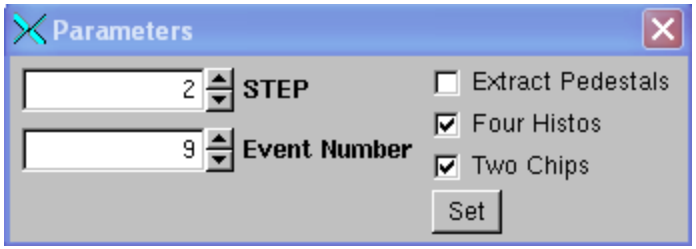


1mV = 0.52 ns

Event Display



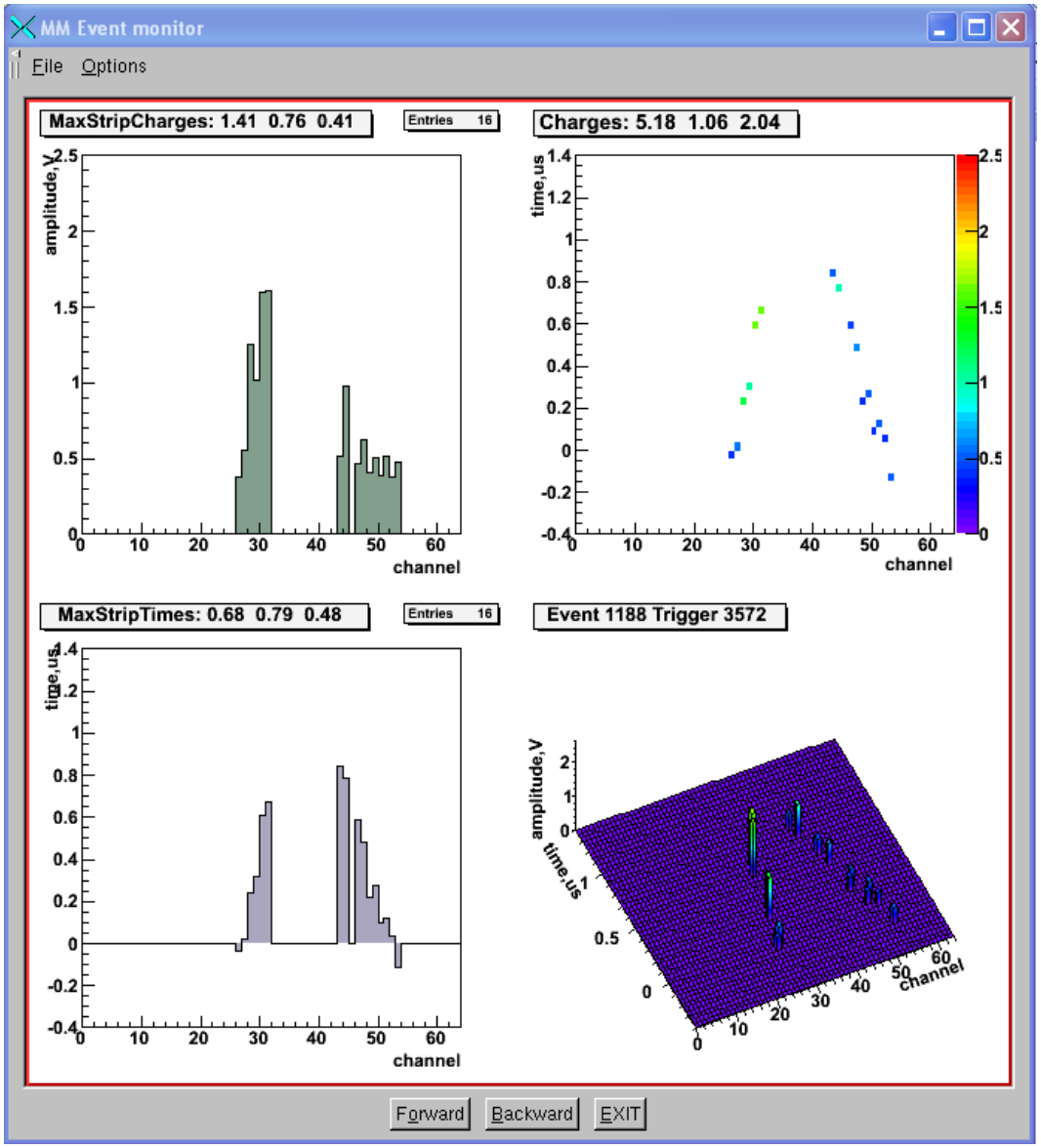
Tracking done on-line



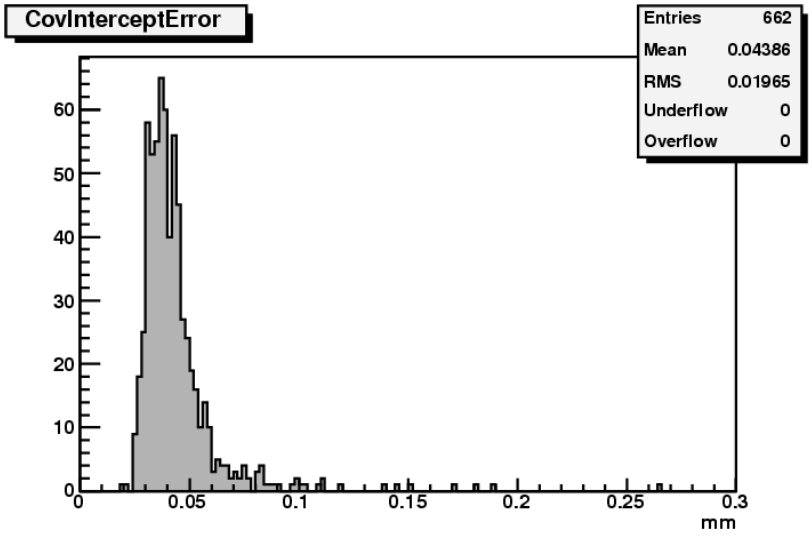
Te same color palette used

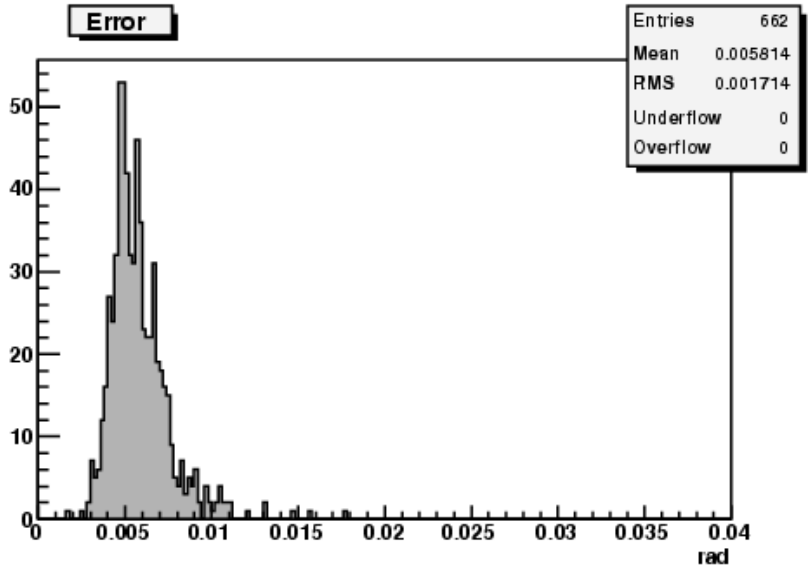
3D Object

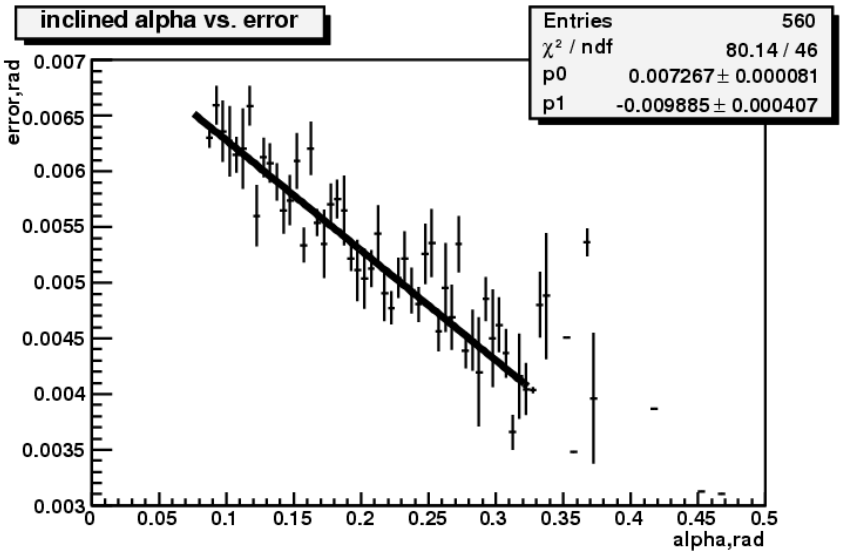
Double Track Events



Precision in determining angle and position







C-Card Goal

- This project is to design and build a C-card to facilitate testing of BNL ASICs for micromegas detectors
  - The first C-card will be used to digitize data from the BNL MMC1 card ("hybrid card") that contains two TPCV3 ASICs
    - In the intermediate term, the C-card will be used to digitize data from the next generation (analog) BNL ASIC
    - In the longer term, the C-card will evolve into a front end card containing the final BNL (analog plus digital) ASIC for micromegas

C-Card Specification

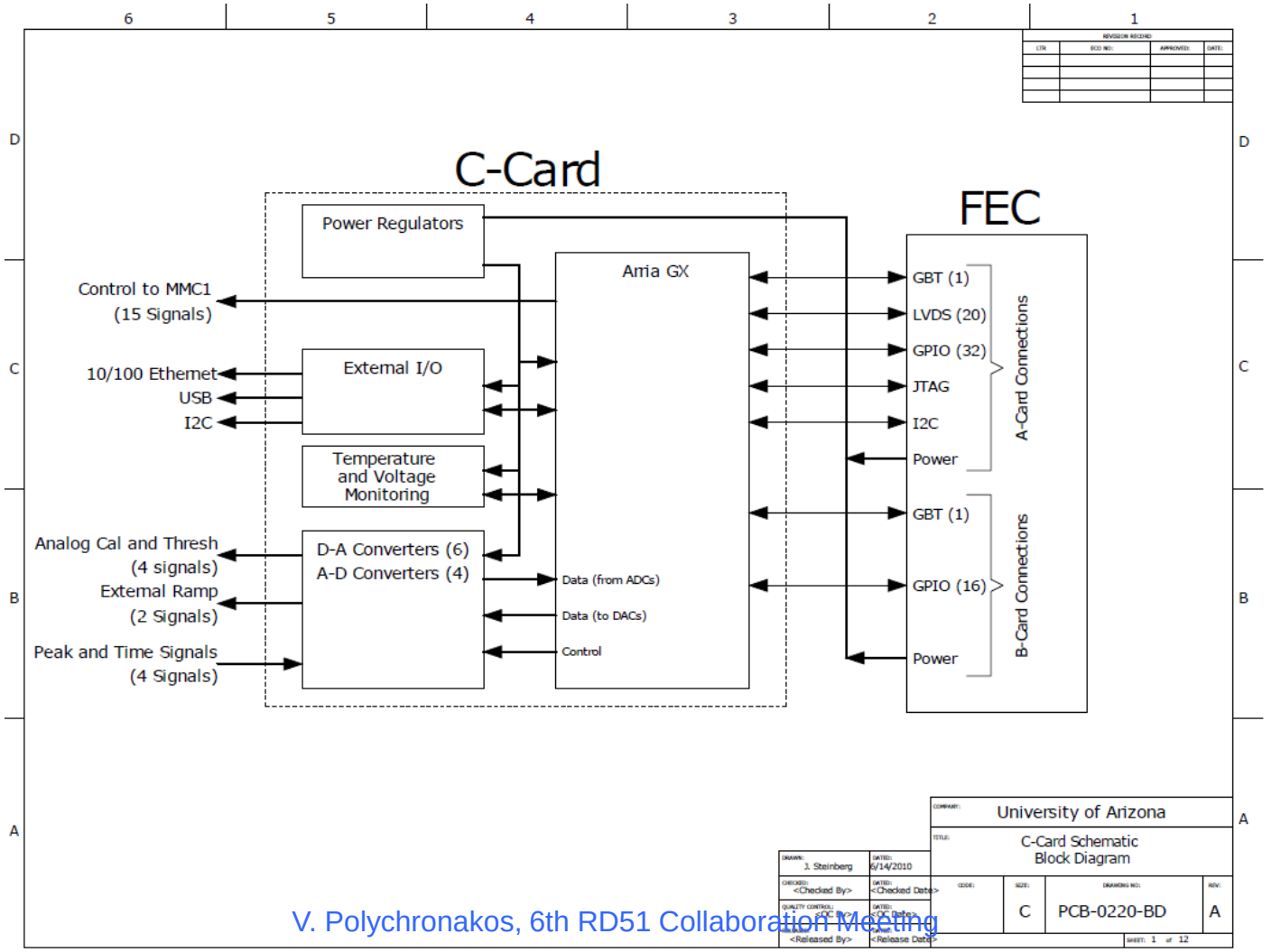
Ken Johns, Joel Steinberg, Dan Tompkins

(U. Arizona)

- Will control and acquire data from the MMC1 card (BNL)
- Will transfer digitized and formatted data to the FEC card (Valencia) and SRS (Scalable Readout System) (CERN)
  - This will be the default test beam DAQ system for micropattern detectors at CERN for the next several years
- Will also operate in a standalone mode for debugging and limited DAQ in the lab without FEC card and SRS system

C-Card Progress

- Schematic in progress



BROOKHAVEN NATIONAL LABORATORY

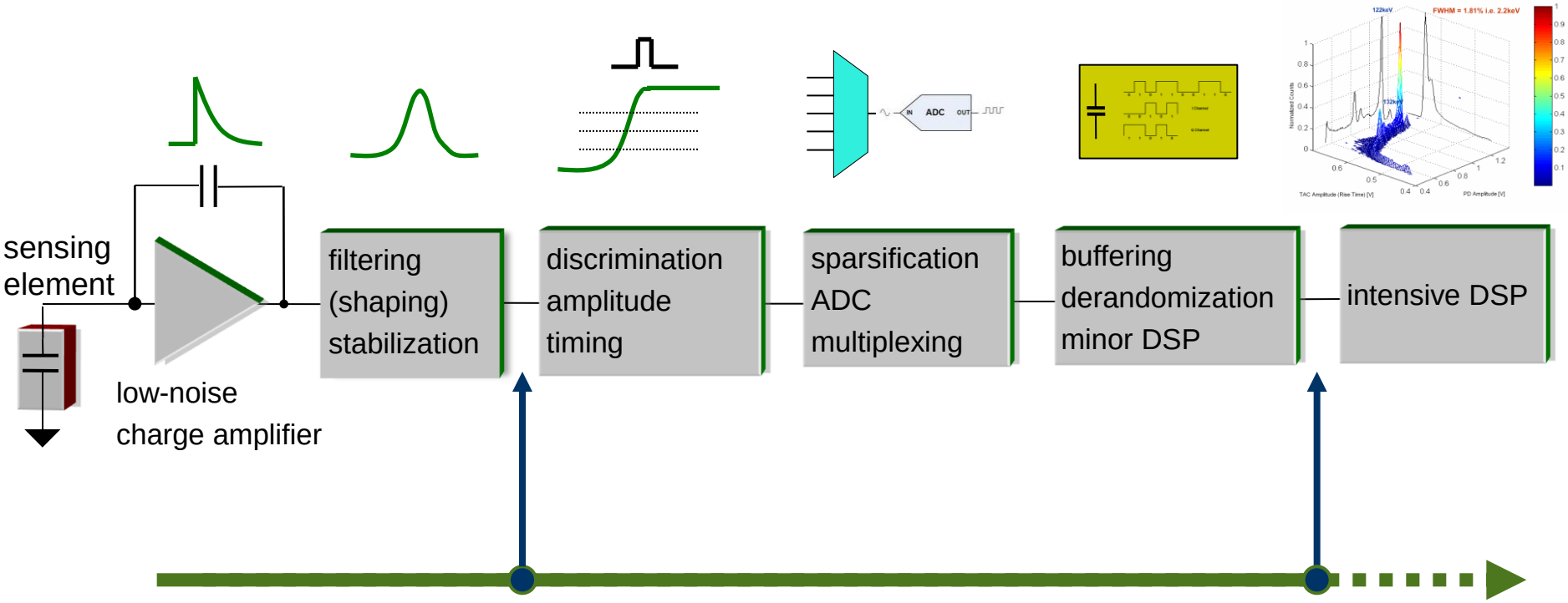
managed by Brookhaven Science Associates
for the U.S. Department of Energy

Gianluigi de Geronimo

- VMM1 ASIC
- Front-end IC for Charge-interpolating Position-sensitive Detectors
- Could work for both TGC and Micromegas Detectors

...
Instrumentation Division
BNL

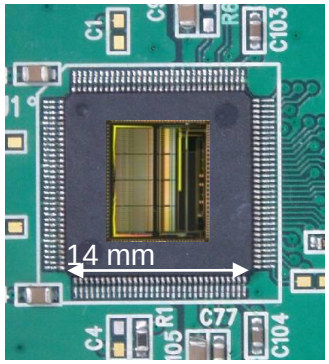
Typical front-end electronics channel



Application Specific Integrated Circuits

(in BNL since early '90 with Paul O'Connor)

year 2000
- 500 nm technology
- 16,000 transistors
- 16 channels
- analog

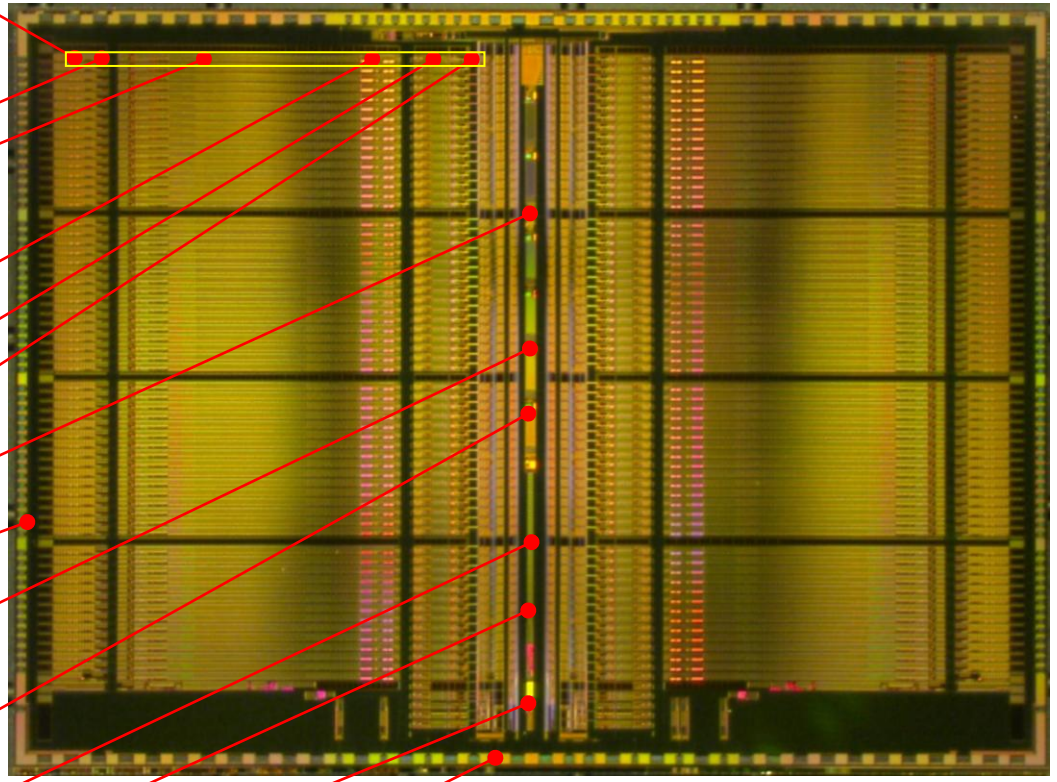


64-ch ASIC for Neutron Detectors

year 2009
- 130 nm technology
- > 1M transistors
- > 100 channels
- analog and digital (mixed-signal)

Subcircuits

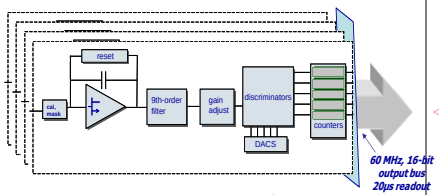
- Low-noise, low-power charge amplifiers
  - gas, liquid, solid state detectors
  - capacitances from 10^{-14} to 10^{-8} F
- Switched and continuous adaptive reset
- High-order filters, stabilizers, drivers
  - peak time / gain adjustment
- Single- and multi-level discriminators
- Peak and time detectors, derandomizers
- Analog memories and multiplexers
- Counters and digital memories
- Configuration registers
- ESD protections
- Calibration pulse generators
- Analog-to-digital converters
- Digital-to-analog converters
- Precision band-gap references
- Temperature sensors
- Readout control logic
- Low-voltage differential signaling
- Current-mode analog and digital interface

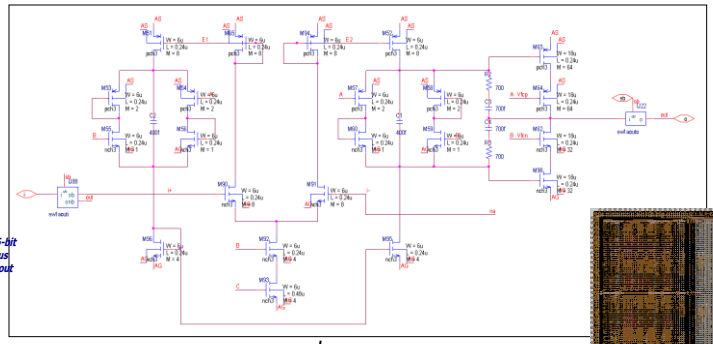


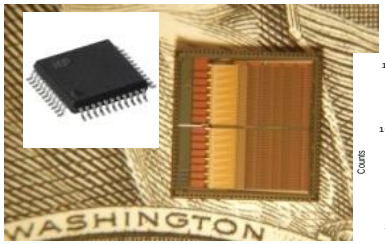
ASIC for 3D CZT
Position Sensitive Detectors
- 128 channels
- 2 mW/channel
- 13 x 10 mm²
- 300,000 transistors
- CMOS 250 nm

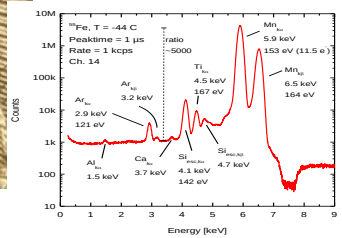
Functionality and complexity increase by the years

ASIC Design Flow









design phase	system level design	transistor level design	masks layout	fabrication	tests
months	~ 2	~ 6	~ 2	~ 3	~ 2

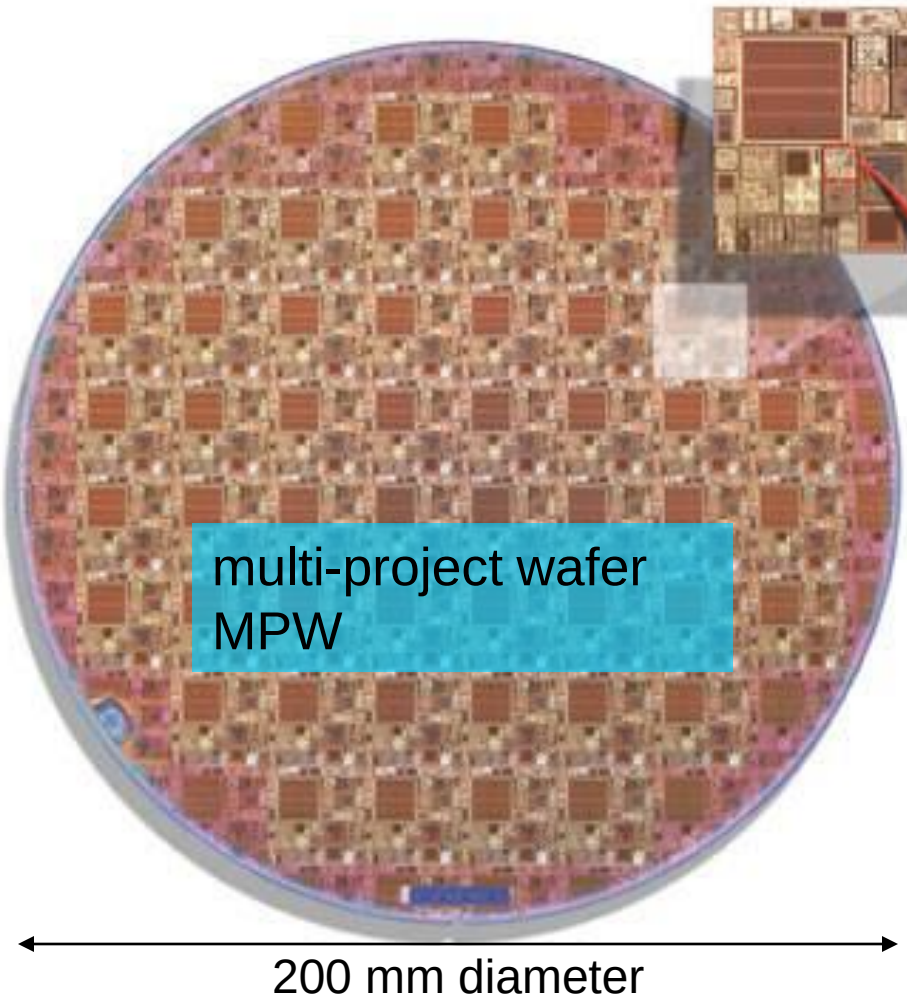
revision cycle

From concept to ready-for-production:
1 - 2 cycles, 2 - 3 years, 3-6 FTE (depending on complexity)

Higher functionality and complexity means more resources and expertise , higher risk, longer development time

ASIC Fabrication : Prototyping

Major foundries accept designs from multiple customers (MPW)

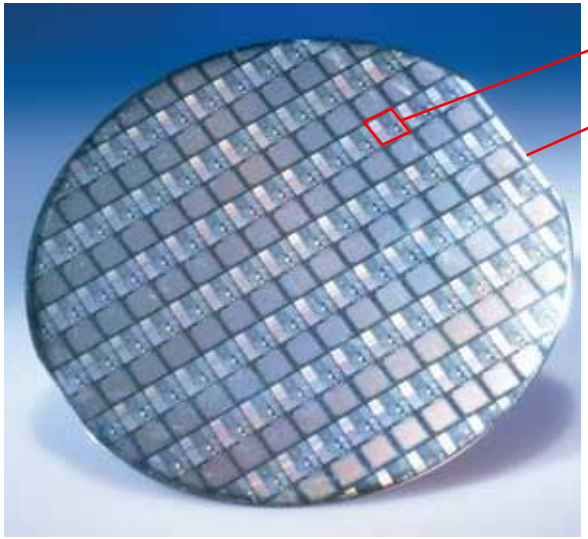


	MPW	dedicated
cost [k$]	10 to 100	150 to 1500
samples	tens	thousands

ideal for prototyping and low volume

ASIC Fabrication : Production

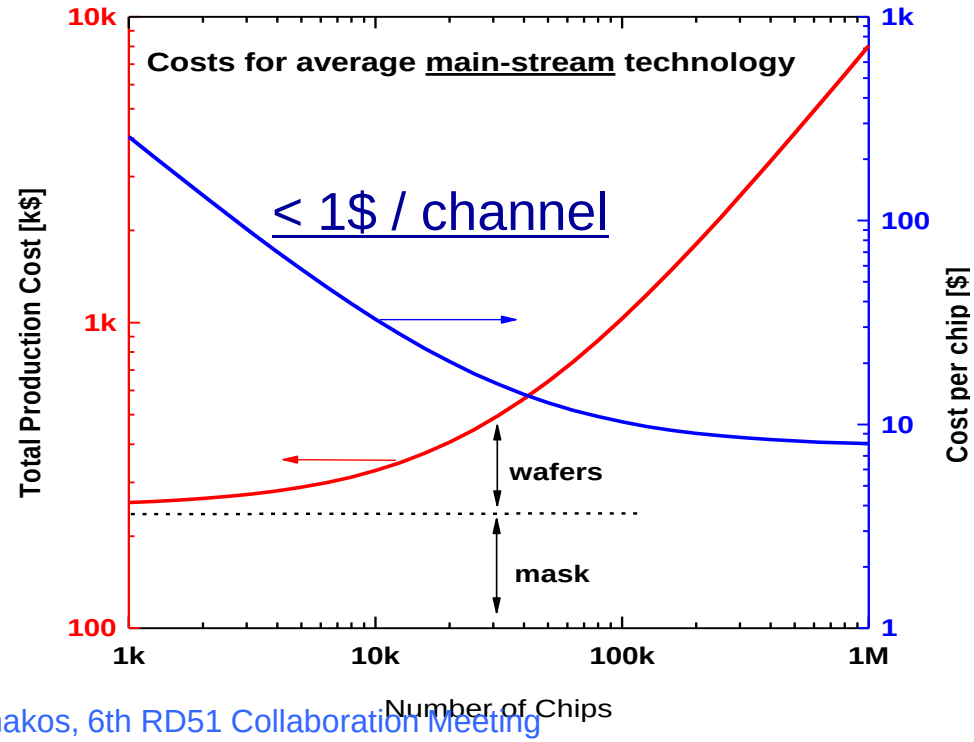
Major foundries accept purchase of dedicated run



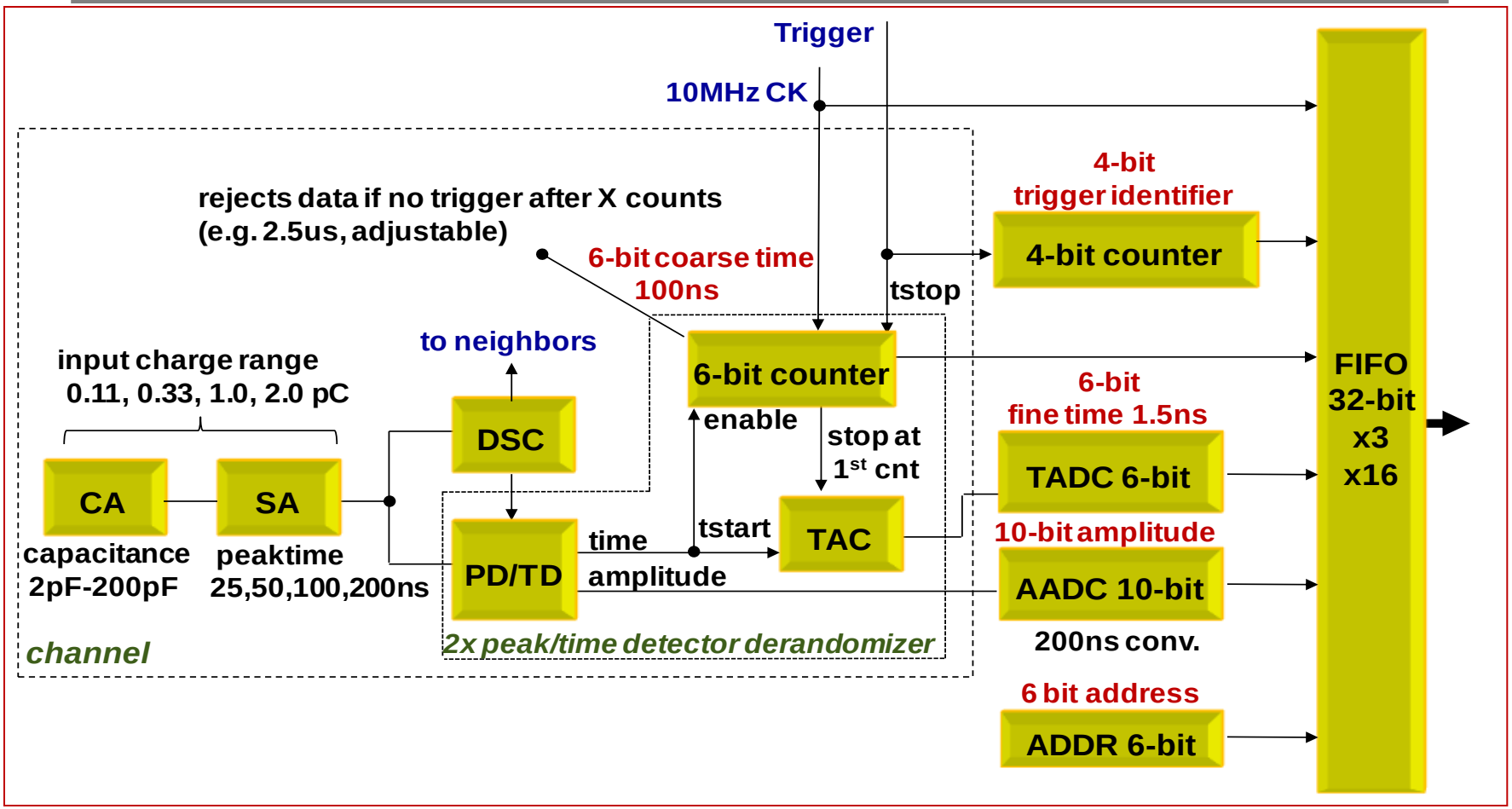
4-10 chips in a ~20x20 mm^2 reticle

~ 55 reticles per wafer

	cost [k$]
mask	100 to 700
each wafer	1 to 10



VMM1 ASIC: Architecture



- 64 channels
- adj. polarity, adj. maximum charge (0.11 to 2 pC), adj. peaktime (25-200ns)
- derandomizing peak detection (10-bit) and time detection (1.5ns)
- integrated threshold with trimming, sub-threshold neighbor acquisition
- integrated pulse generator and calibration circuit
- analog monitor, channel mask, temperature sensor
- continuous measurement and readout, derandomizing FIFO
- few mW per channel, chip-to-chip (neighbor) communication, LVDS interface

VMM1 ASIC: Schedule and Status

	schedule	status/notes
Analog section	Jul-Oct 2010	**in progress**
Peak/time detection	Nov-Dec 2010	scheduled
Digital section	Jan-Feb 2010	scheduled
Physical layout	Mar-May 2010	scheduled
Fabrication 1st prototype	**Jun-Sep 2010**	CMOS 130nm, 1.2V, MPW

Analog section:
transistor-level simulations
power ≈ 4 mW