

# Status of the APV25 electronics for the GEM tracker at JLab

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On behalf of:

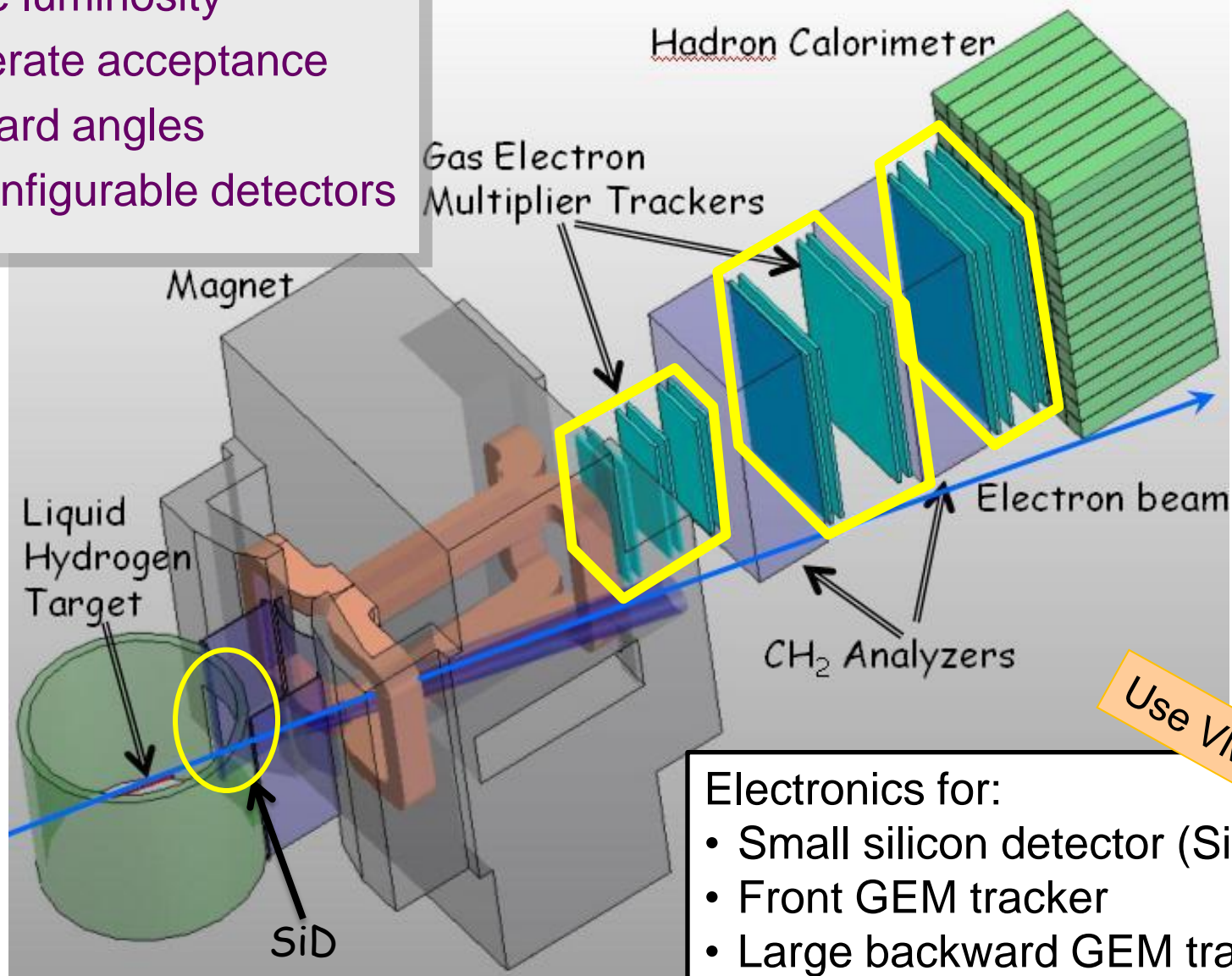
Paolo Musico, Saverio Minutoli, Giuseppe Gariano - INFN/GE

Bari 09/October/10

WG5-RD51 Collaboration Meeting

# SBS Spectrometer in Hall A

- Large luminosity
- Moderate acceptance
- Forward angles
- Reconfigurable detectors

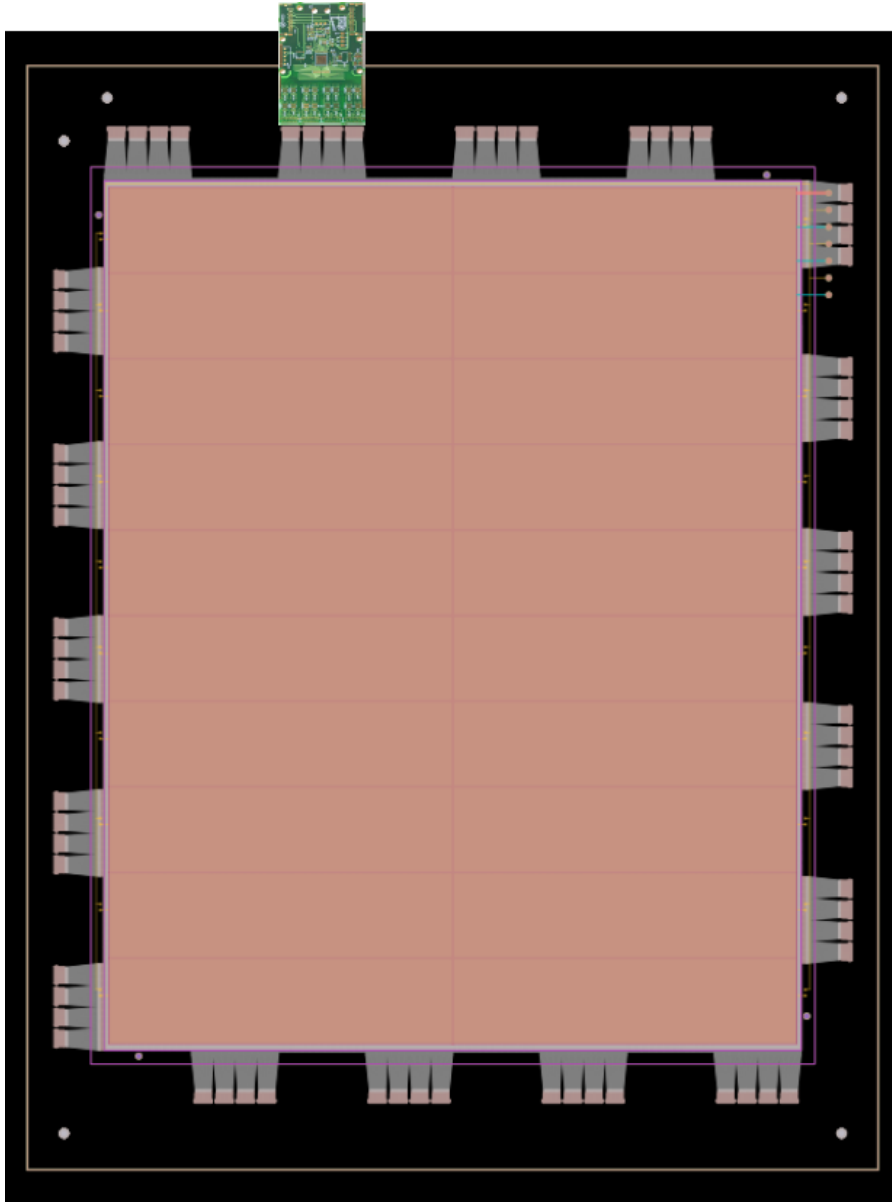


Electronics for:

- Small silicon detector (SiD)
- Front GEM tracker
- Large backward GEM trackers

⇒ **>100k channels**

# Readout Foil

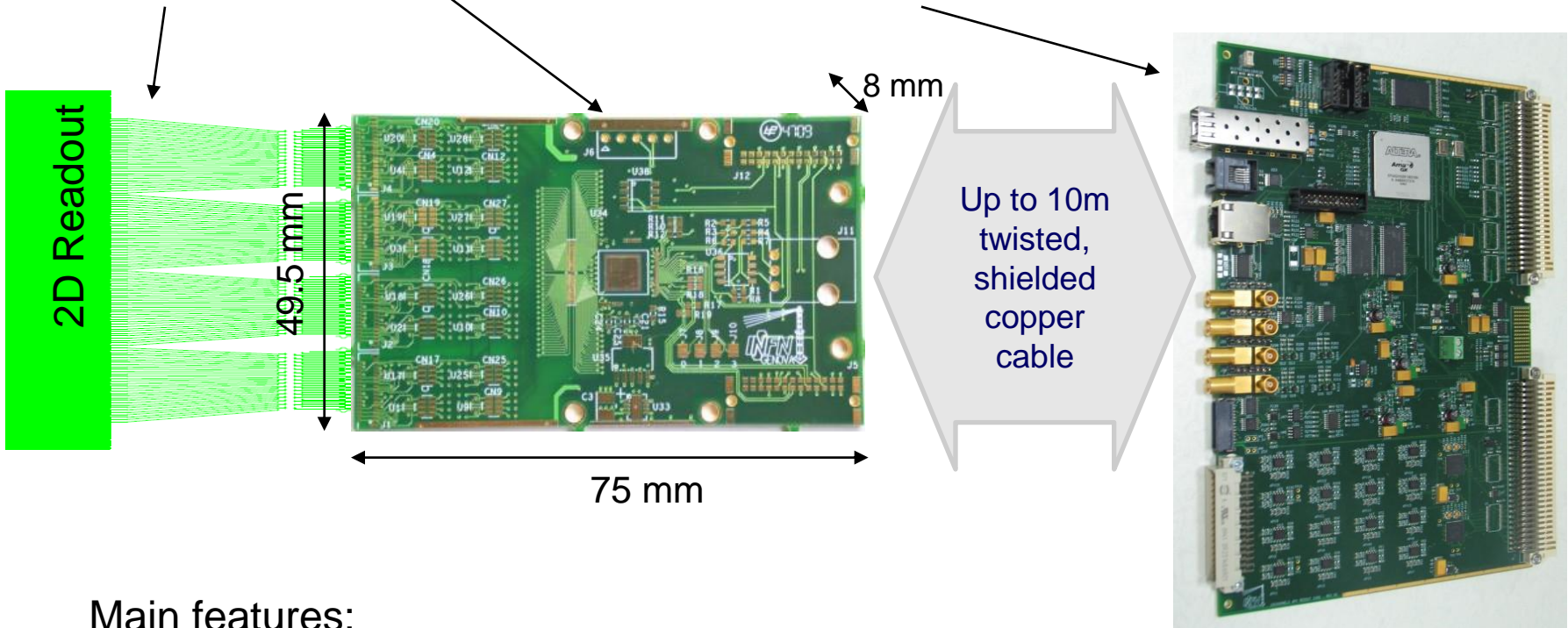


No soldering, very thin connections  
Laser cutting required



# Electronics Components

GEM ⇒ FEC ⇒ ADC+VME Controller ⇒ DAQ

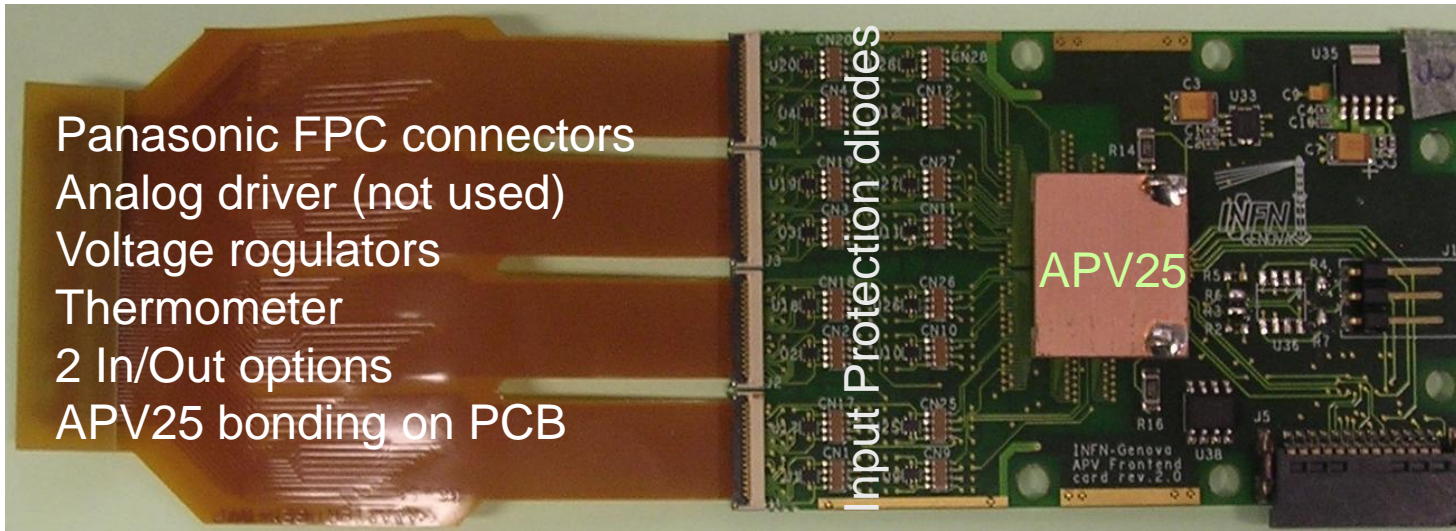


Main features:

- Use analog readout APV25 chips
- 2 active components: Front-End card and VME64x custom module
- Copper cables between front-end and VME

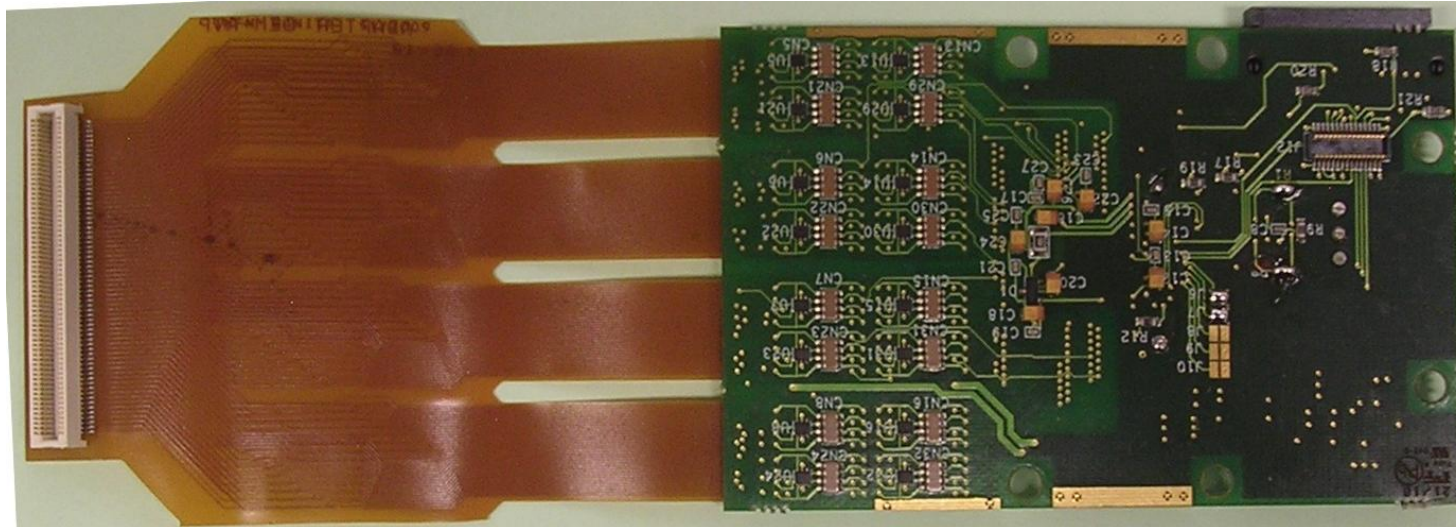
# Front End Card (Proto 1)

GEM  $\Rightarrow$  **FEC**  $\Rightarrow$  ADC+VME Controller  $\Rightarrow$  DAQ



Analog Output

Digital Input + Power supply



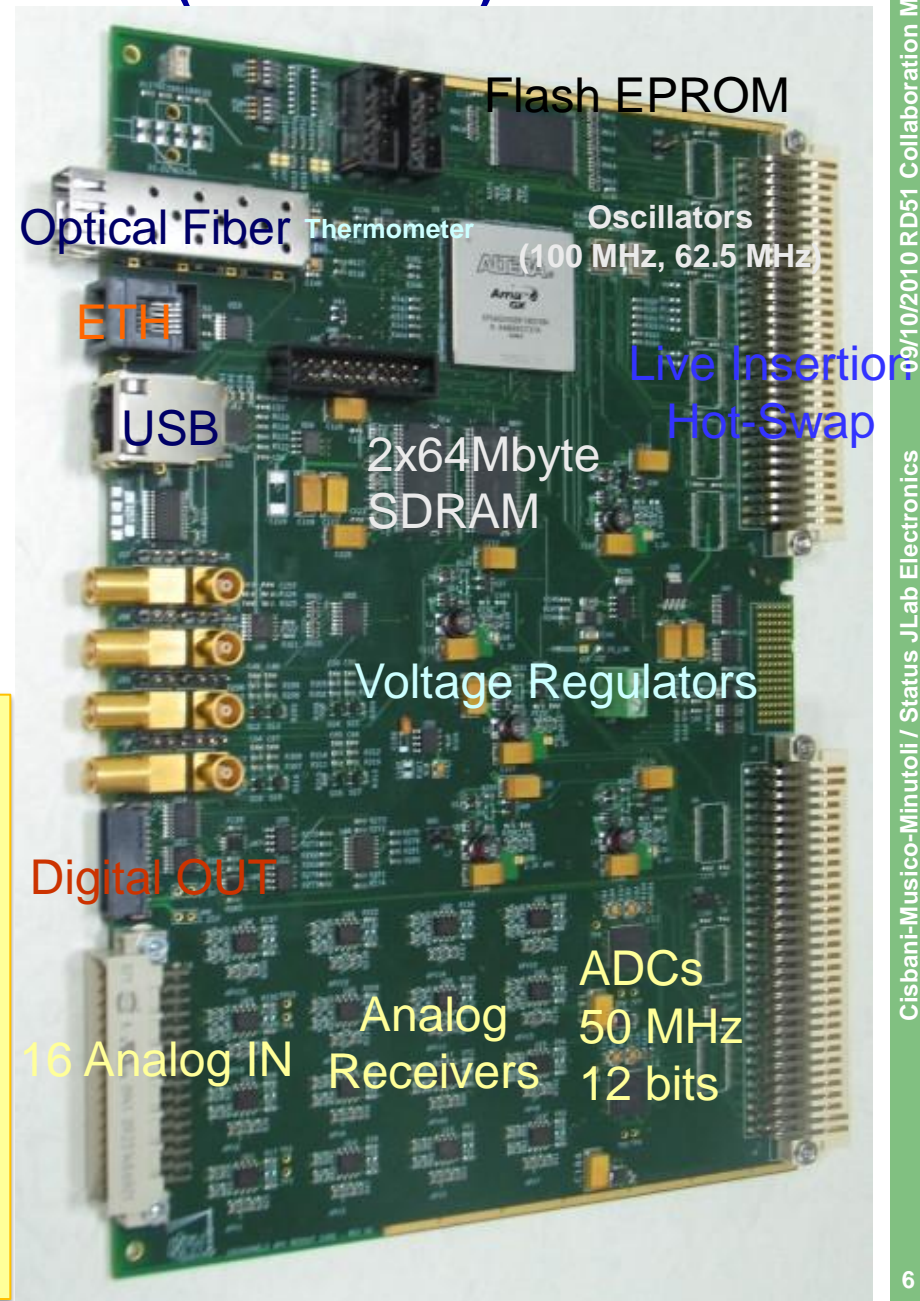
Analog out + Digital Input + Power supply



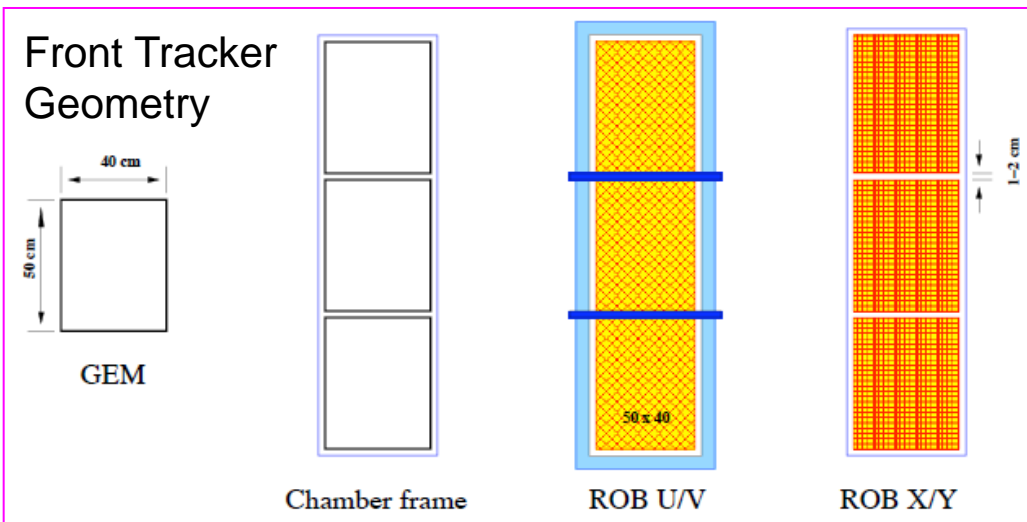
# VME64x Controller (Proto 0)

- VME controller hosts the digitization of the analog signals coming from the front-end card.
- It handles all control signals required by the front end cards (**up to 16 FE**)
- **Compliant to the JLab/12 VME64x VITA 41 (VXS) standard**
- We intend to make it accessible by standard VME/32 as well

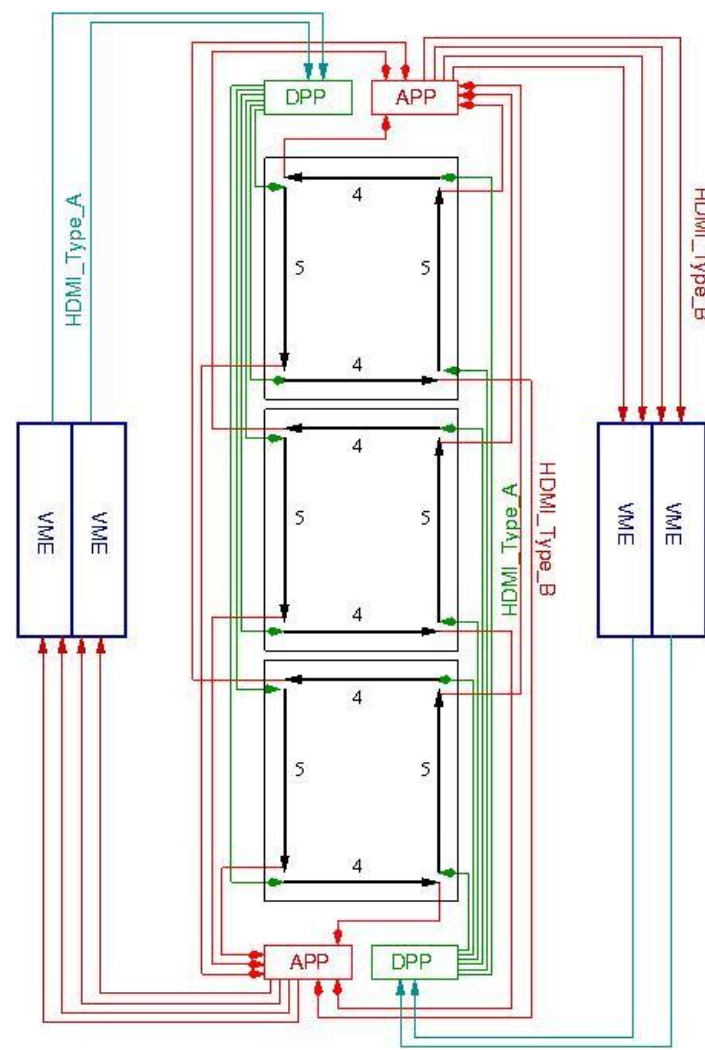
- **Version 1 submitted for production:**
  - Minor bug fixed
  - 2 HDMI-type A: digital lines + 2 analog lines (compatible with SRS hybrids connector)
  - 2 HDMI-type B: 16 analog lines
  - Added delay line for clock-convert phase fine tuning (DELAY25 from CERN)



# GEM Electronics Layout

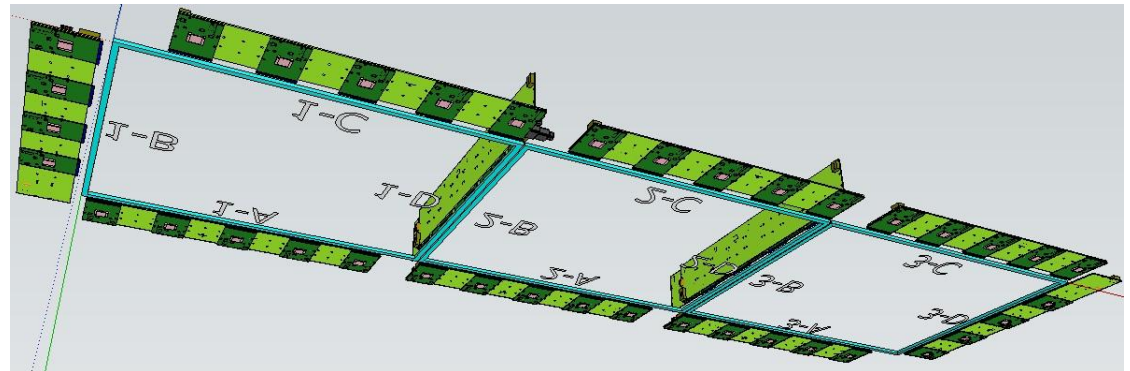
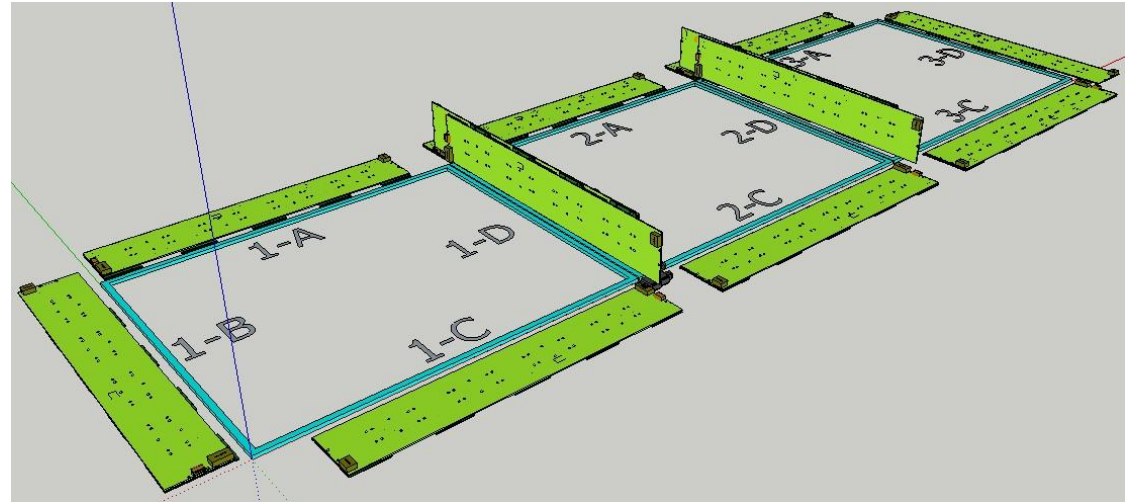
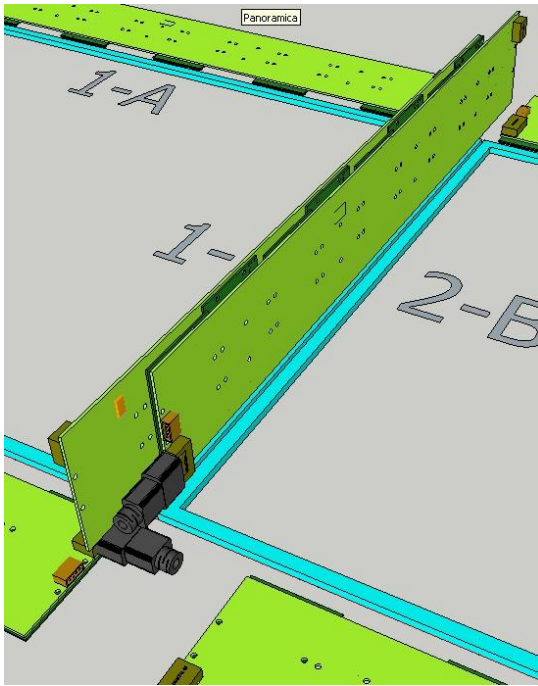


1. Use high density, high quality, standard HDMI (A-type for digital signals, B-type for analogo output)
2. Analog and digital lines rus independently
3. Analog and Digital patch panels collect and reroute channels
4. Similar solution for the SiD planes



VME ⇔ Patch Panel ⇔  
Backplane ⇔ Front End Cards

# Electronics layout on one chamber



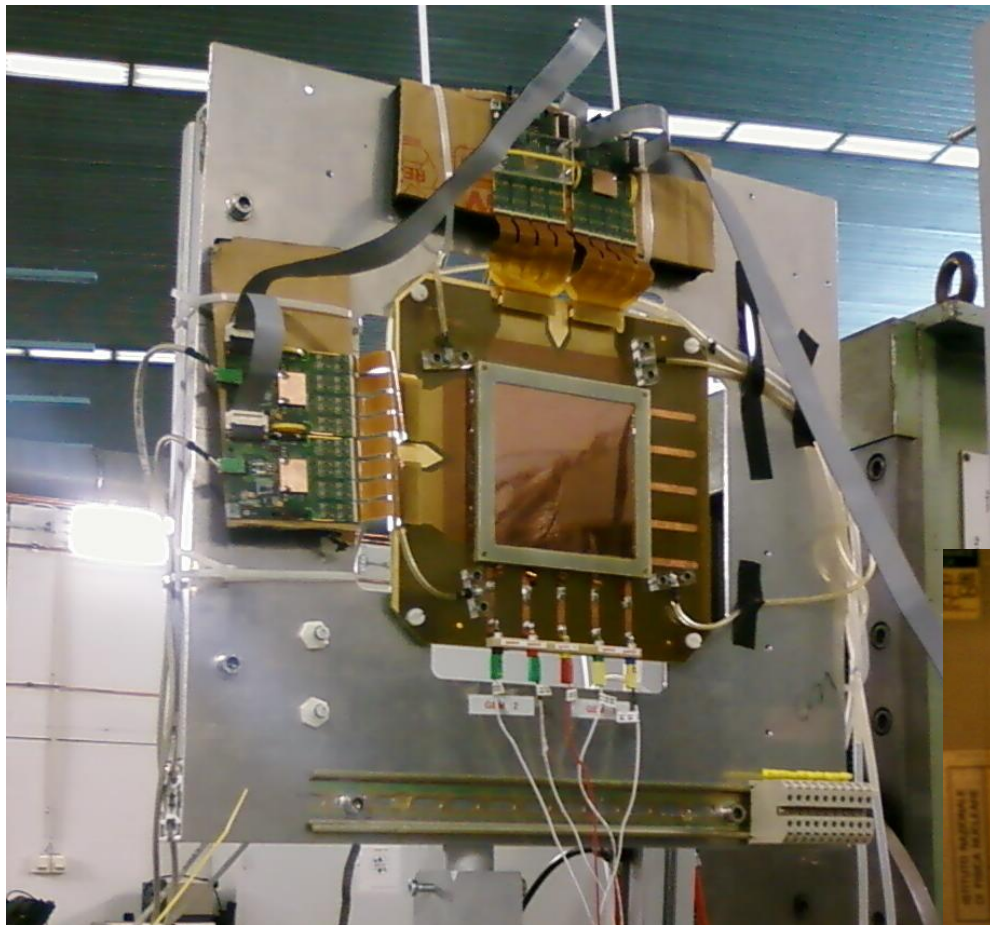
Cards and modules are supported by an **outer carbon-fiber frame** which runs all around the chamber.

Front-end cards are electromagnetically shielded by backplane and carbon-fiber (with thin conductive tape)

Power dissipation to be verified



# Beam test @ DESY (EUDET support)



2xGEM 10x10 cm<sup>2</sup> chamber

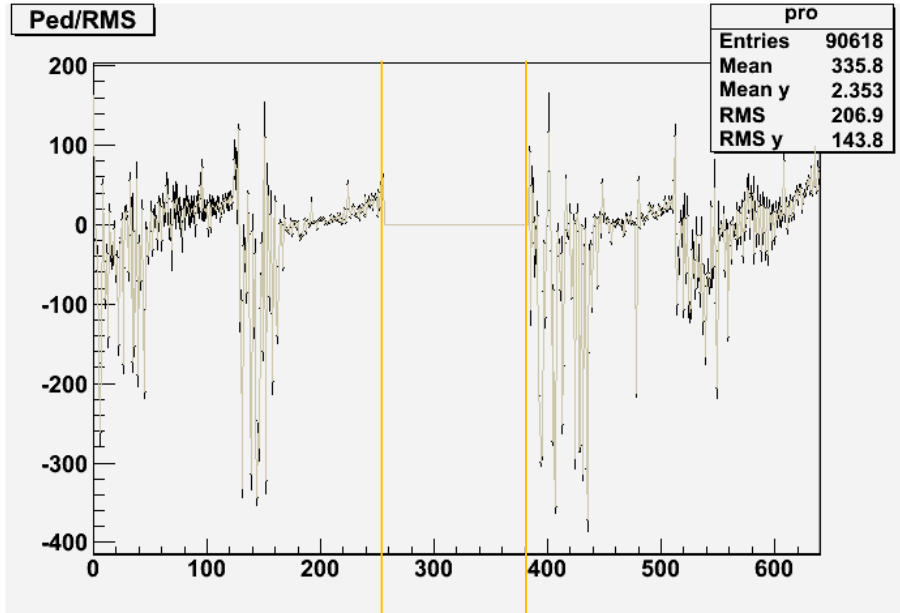
2D readout (a la COMPASS)

4 front-end cards (proto 0)

Low intensity electron beam 2-6 GeV/c

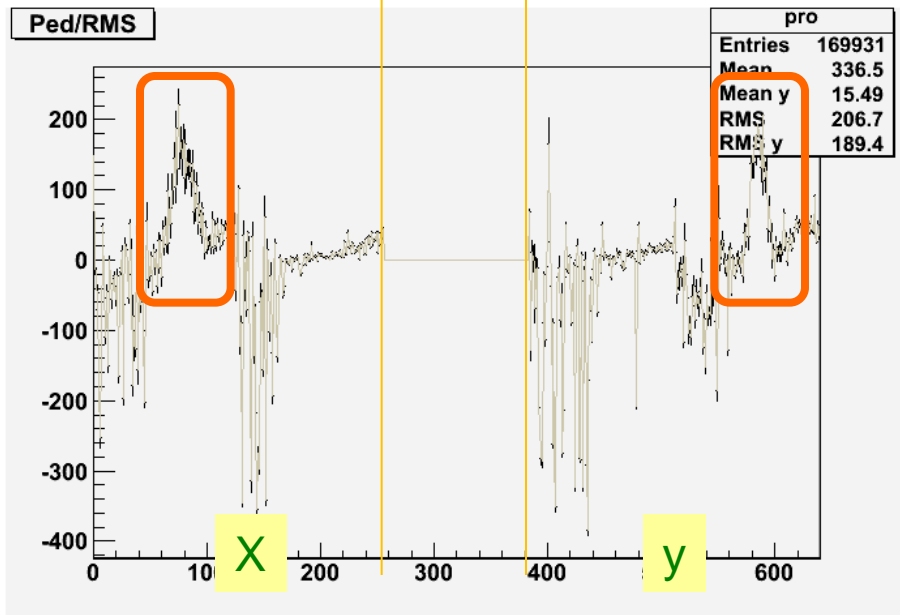


# Test Beam / Evidence of the beam



← No BEAM

Relevant noise, partially suppressed by common mode (offline) subtraction

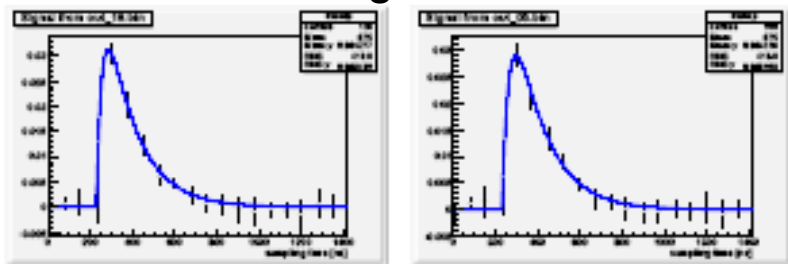


← BEAM

Large pedestal fluctuation

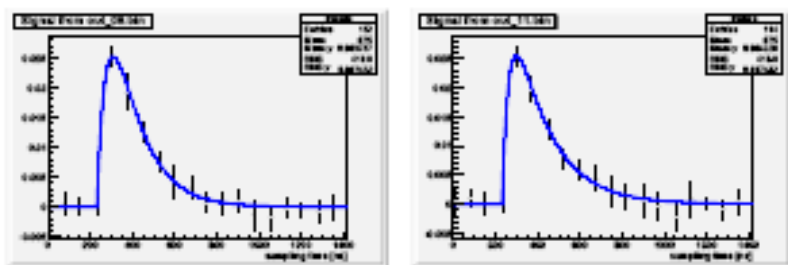
# Signal vs Cable length

Test signal



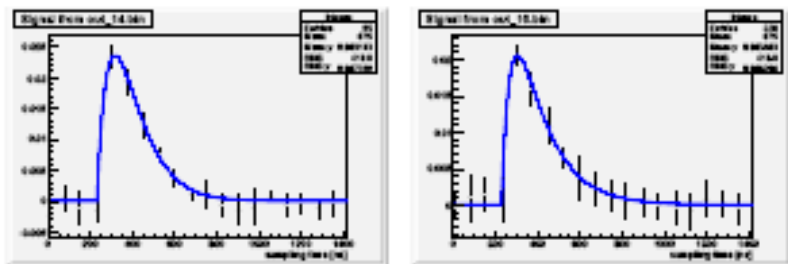
3 m

6 m



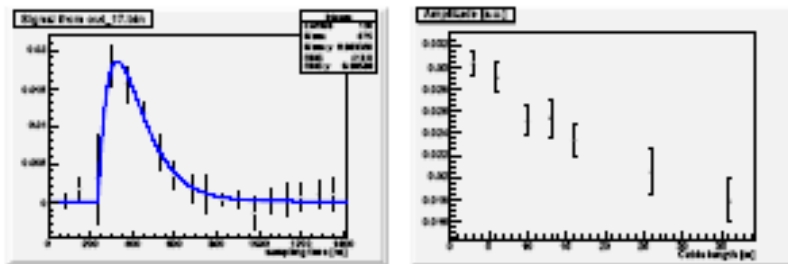
10 m

13 m



16 m

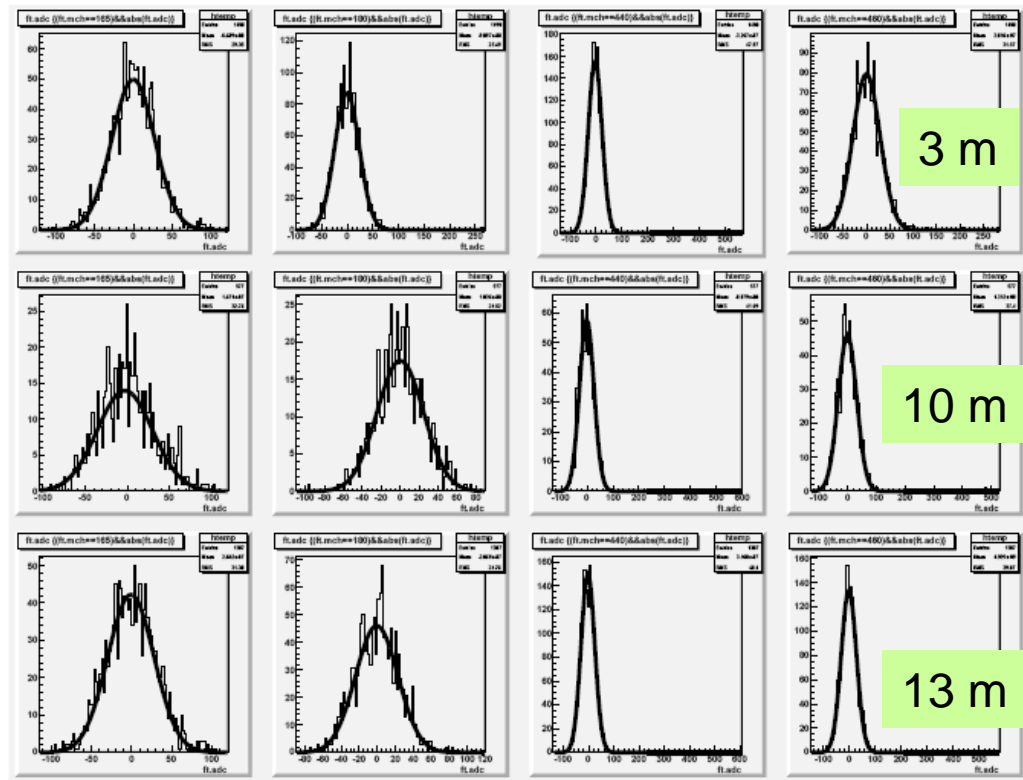
26 m



36 m

Amplitude

Pedestals



3 m

10 m

13 m

⇒ Long cables seems to work well: no distortion, noise slightly increase, amplitude attenuation as expected

Capacitance coupling to be optimized (in final size chamber)

APV25 parameters to be tuned!



# To do list

- Hardware
  - Improve noise (capacitor tuning, grounding ?)
  - Test new prototype version of the VME module
- Firmware
  - Continue bug fixing
  - Improve event builder (consistency data check)
  - Use of external RAM memory
  - Mean/Median evaluation and common mode subtraction on FPGA
  - Zero suppression

# Conclusions

- Front-end card:
  - Second prototype tested
  - Can be considered final version
- VME-controller:
  - Bug fixed
  - Most of the basic firmware implemented
  - New version under production
- Working on noise
- Expect to operate the new prototype in first 40x50cm<sup>2</sup> GEM in November; do beam test end of November