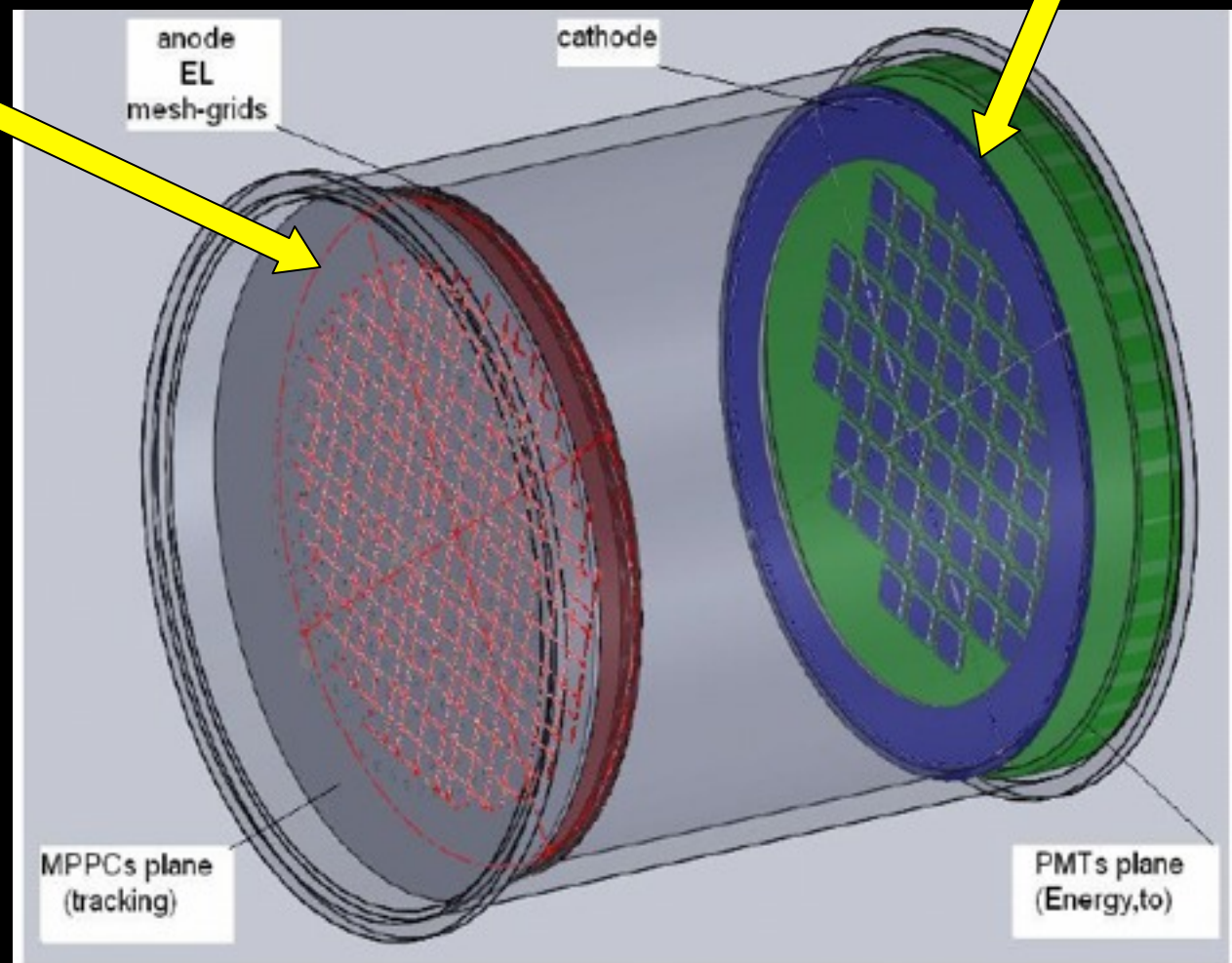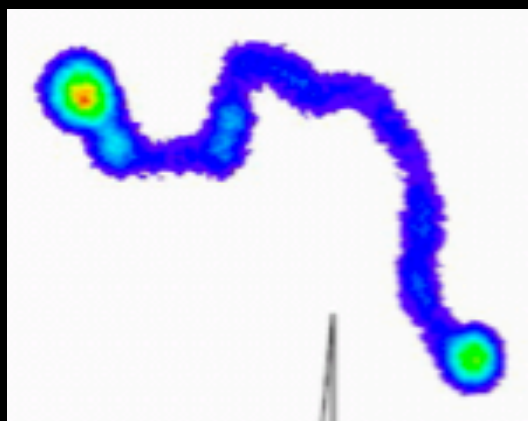# An SRS DAQ for NEXT-1-EL

J. Toledo

RD51 meeting - Bari, October 2010

# NEXT-1-EL

- NEXT is a bb-0n experiment based on a Gas Xe TPC

- NEXT1-EL is a small electroluminiscent TPC prototype:
  - t0 and energy are measured by 19 PMTs
  - 300 SiPMs for tracking

# NEXT-1-EL

- **PMT FE**: dual path per channel (E, t0) amp + shaper
  - 19 + 19 analog outputs
  - 3 CERN ADC C-cards needed to digitize all 38 ch
  - 3 FECs needed

- **SiPM FE**: amp + gated integrator + digitizer + LVDS ouput
  - Digital outputs (RJ45 conn., 4 LVDS pairs)
  - 16ch/ FE board, so we need 20 FE boards
  - Interface to DAQ: either SRU of FEC + LVDS interface
  - 1 SRU or 2 FECs needed

- NEXT-1-EL will be operational by Dec.2010, so a small batch of FEC v1.2 is undergoing right now
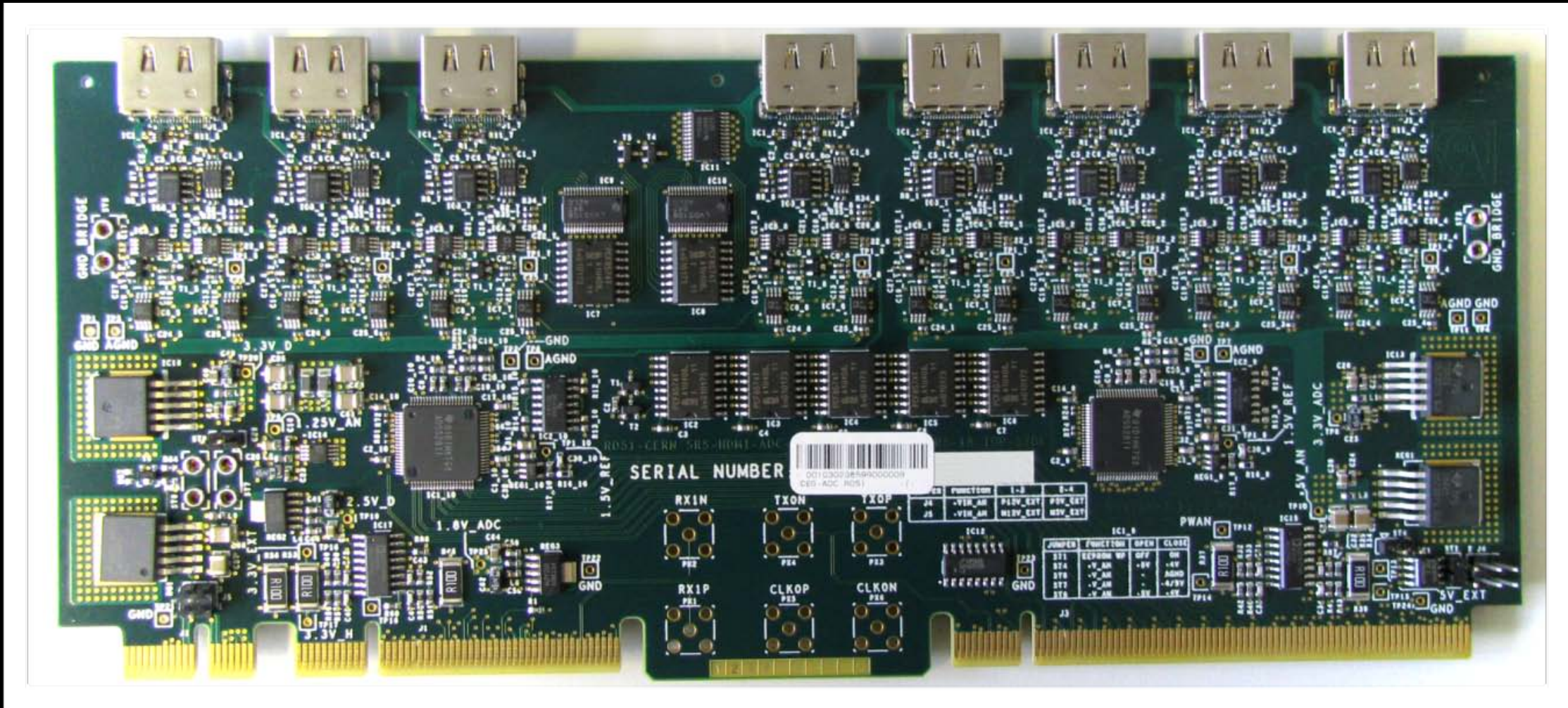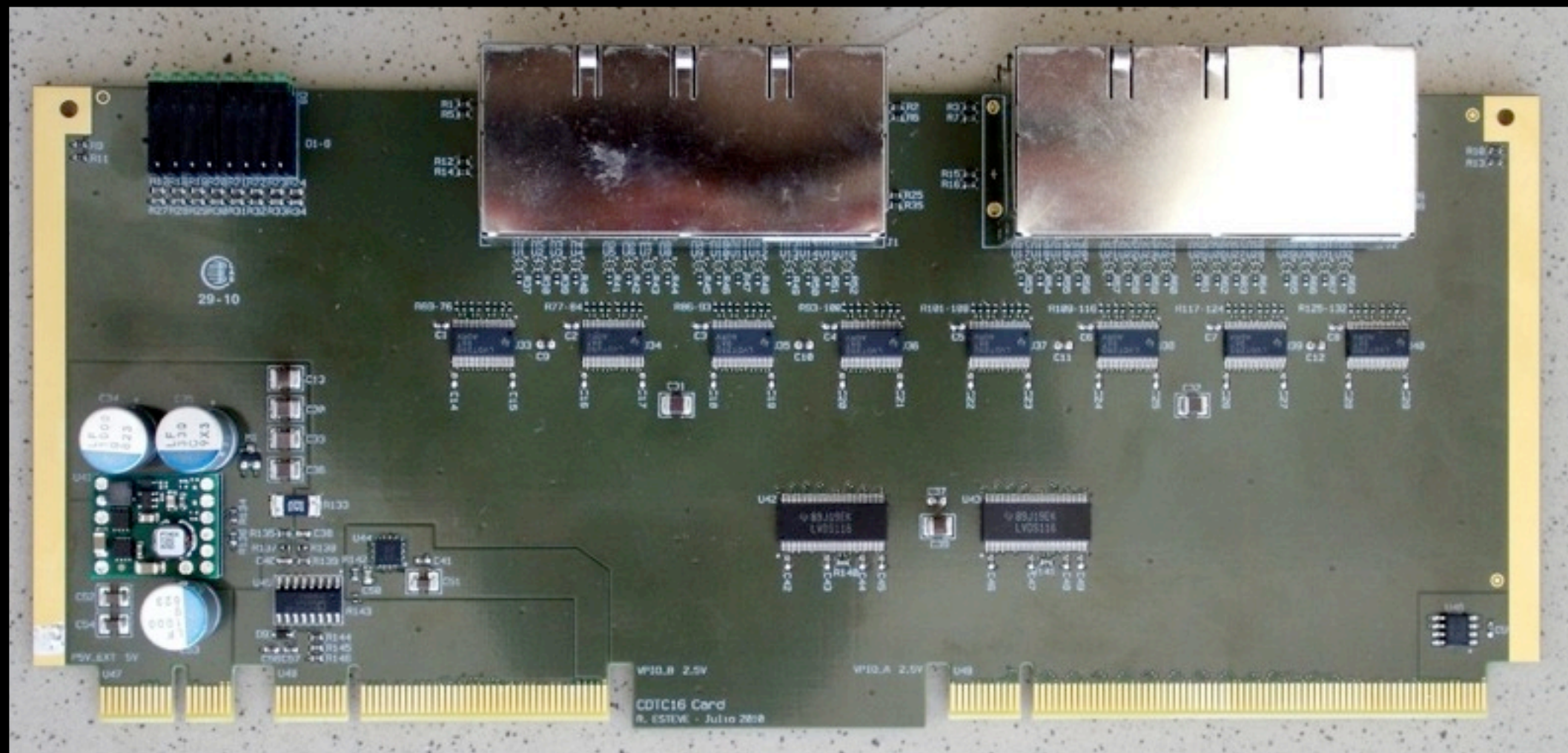
# NEXT-1-EL DAQ architecture
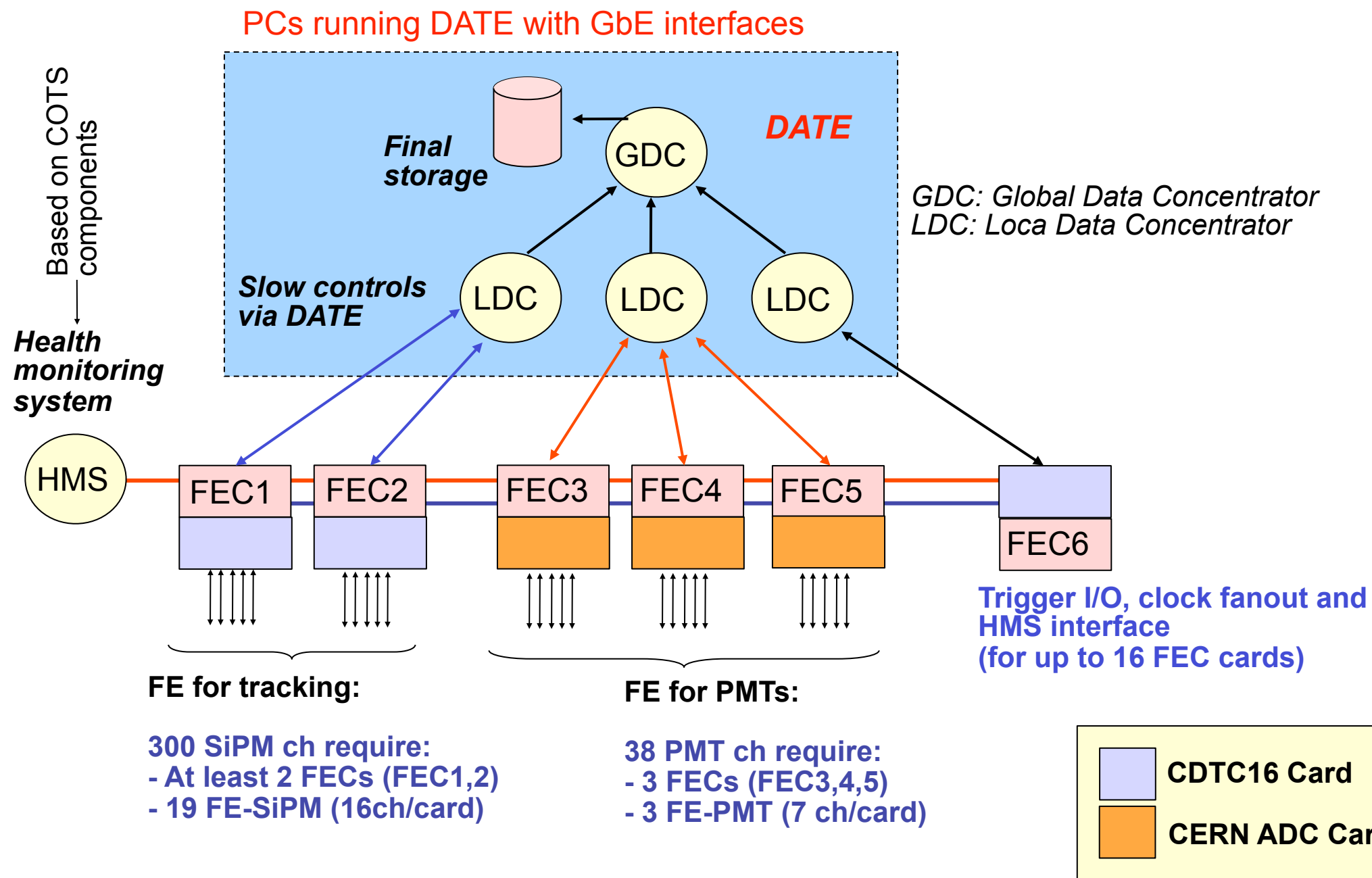
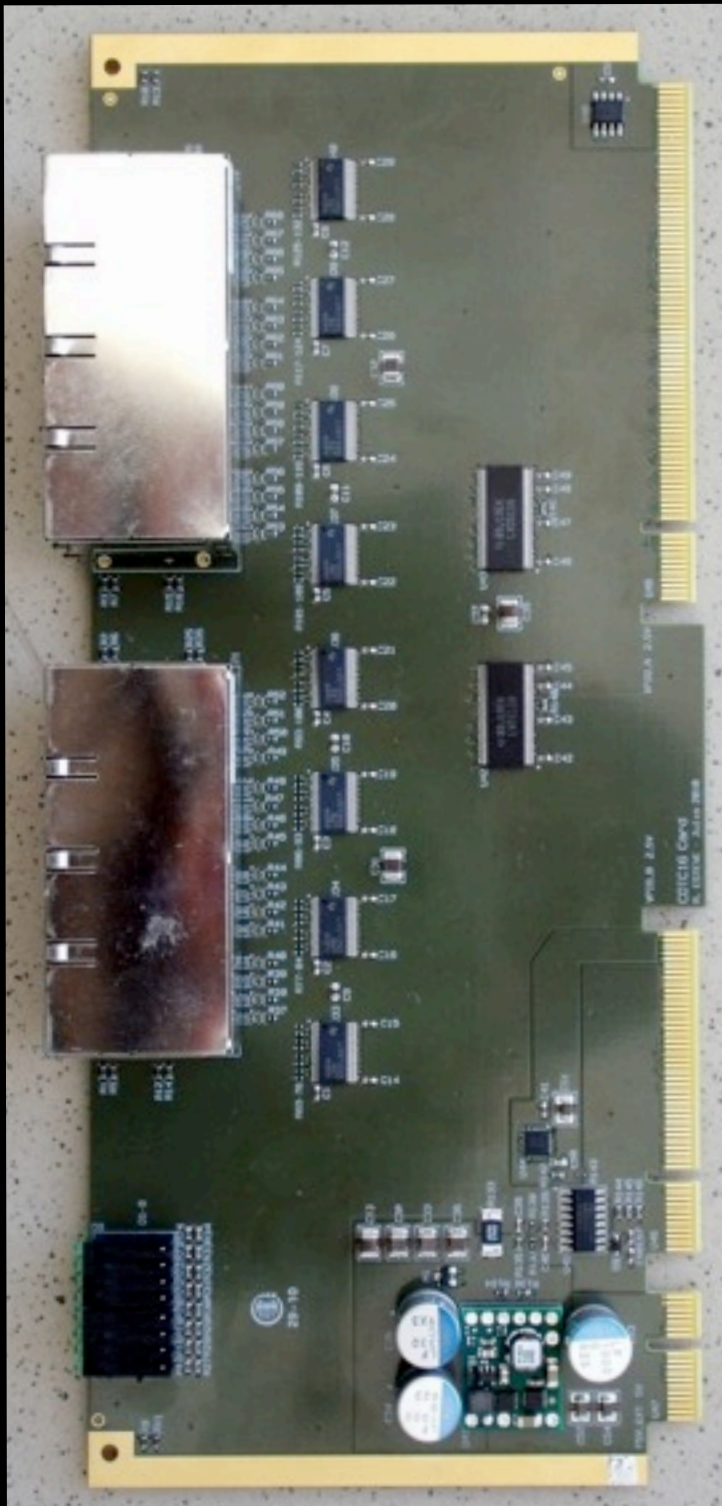# DAQ components
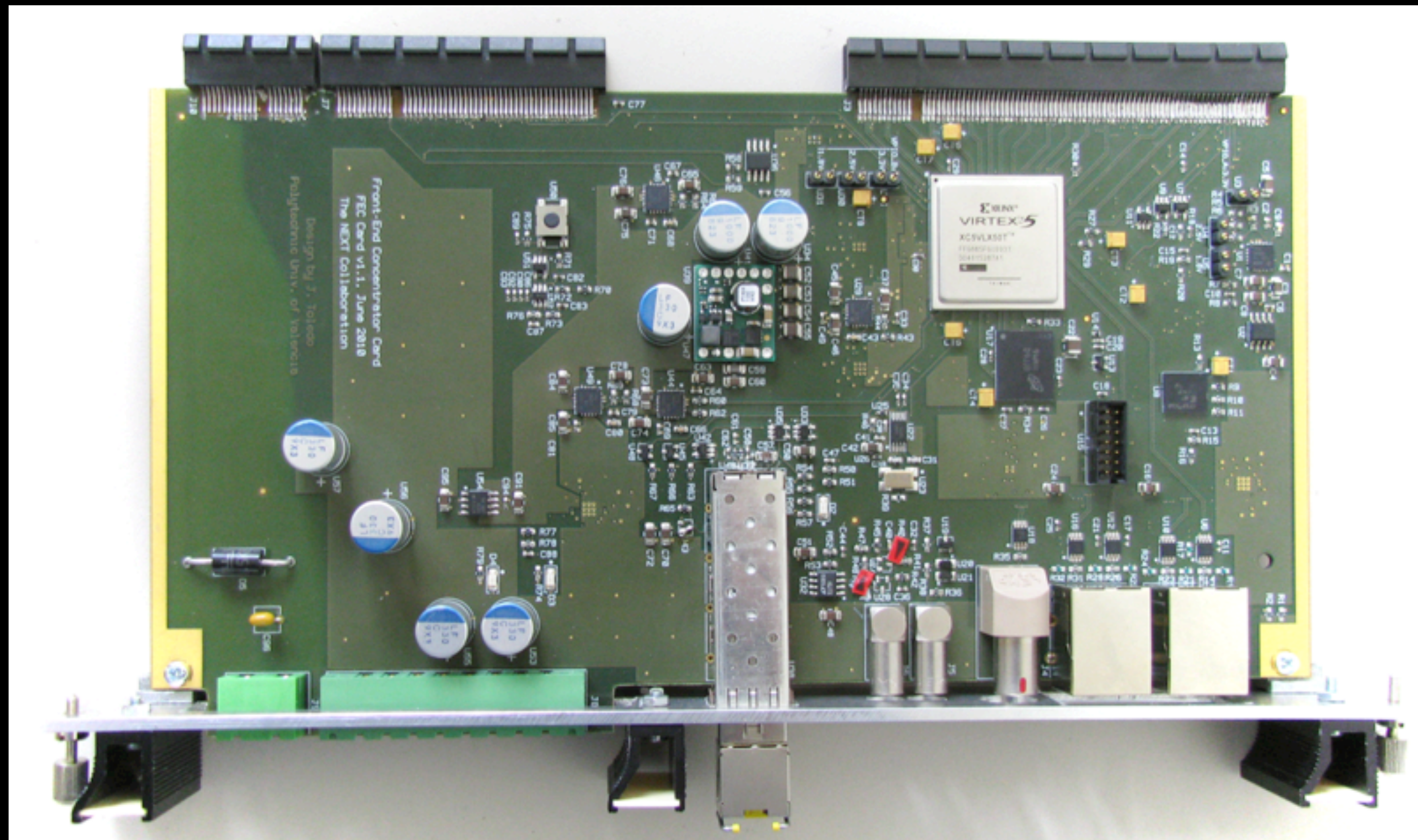


1 - The FEC card (6 units)

# DAQ components



## ADC C-Card Overview

- 2 Octal ADCs with LVDS serial

# DAQ components



III - The CDTC16: a 16x LVDS RJ45 interface C-card. Used as tracking (2 units) and trigger interface (1unit).
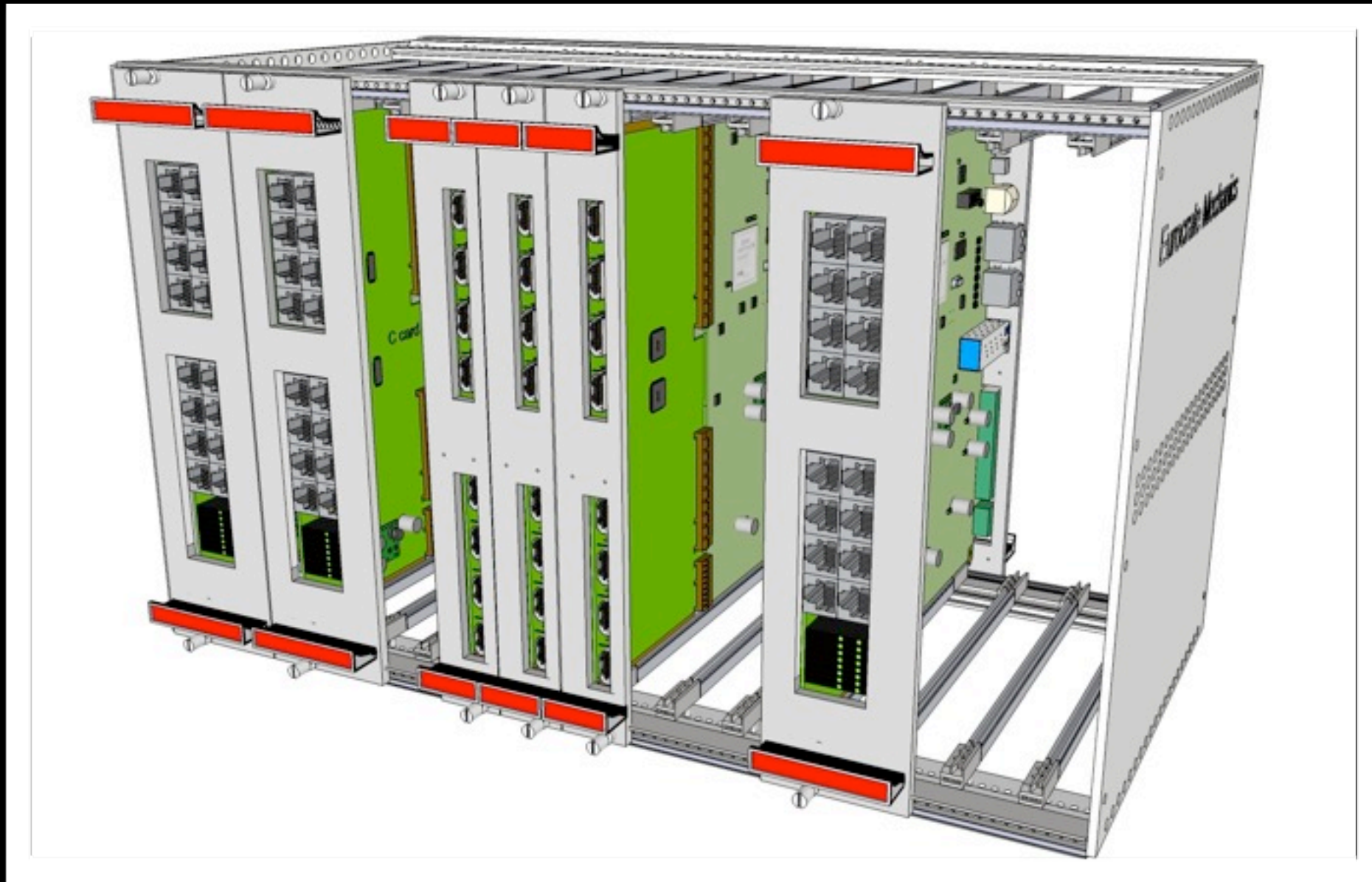
# The CDTC16 card



- NEXT design, approx. 600 €

- 16 x RJ45 conns., 4 x LVDS each

- 2 LVDS in, 2 LVDS out per connector

- Common Trig and clock+command outputs

- 200/400 Mb/s data inputs from each RJ45

- Dual use as FE-SiPM interface and Trigger board

16 channel Clock, Data, Trigger and Control

# The NEXT-1-EL DAQ box



6x FECs: 3 x ADC + 3 x LVDS interface

# Coming milestones

- Oct.2010: new FECv1.2 production starts urgently

- Dec.2010: the complete DAQ must be ready to operate

- Jan.-June 2011: DAQ test and operation, <u>a lot of FW design !!</u>

- June-Dec. 2011: Looking towards NEXT-100: cost reduction, new technologies evaluation: SRU as DAQ backbone. NEXT-100 has approx. 10k SiPM ch + 400 PMTs

# Thanks for your attention