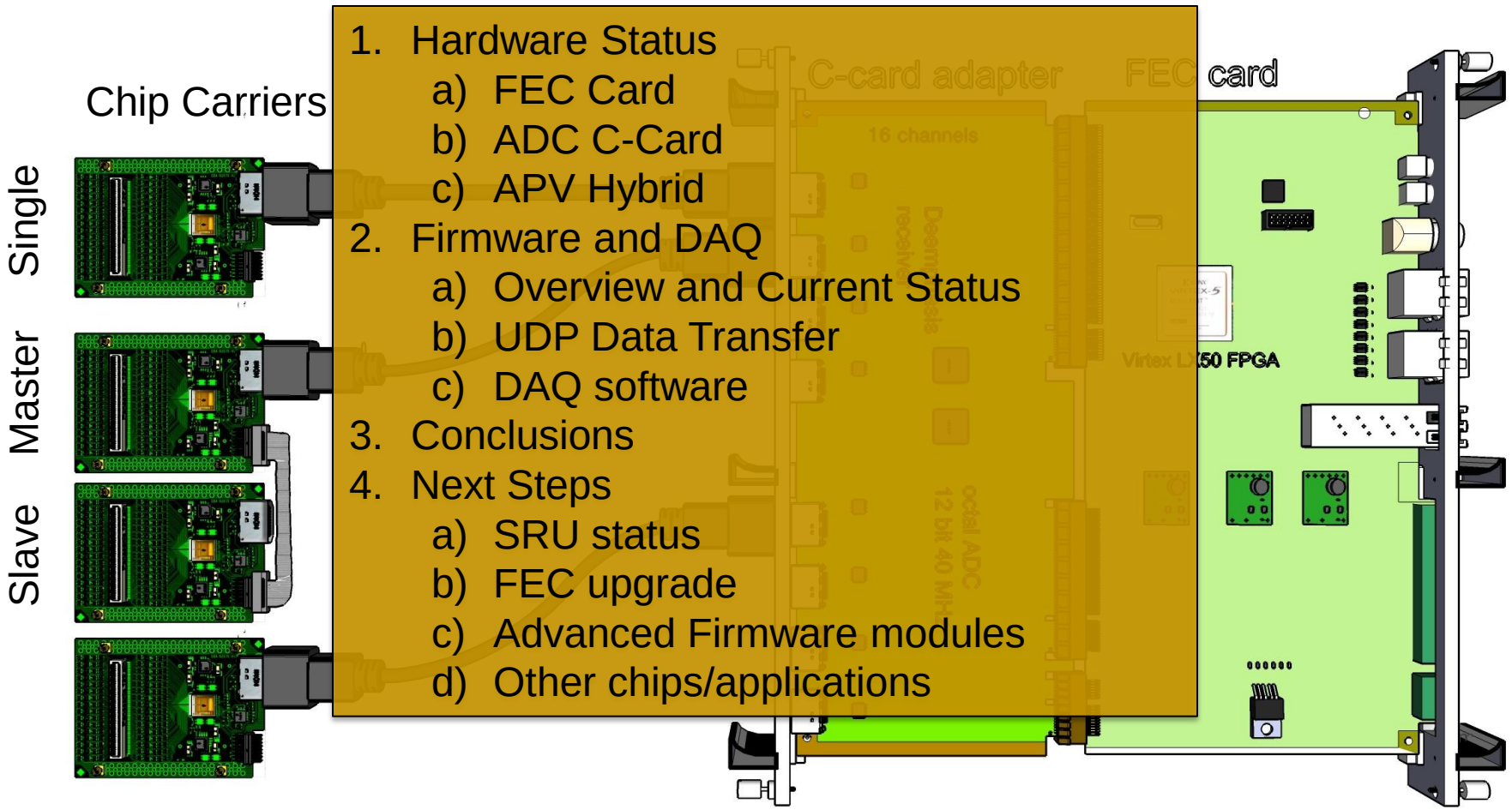
Status of the SRS

Hardware and Performance

Sorin Martoiu, CERN PH/DT

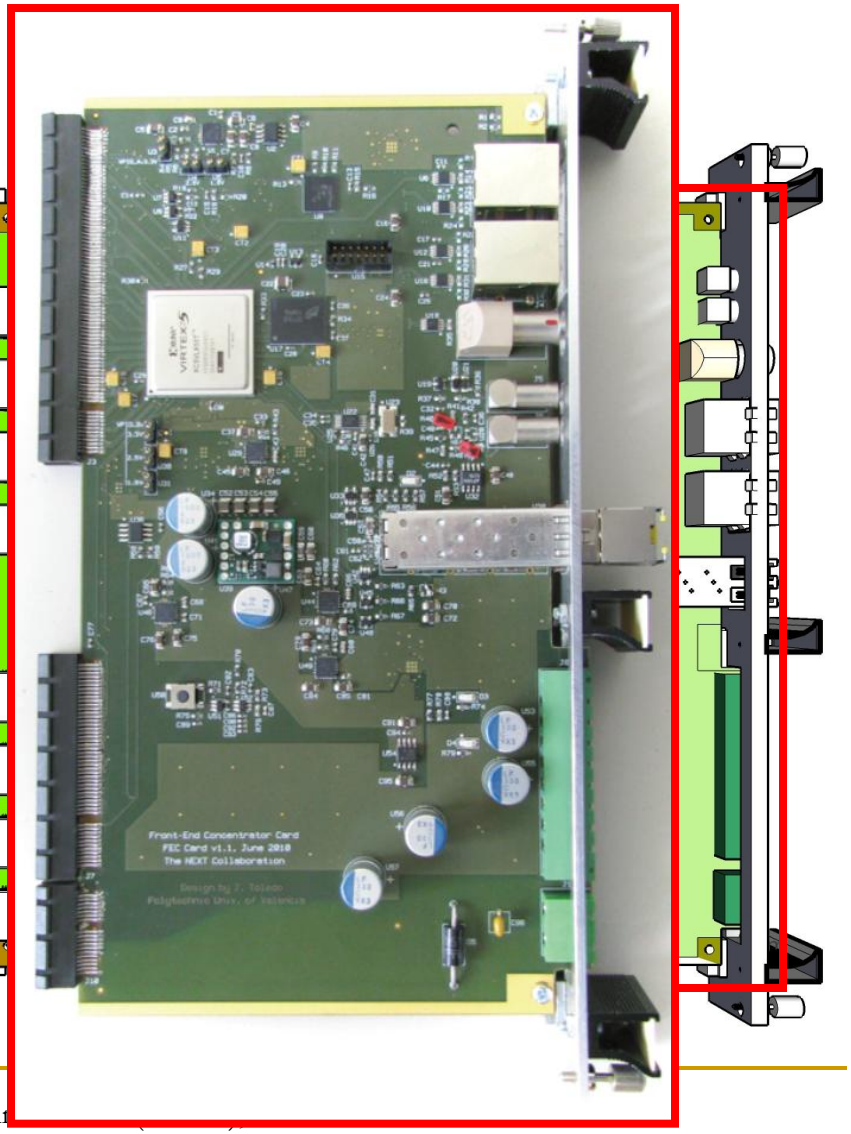
SRS APV DAQ



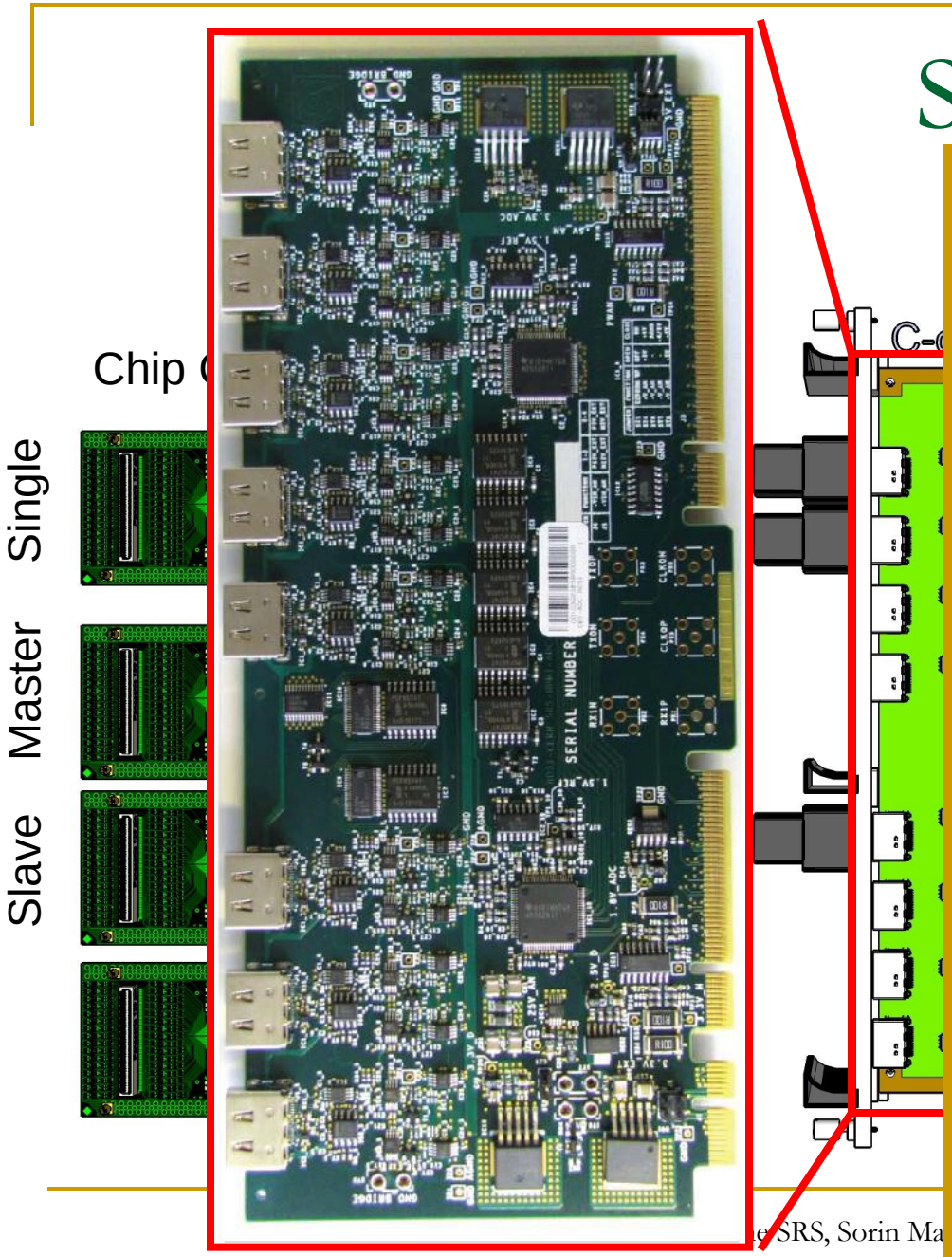
1. Hardware Status
   a) FEC Card
   b) ADC C-Card
   c) APV Hybrid
2. Firmware and DAQ
   a) Overview and Current Status
   b) UDP Data Transfer
   c) DAQ software
3. Conclusions
4. Next Steps
   a) SRU status
   b) FEC upgrade
   c) Advanced Firmware modules
   d) Other chips/applications

SRS FEC Card

- Designed and realized at the Polytechnic University of Valencia (J.Toledo – see following talk)
- Virtex LX50T FPGA
- A/B extension interface (PCIE conn)
  - 20 differential
  - 48/24 single-ended/diff
  - 2 x I2C, 1 x JTAG
  - 2 x 3.75Gbps RocketIO GTP transceivers
- 200 MHz local clock oscillator
- 1Gb DDR2 RAM, 1kb GP FLASH
- SFP/Gb Ethernet/DTC interface
- NIM/LVDS GPIO
- Power control and distribution ; HV feed-through



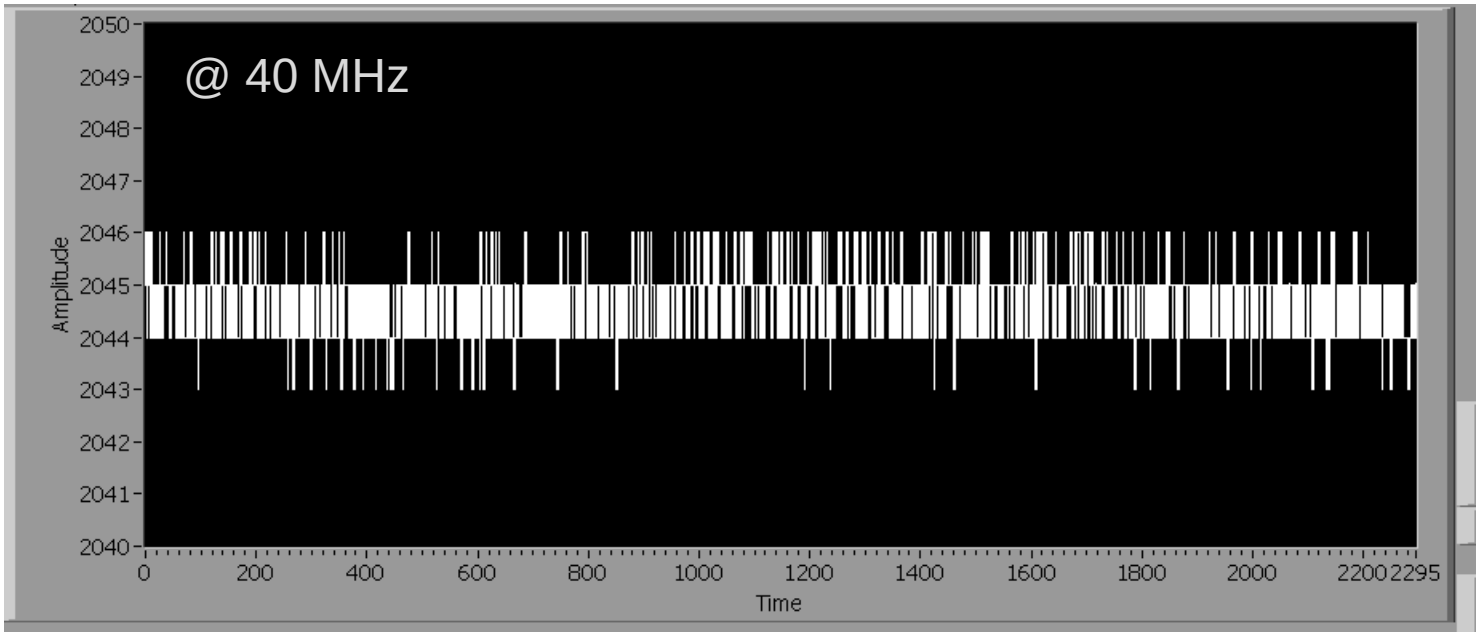
SRS ADC C-Card



- 2 x 12-Bit Octal-Channel ADC
  - up to 50(65) MSPS
  - Programmable Gain: 0dB to 12dB
  - Low-Frequency Noise Suppression
- 8 x HDMI channels
  - 2 analog channels (differential) with variable equalization
  - 1 x I2C, 1 x CMOS (rst)
  - 2 x LVDS OUT (clk, trg), 1 x LVDS in
  - Tailored for APV25 or Beatle FE chips
  - compatible with other analog FE (see next talks)
- Power and equalization control
- Slow control mux/switch
- Clock distribution
- Temperature/Voltage Monitoring

ADC C-Card

Performance



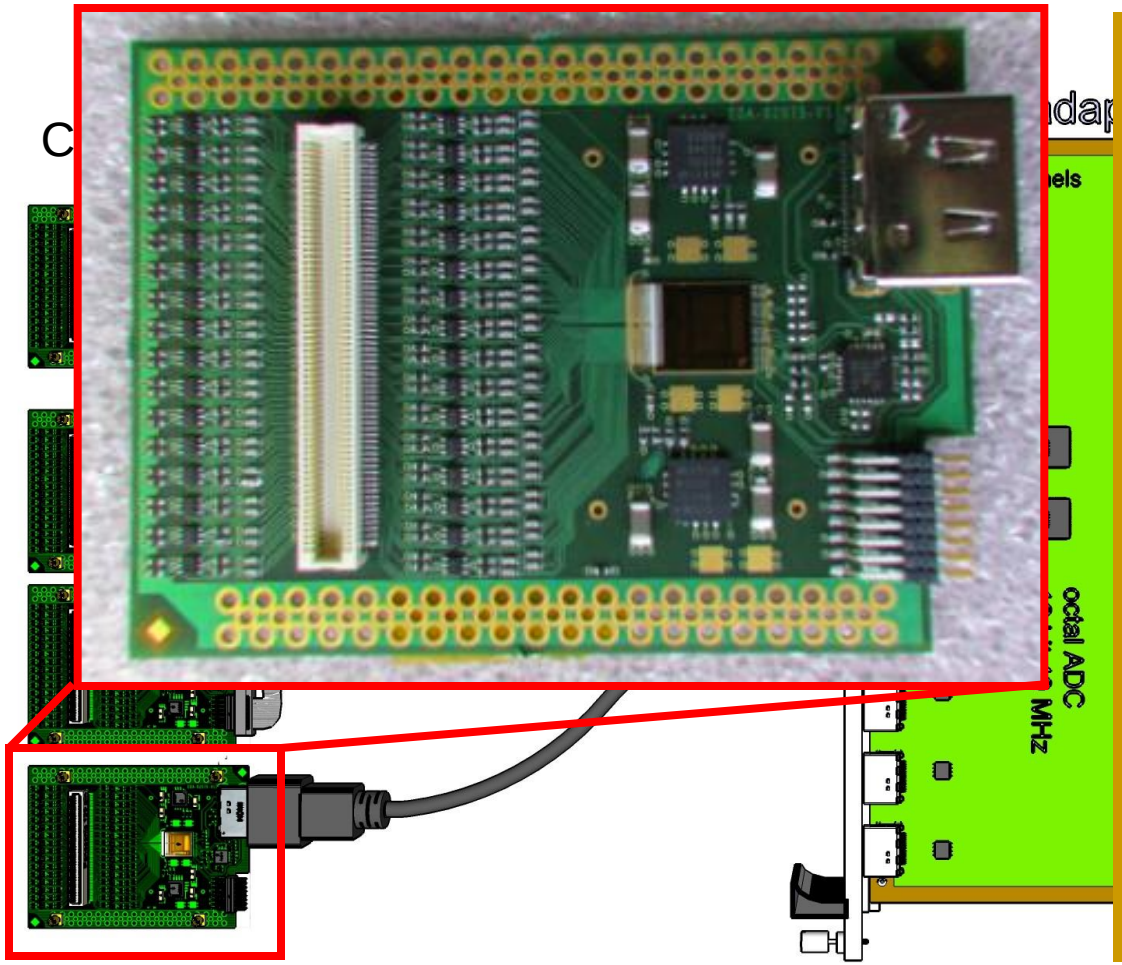
noise ≅ 0.63 ADC bins (rms)
≅ 300 uV (rms)

ADC C-Card

Power Consumption

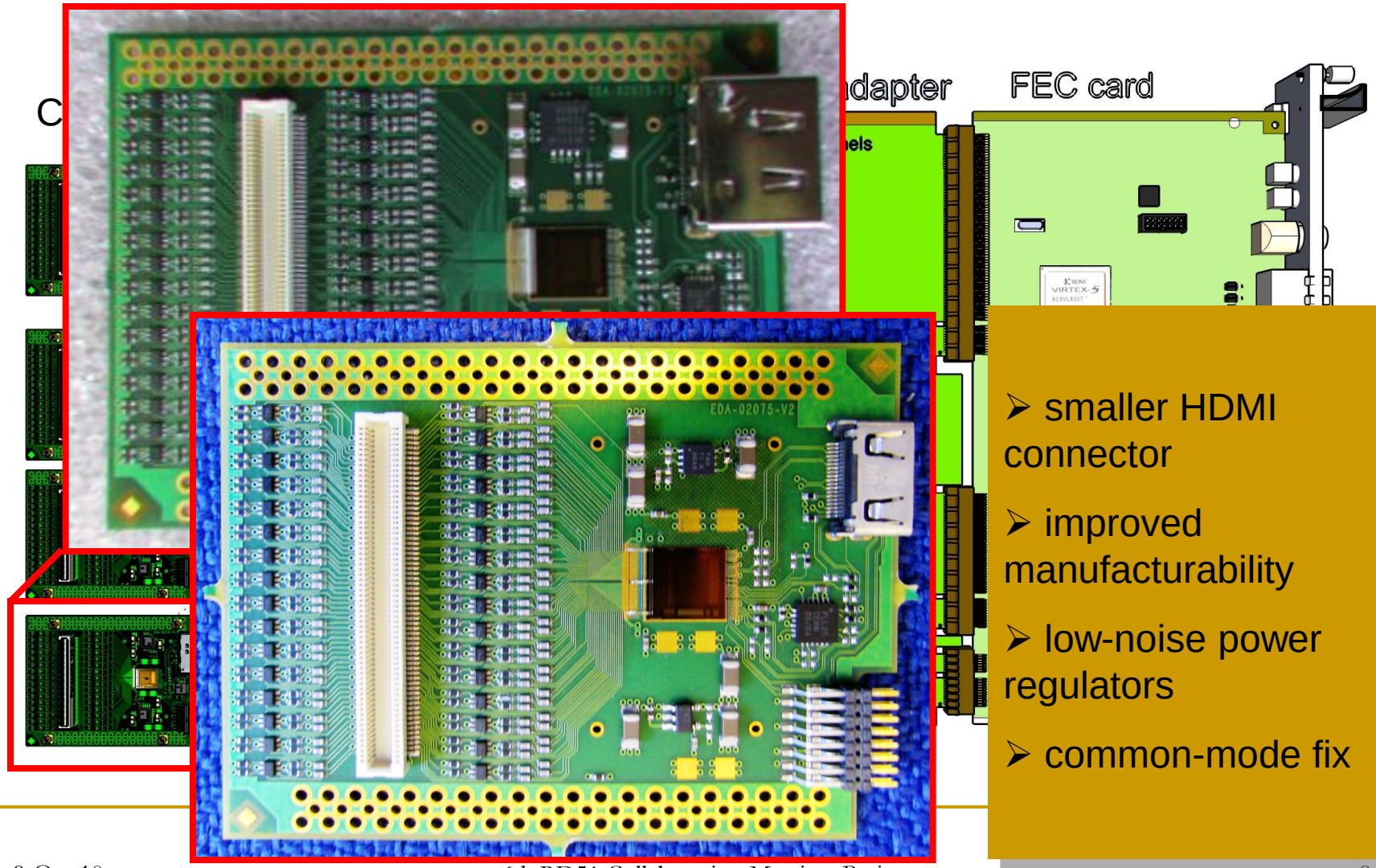
	Supply (V)	Regulated	I(A)	P(W)	P/ADCch (W)	P/APVch (mW)
digital 1	3.3	2.5; 1.8	0.160	0.53	0.033	0.26
digital 2	5	3.3	0.400	2.00	0.125	0.98
analog+	5	4	0.380	1.90	0.119	0.93
analog-	-5	-4	0.380	1.90	0.119	0.93
adc analog	5	3.3	0.600	3.00	0.188	1.46
TOTAL				**9.33**	**0.583**	**4.55**
APV hybrid	3.3	2.5; 1.25	0.180	0.59		4.64
TOTAL (with 16 APVs)				**18.8**		**9.20**

SRS APV Hybrid



- APV25 front-end
  - 128 channels
  - analog sampling memory (192s/ch)
  - current-mode differential serial analog output
- Discharge protection
- Power regulation
- Clock PLL/trigger decode

SRS APV Hybrid v2

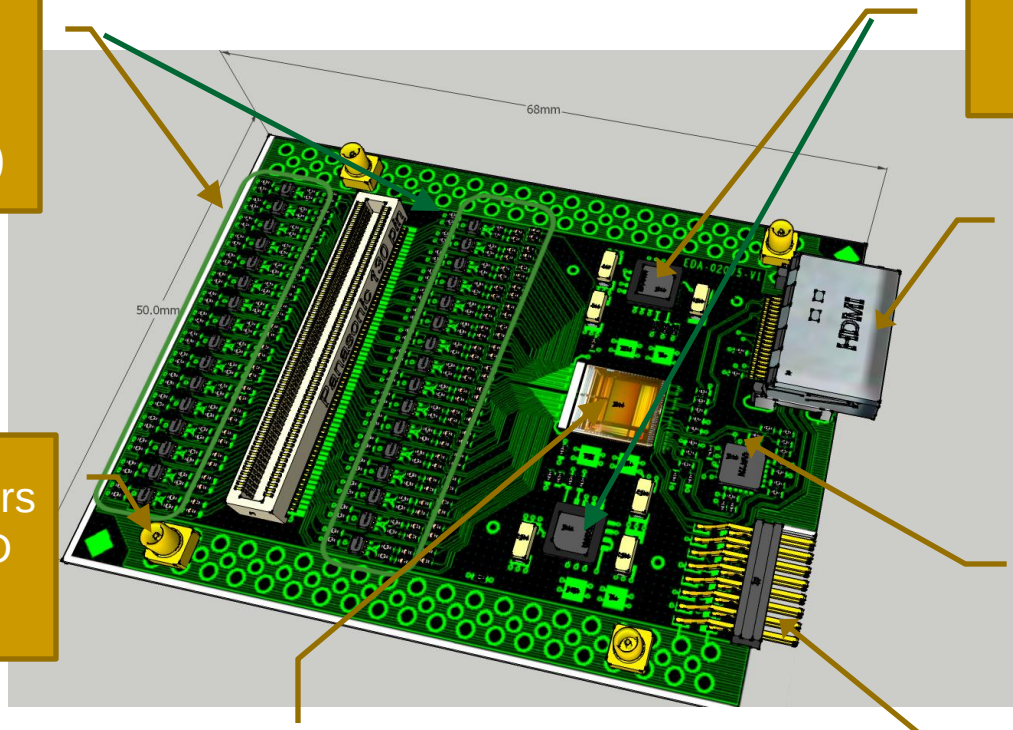


- smaller HDMI connector
- improved manufacturability
- low-noise power regulators
- common-mode fix

APV Hybrid Overview

Discharge protection (NUP4114)

Power regulators (MAX8556)



HDMI connector
- power
- clock/trigger
- analog signals
- I2C

Coax Connectors
- <2mohm GND
- mechanical

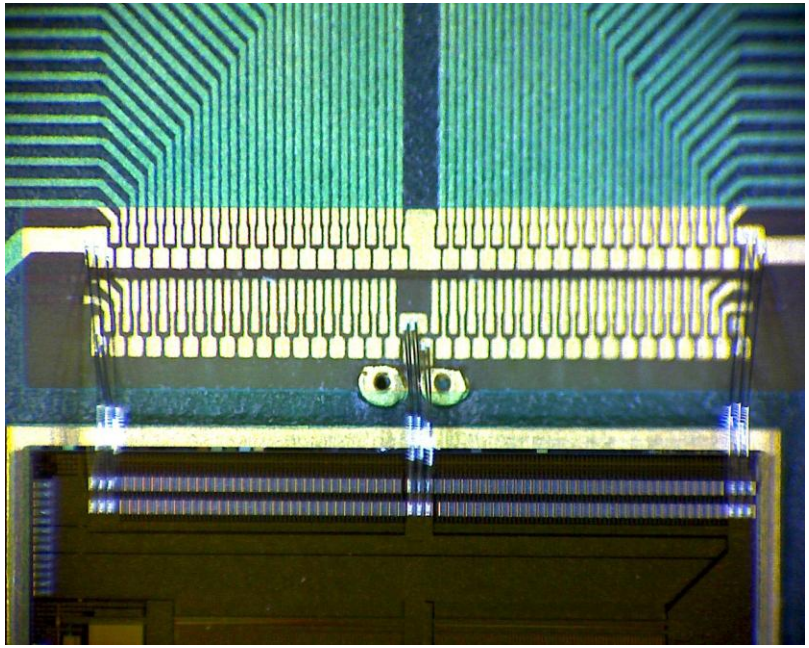
PLL25 rad-hard chip
clock/trigger

APV25 chip
- 128 channels
- 192-deep analog sampling memory

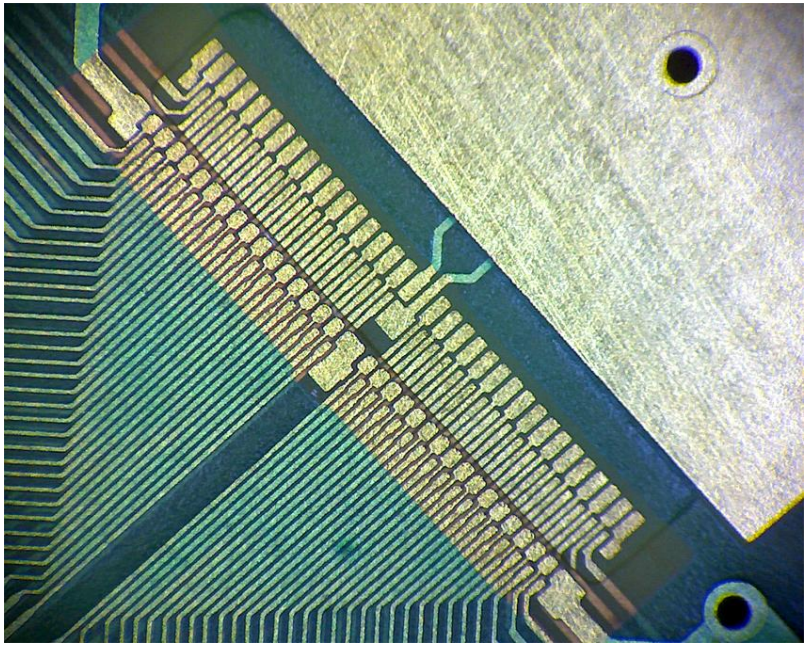
Extension connector for a second APV25 Hybrid

SRS APV Hybrid

Manufacturability



APV Hybrid v1

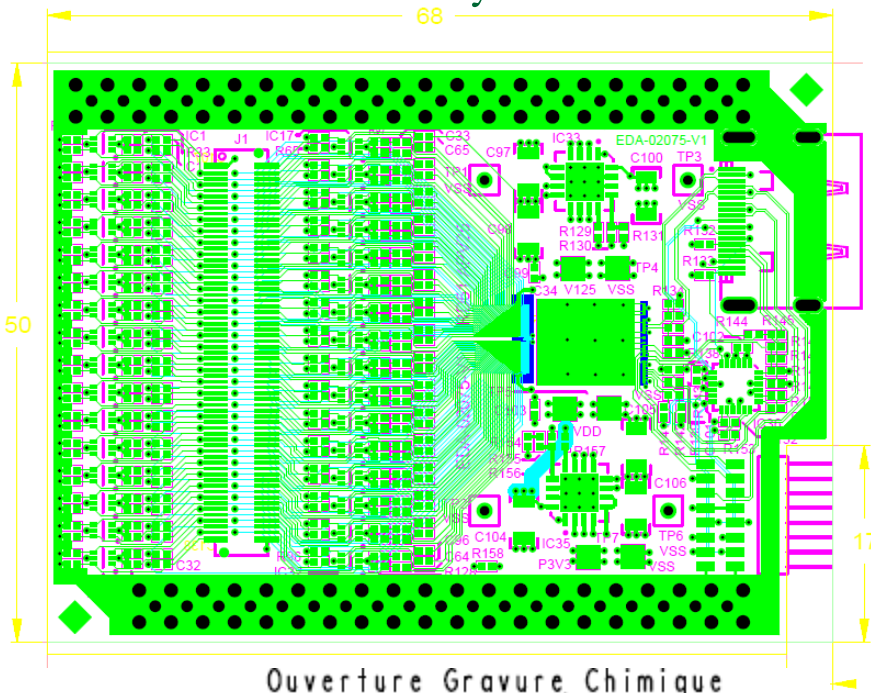


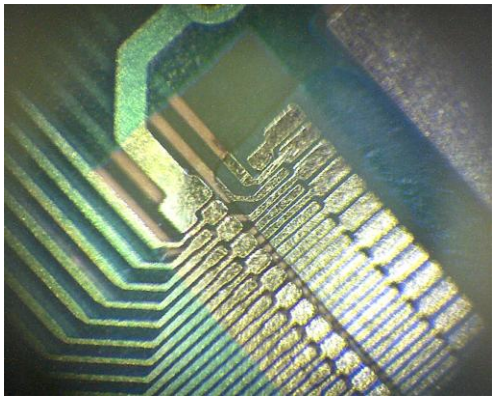
APV Hybrid v2

- The two vias in the bonding region eliminated to improve manufacturability

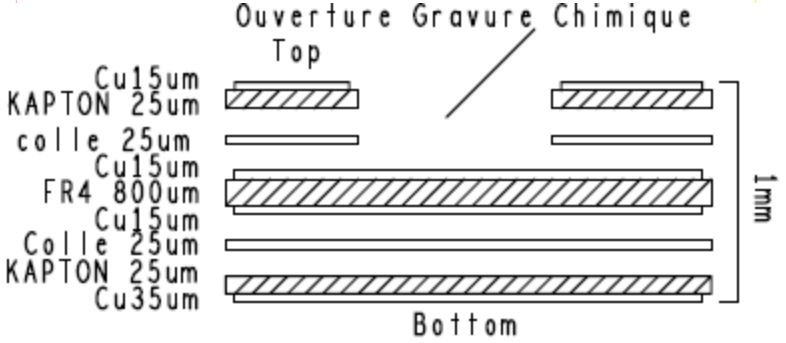
SRS APV Hybrid

Manufacturability





- 50mm x 68mm form factor
- 4 layers PCB/capton
- 1 mm thickness



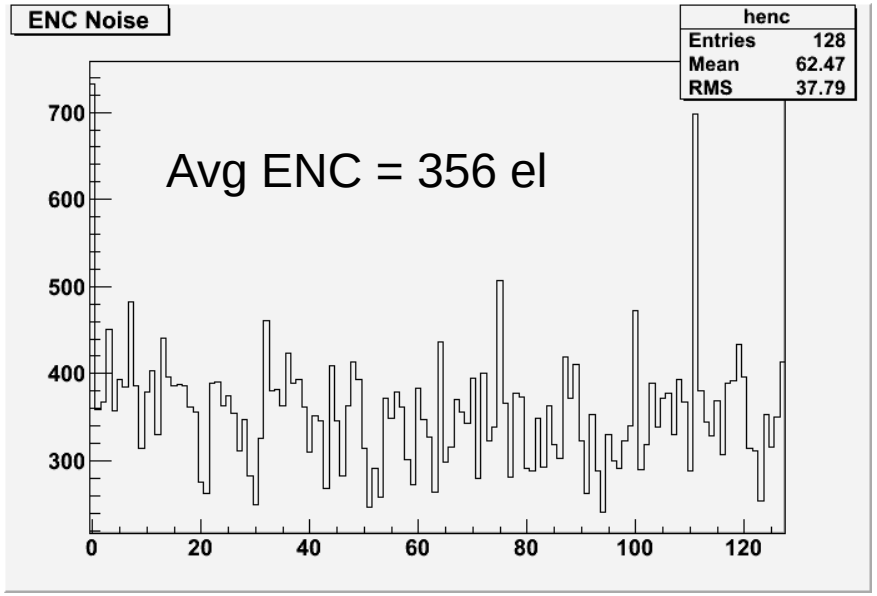
Manufacturability issues:

- chemical etch
- clearance < 50 um in the bond-pad region
- still waiting for production quotes

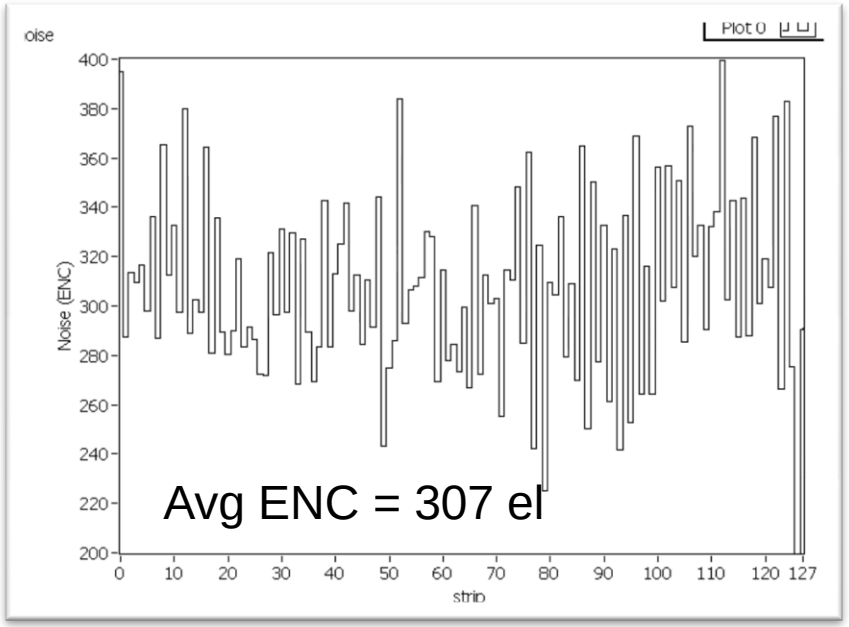
SRS APV Hybrid

Performance

APV Hybrid V1 – noise



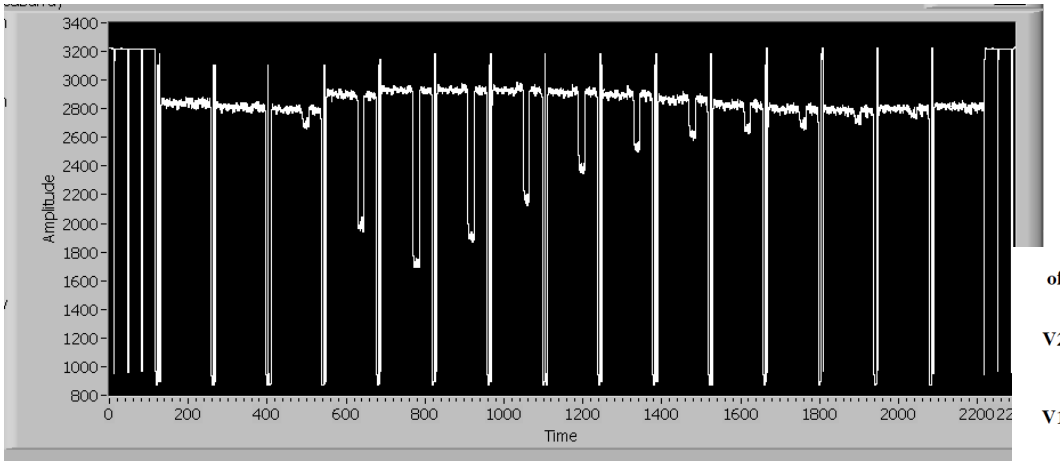
APV Hybrid V2 – noise



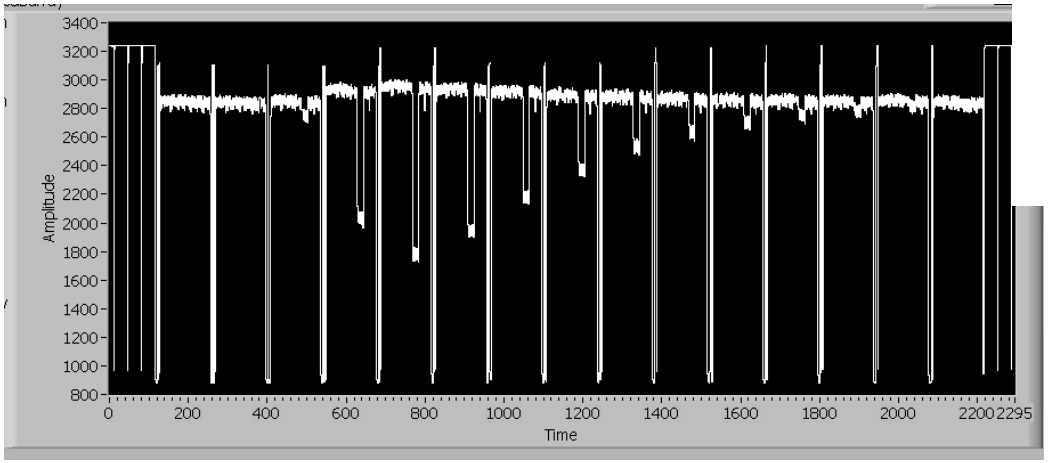
- Bench performance (no detector)
- More on performance with GEM detectors in Kondo's talk

SRS APV Hybrid

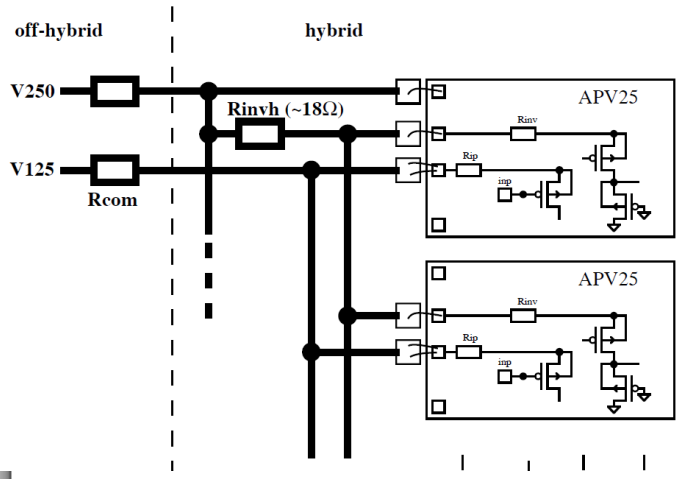
Common-Mode Problem



APV Hybrid V1 – raw analog stream

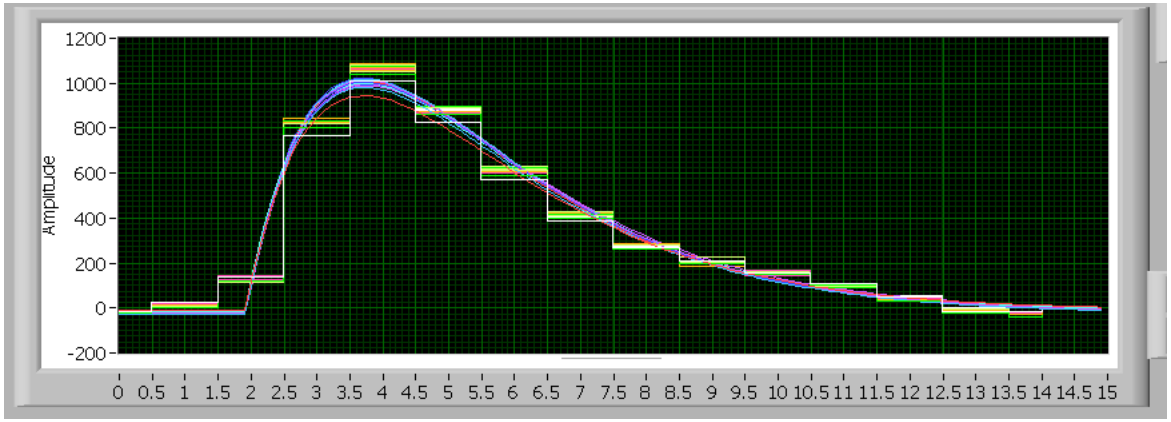


APV Hybrid V2 – raw analog stream

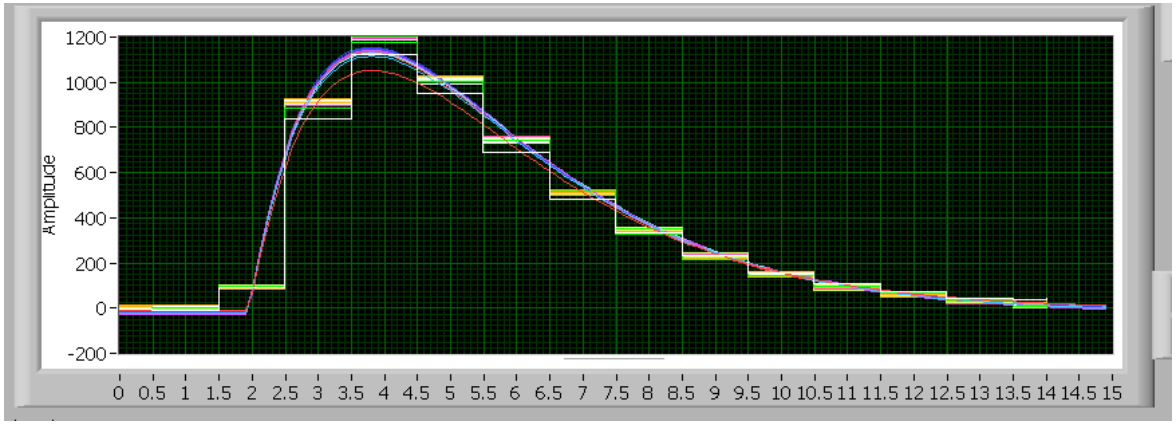


SRS APV Hybrid

Common Mode Correction



APV Hybrid V1 – Signal Fit



APV Hybrid V1 – Signal Fit

Offline common-mode correction

Firmware and DAQ

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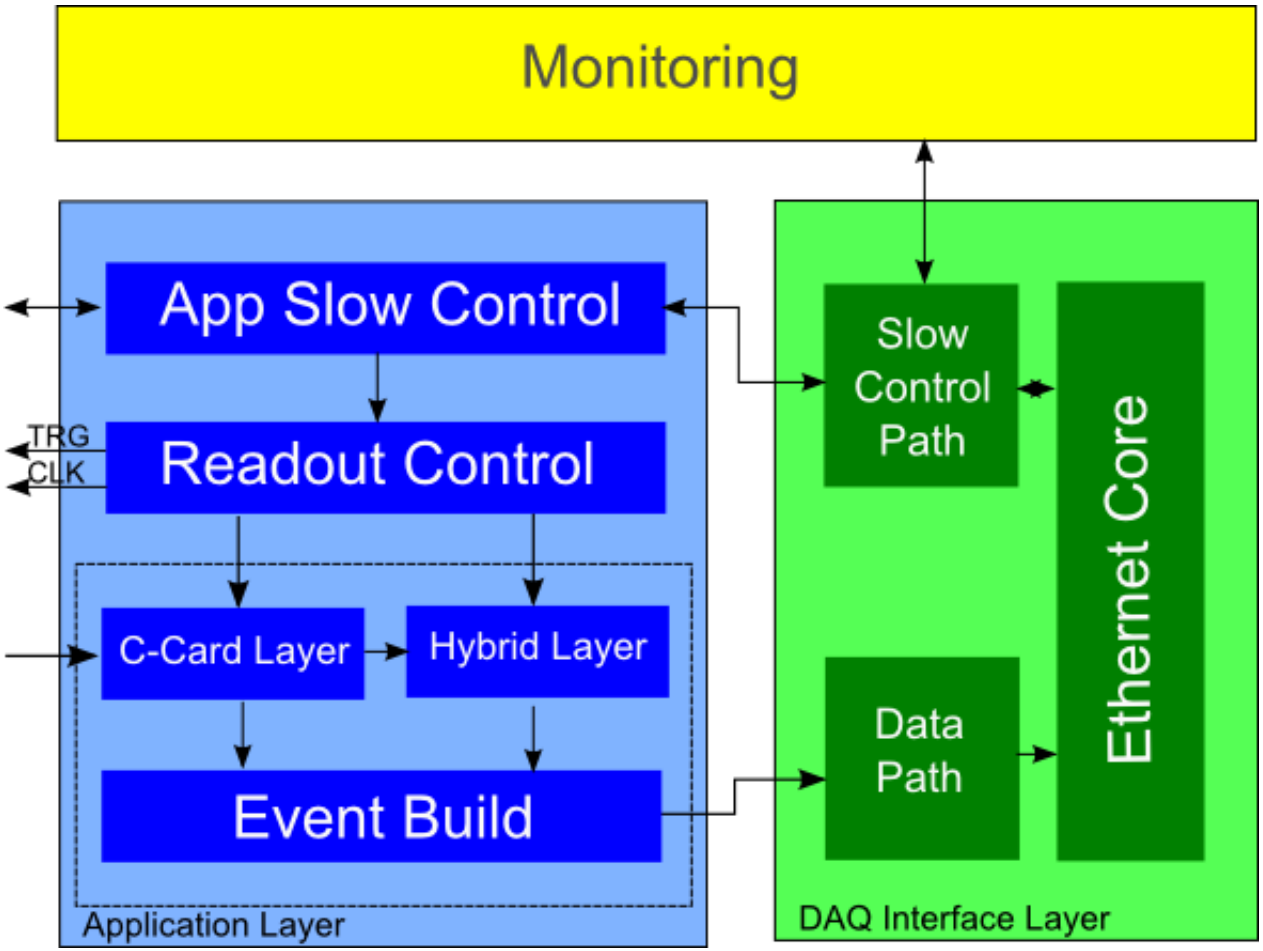
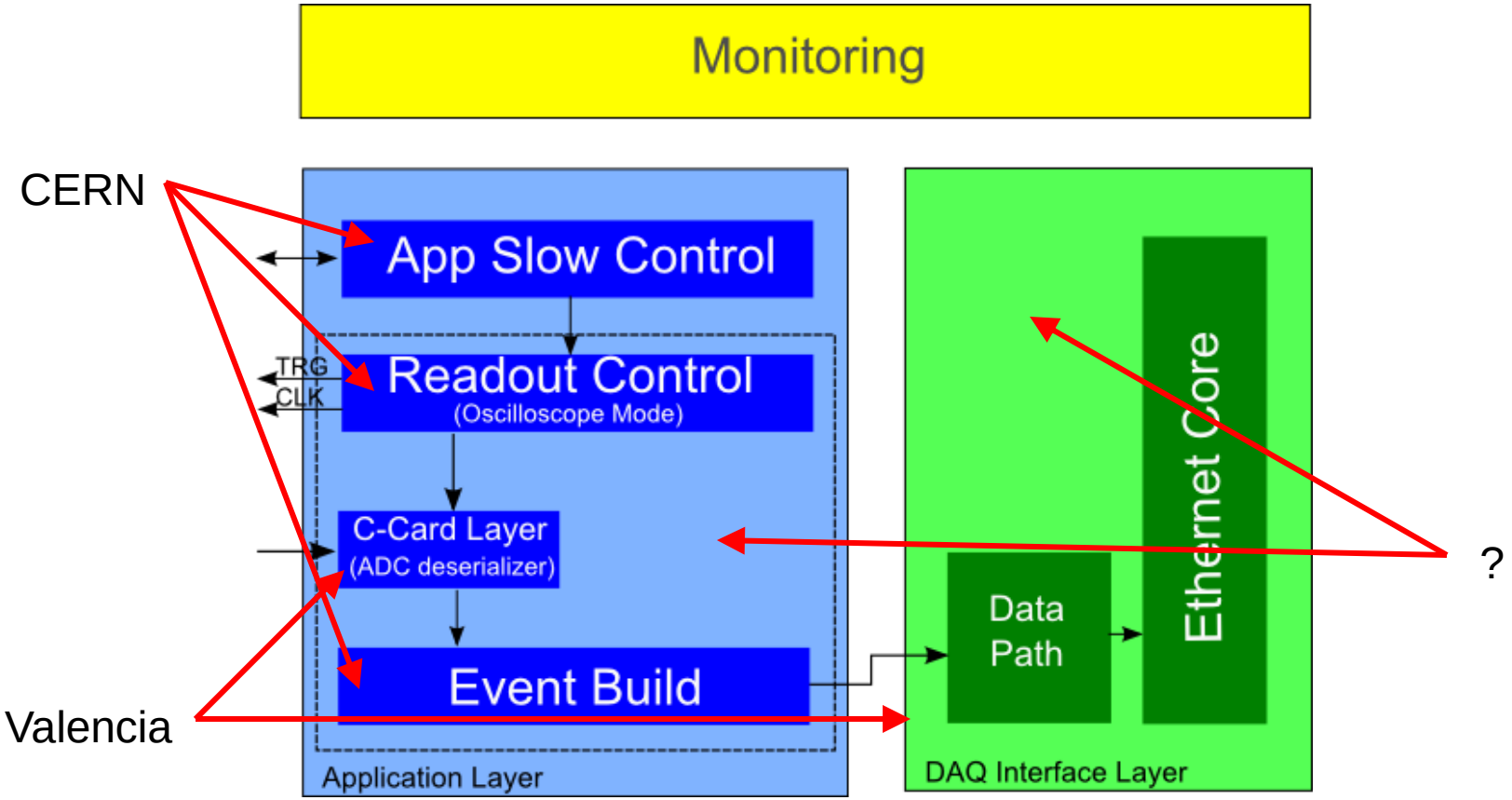
Firmware

Overview

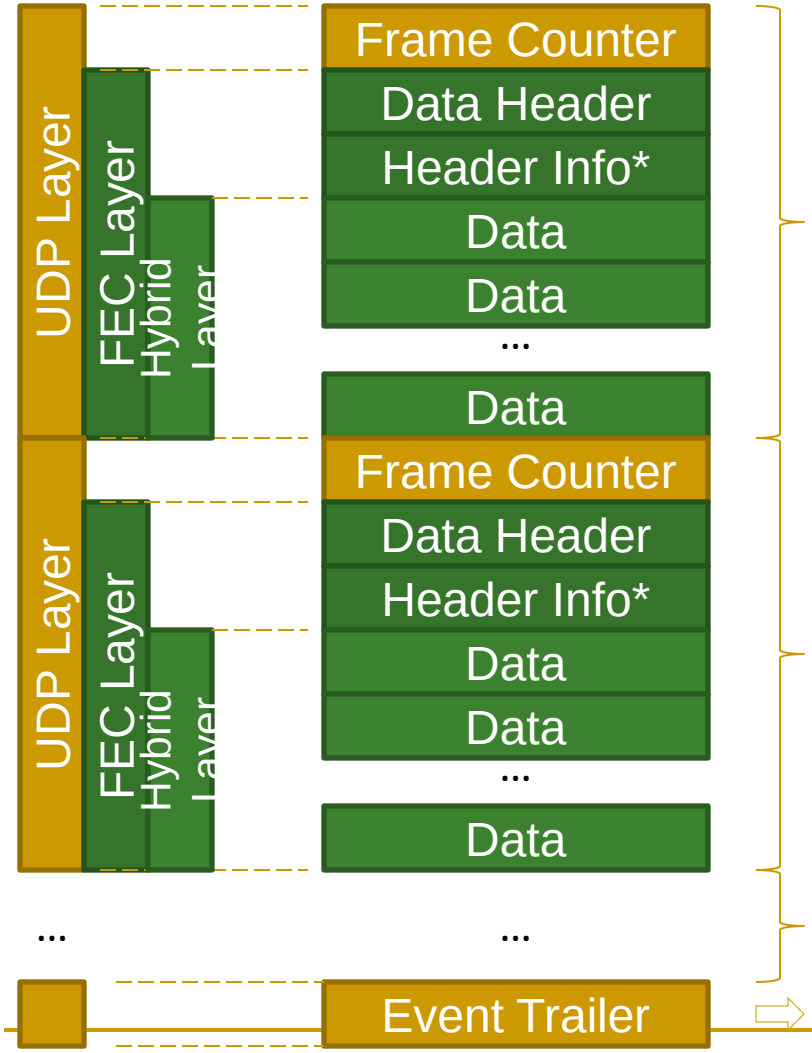


Firmware

Status

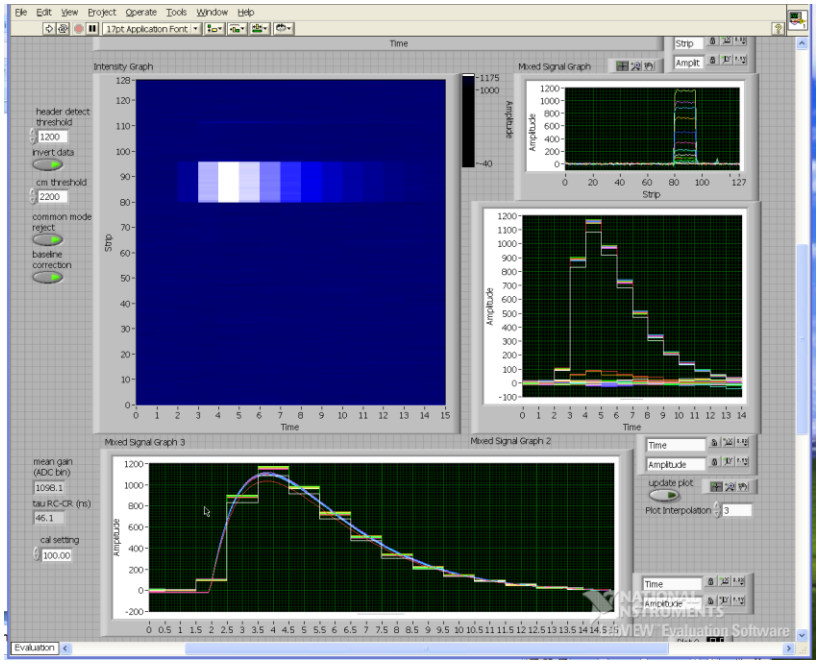


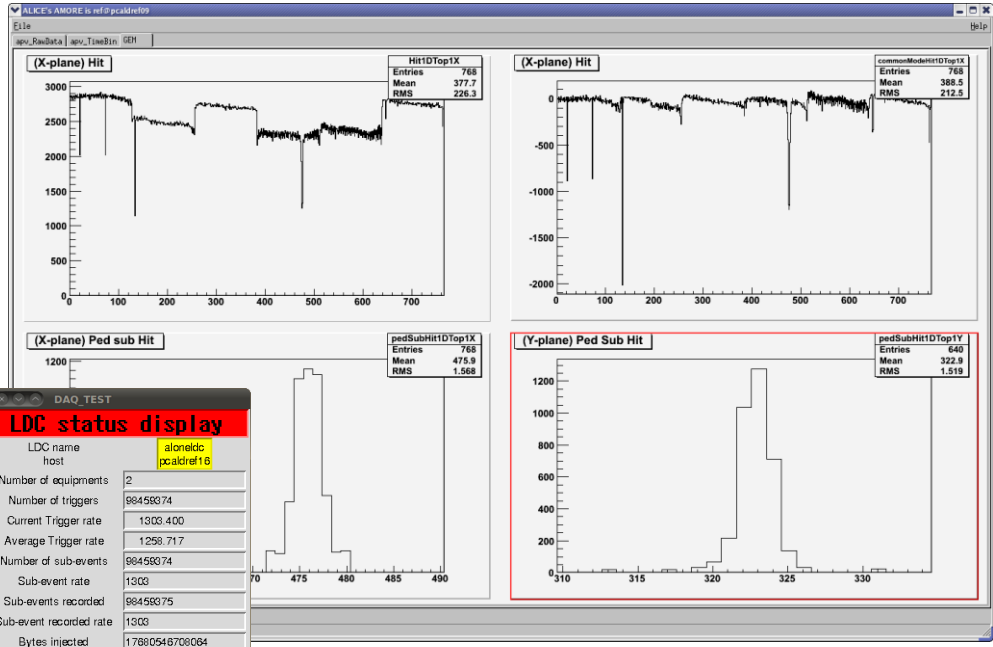
SRS UDP data protocol



- Event is broken into a number of frames (MTU = 9kB)
- Frame Counter used for fragment re-ordering and fragment loss detection
- Data Header and Header Info identifies the data type, address, word packing, etc

DAQ Software





Labview DAQ:

- laboratory based
- monitoring and debugging
- no proper DAQ (help welcomed)

DATE/AMORE:

- full DAQ/monitoring system
- separate slow control

Conclusions

- First SRS system with 11 APV hybrids up and running taking cosmic data with GEM detector (see Kondo's talk).
- First SRS system running with PMTs and SiPMTs for NEXT experiment (see next talk)
- 1Gb Ethernet-based readout with DATE.
- Good performance and system stability.
- SRU based scalar system will follow shortly
- Other applications

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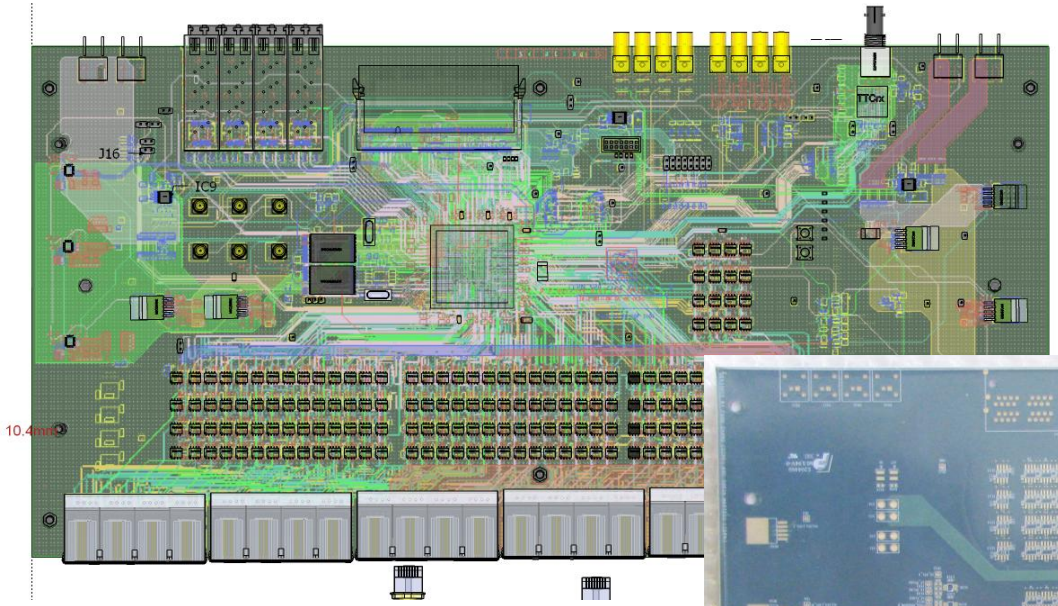
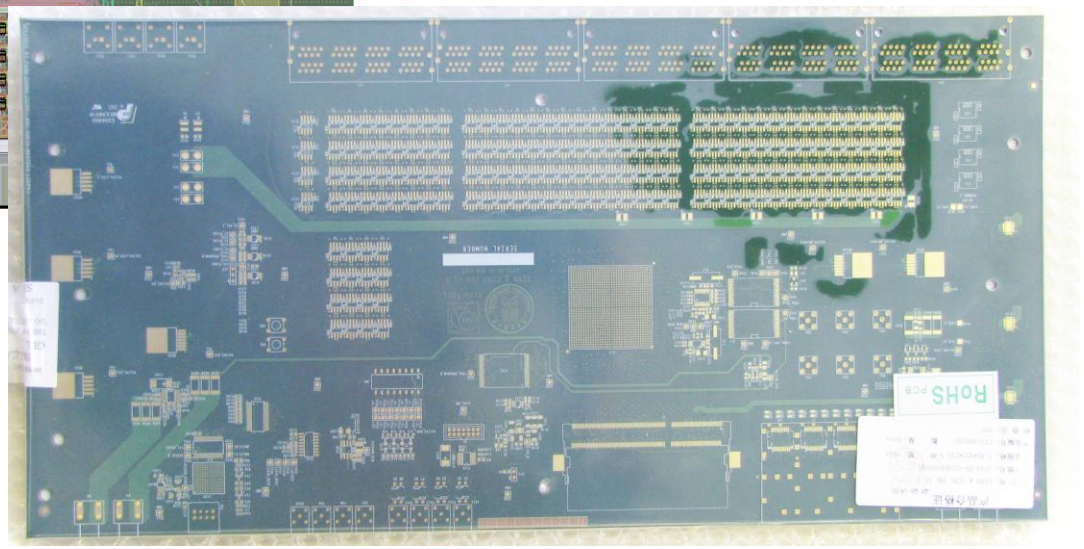
SRU Status





- ✓ 12 PCB's manufactured
- ✓ Assembly in preparation
- ✓ Tests in ~ 6 weeks time

FEC Upgrade

- Virtex 6 FPGA (*built-in SEU protection, more resources, …)*
- A/B extension interface (PCIE conn)
  - 20 differential
  - **80/40** single-ended/diff
  - 2 x I2C, 1 x JTAG
  - **4 x 5Gbps** RocketIO GTP transceivers
- 200 MHz local clock oscillator
- **DDR3 RAM (SO-DIMM?)**, 1kb GP FLASH
- **SFP+/5Gb Ethernet**/DTC interface
- NIM/LVDS GPIO
- Power control and distribution ; HV feed-through

Advanced Firmware Modules

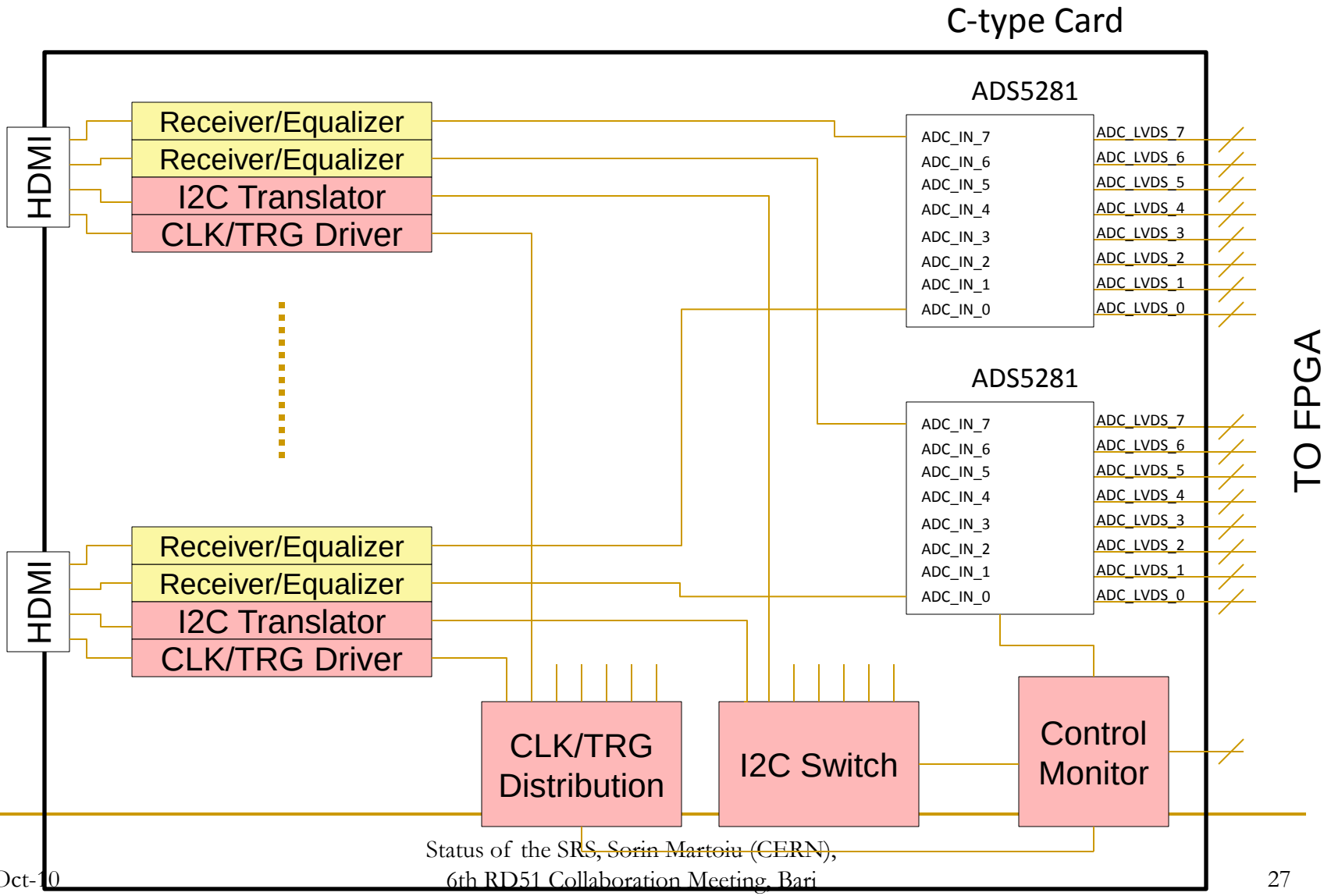
- APV synchronization and sparse (pipelined) readout
- Zero-suppression
  - Common-mode subtraction
  - Baseline correction
- Fully-automatic initialization
  - Hybrid detection and synchronization
  - Cable-length (equalization) adjust
  - Dynamic range and polarity adjust
- *Partial reconfiguration – loading application code automatically when extension card (A/B/C-Card) is inserted*

Other Chips/Application

- Timepix/Medipix (Bonn)
- MaMMA BNL chip (CERN, see Venetios's talk)
- GEMROC
- *VFAT – on-going discussion on availability (respin/redesign)*

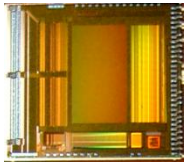
Backup Slides

Simplified Block Diagram



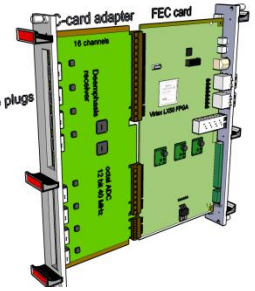
Input Equalization

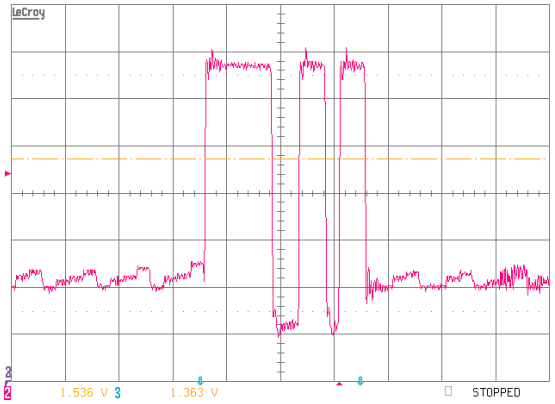
APV25



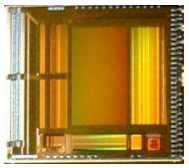
Short Cable

8 x HDMI cable plugs



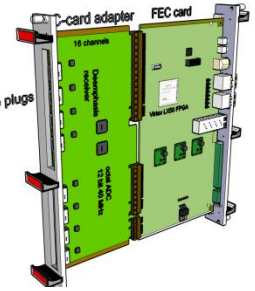


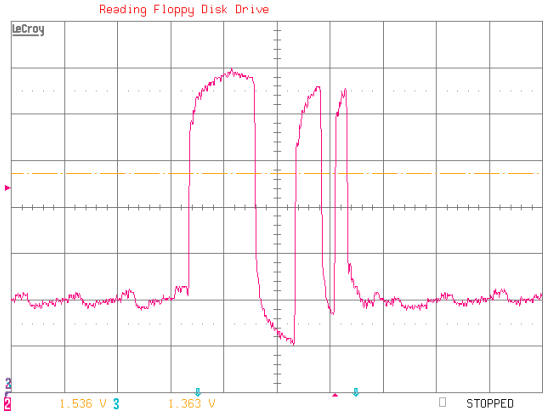
APV25



Long Cable

8 x HDMI cable plugs





- 4 equalization steps to accommodate cables up to 30 meters