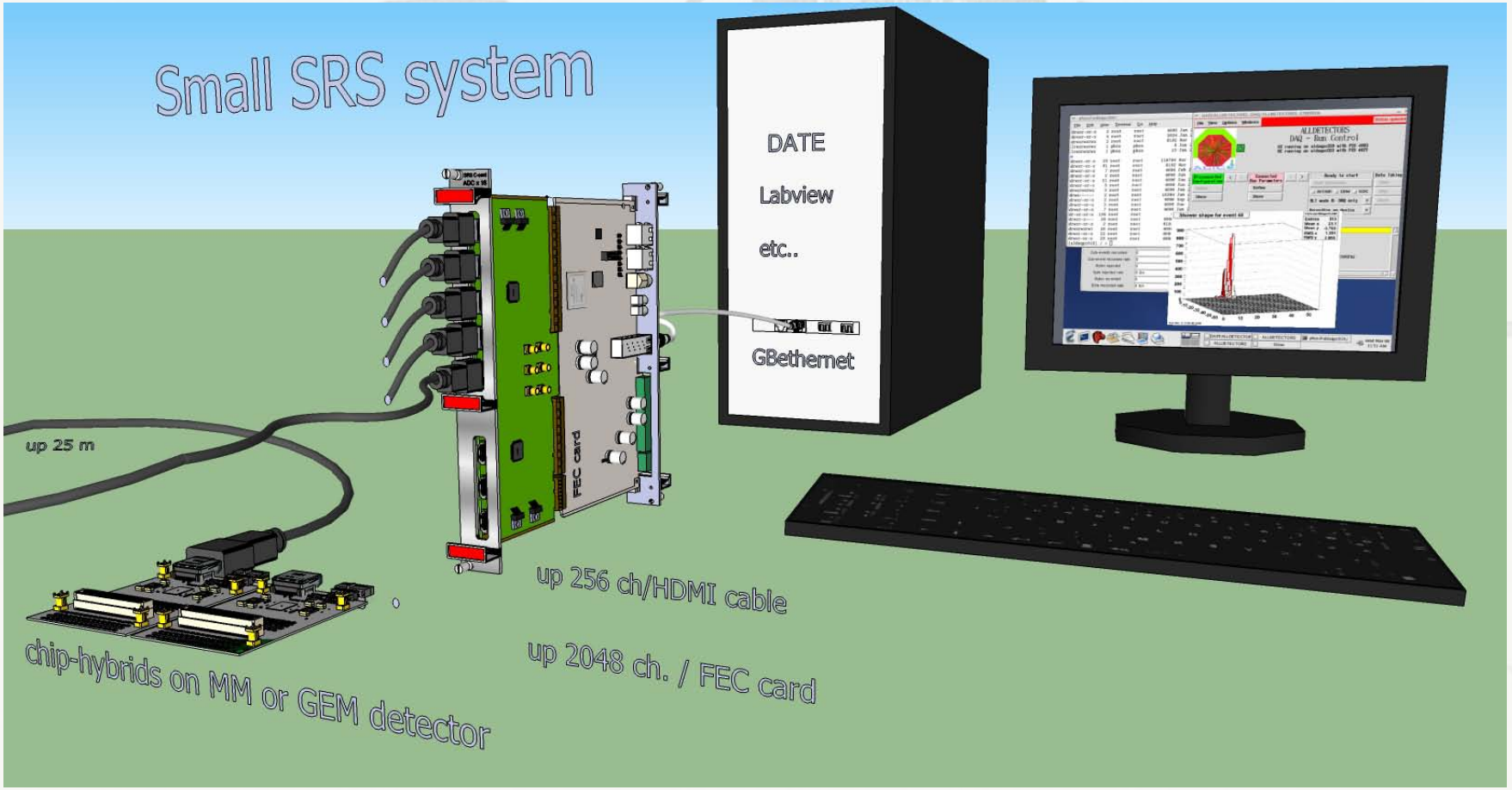
Status of the "Scalable Readout System" S. R. S.

for the RD51 collaboration
and LHC detector upgrades

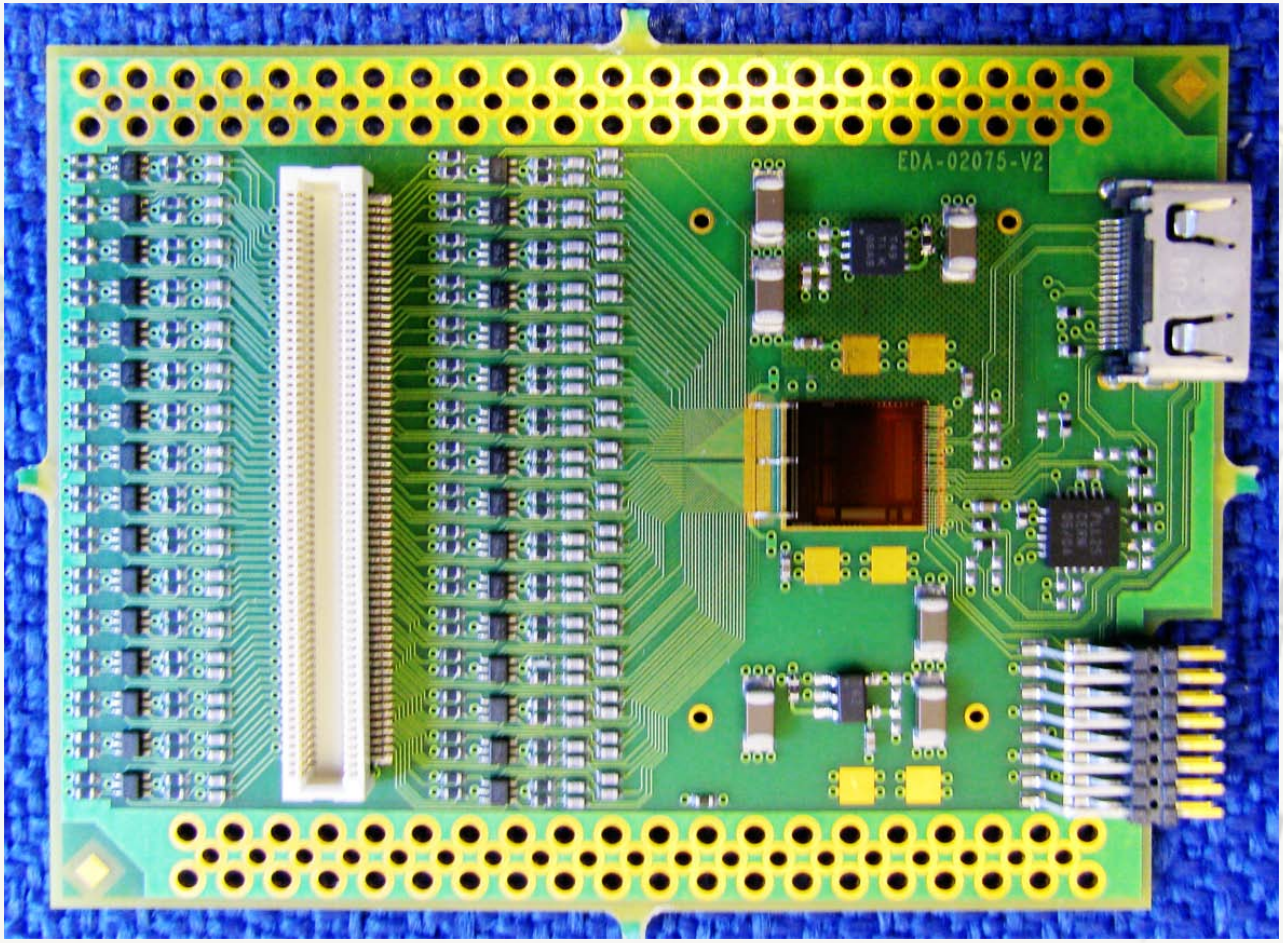
Collaboration meeting Bari, Oct . 7-10 2010

1st Target achieved:

small SRS system



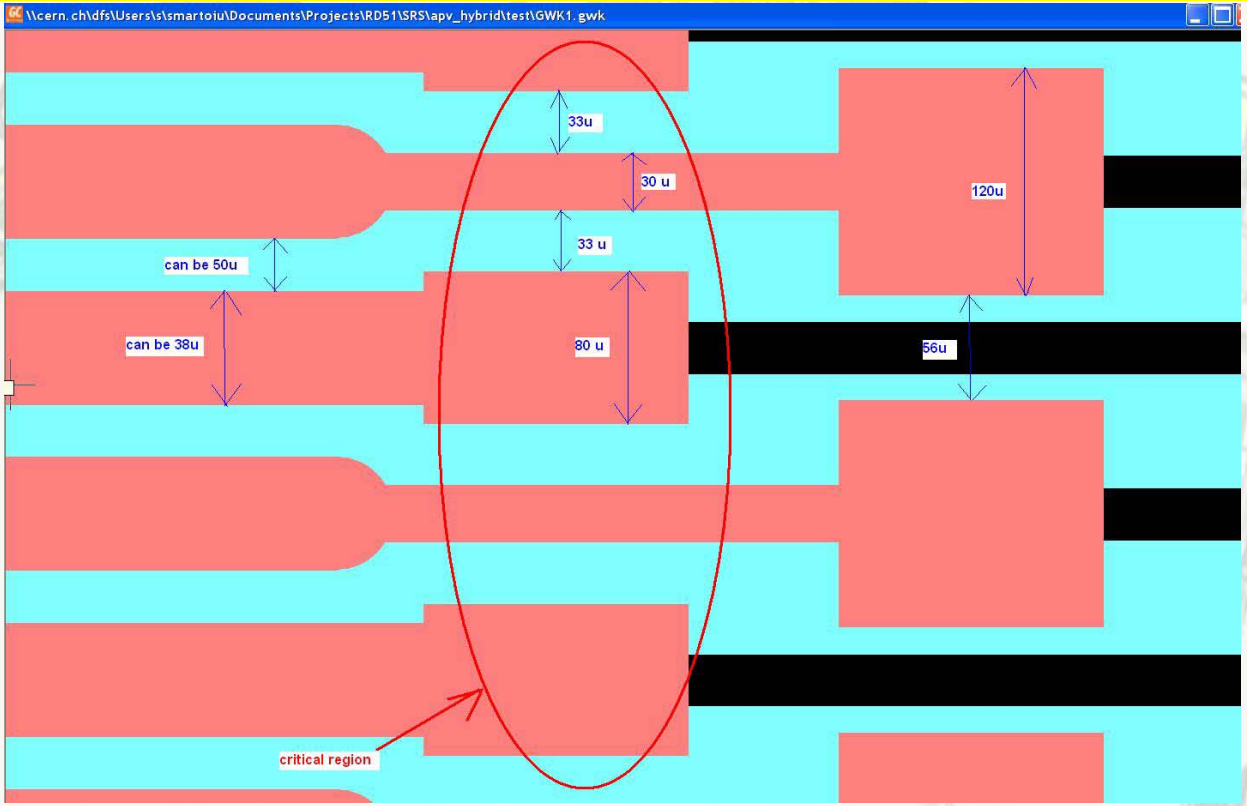
Revised APD hybrid V2



128 analogue channels, powered and read out via mini-HMDI connector

Hybrid production and bonding

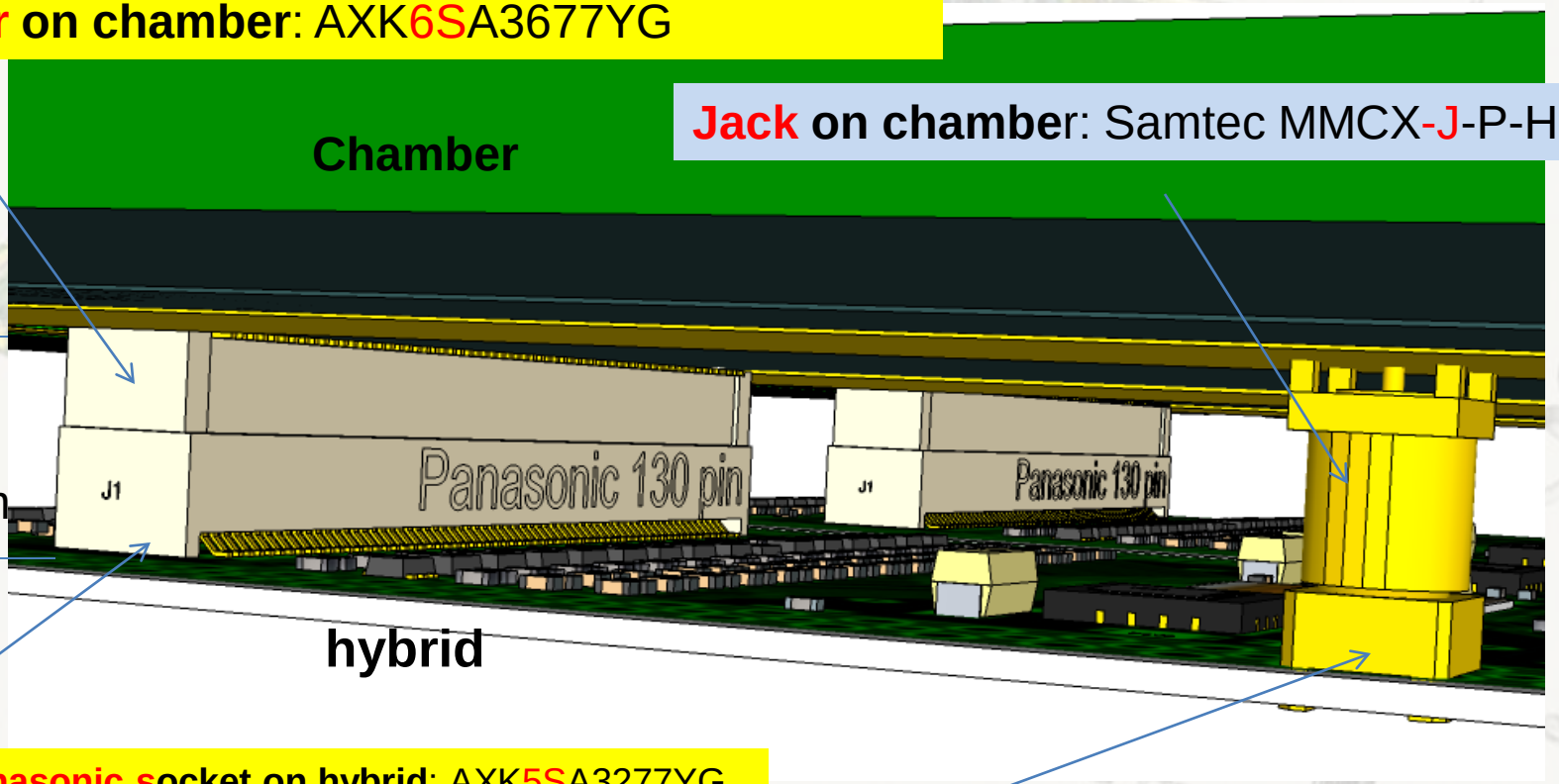
precision requirement is beyond 50u limit of most PCB manufacturers



Technology @ CERN can do it, however volume production requires commercial production (new more relaxed layout being worked on)

RD51 standard connectors

130 pin Panasonic 6.5 mm stackheight header on chamber: AXK6SA3677YG

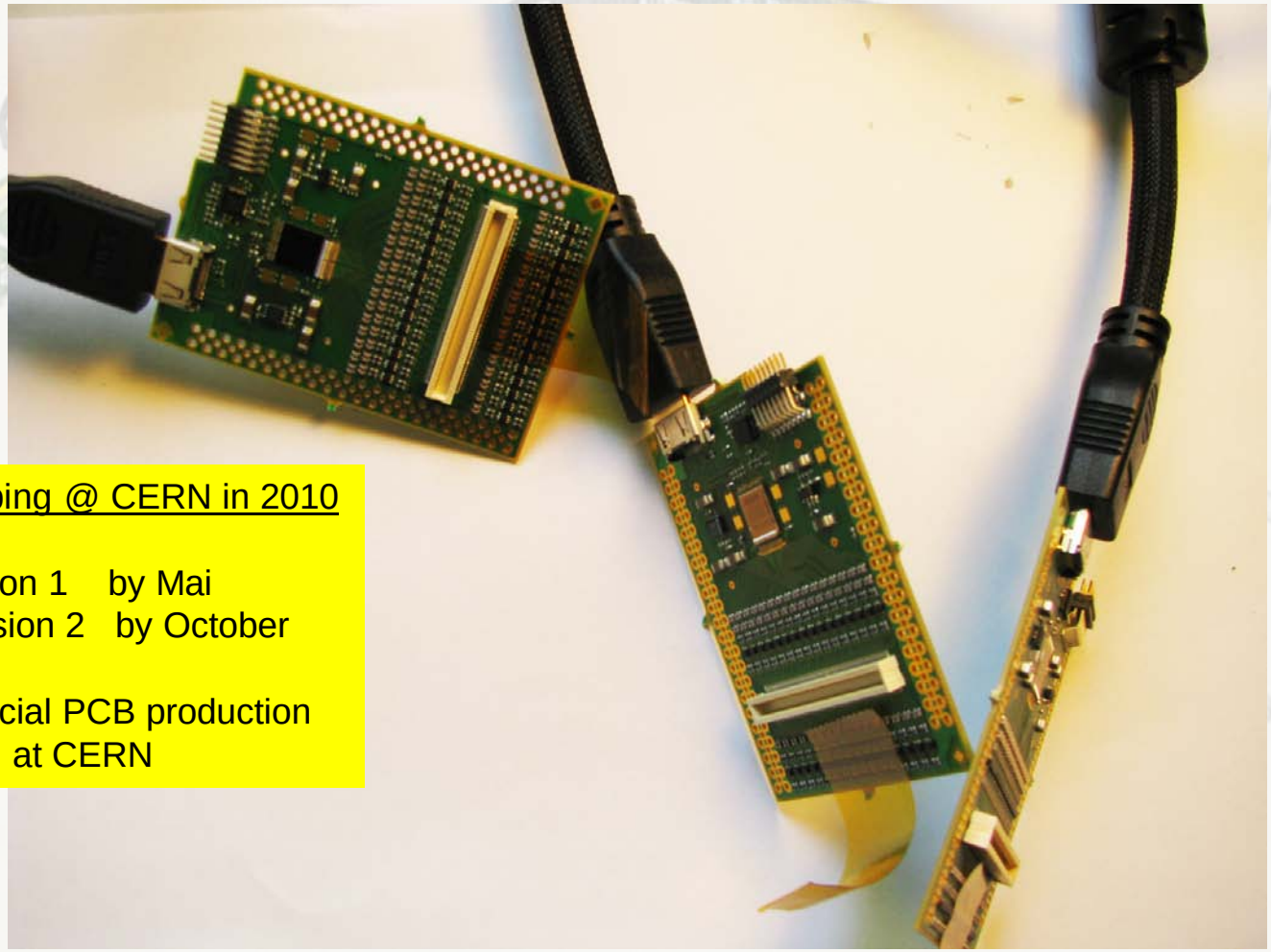


Jack on chamber: Samtec MMCX-J-P-H-ST

130 pin Panasonic socket on hybrid: AXK5SA3277YG
lifetime insertion cycles: 50
60 mOHM contacts

chamber ground and screwless fixation:
Plug on hybrid: Samtec MMCX-P-P-H-ST
2.5 mOHM, 0-6 GHz

Hybrids bonded, tested & powered



Hybrid prototyping @ CERN in 2010

7 hybrids Version 1 by Mai
11 hybrids Version 2 by October

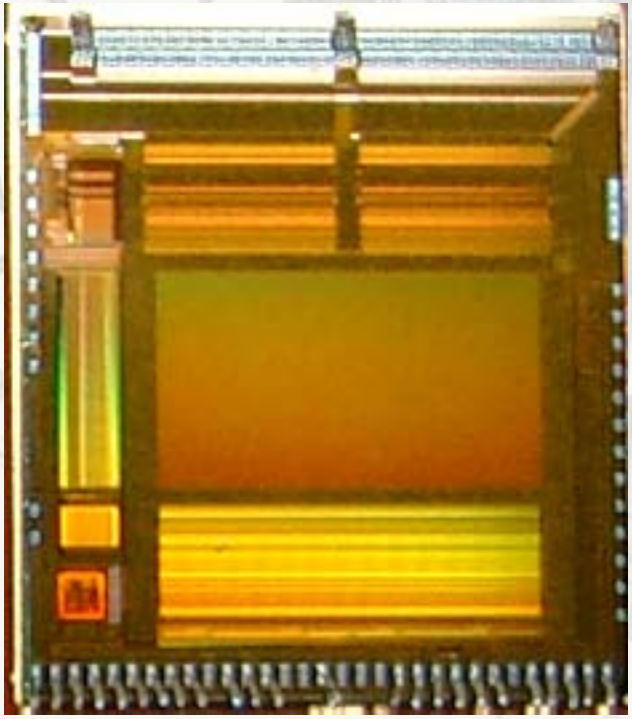
Next: -commercial PCB production
-bonding at CERN

APV chip status

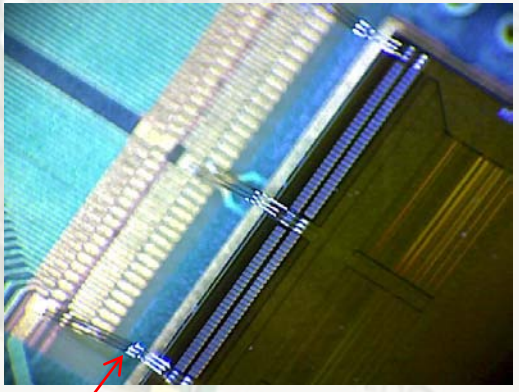
Total in stock:

RD51- 175chips
FTI - 160 chips

10% contingency
(not all chips work)



Version-2 hybrid
revised power , easier bonding
less noise



Bonding wires

CERN Bonding lab
QART Website: http://bondlab-qa.web.cern.ch/bondlab-qa/QA.html

SRS frontend cards

(Eurocard sized 3U and 6U)

PCIe connectors used as interface to A B or C cards

-PCIx1: GND, LV Power and HV (optional)
-PCIx8: GND, I2C, 3Gigabit Rx-Tx-Clk, 8 bit diff. Or 16 bit Control
-PCIx16:GND, JTAG chain,3Gigabit Rx-Tx-Clk, 16 bit diff. Or 32 bit Data

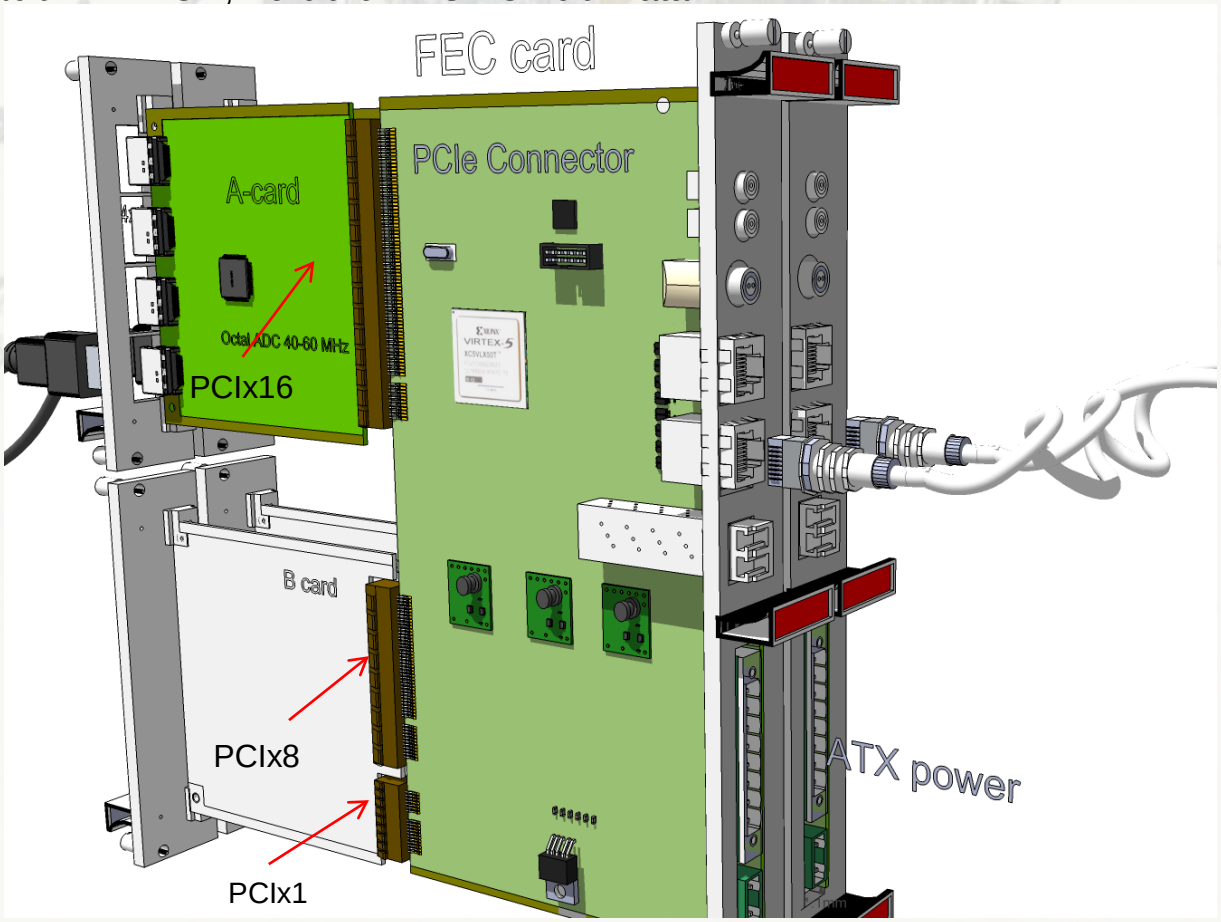
A –Cards: 3U for small detector interface logic

B –Cards: 3 U for miscellaneous extensions and LV-HV control

C – Cards: 6U for large detectors

So far, three types of C-cards

-ADC card CERN
-BNL chip card Arizona Univ
- LVDS card NEXT, Valencia



Adapter card C-format

ADC adapter for 16 analogue chip hybrids

Production Status
12 cards produced
15 needed 2010
10 more (min.) 2011

-APV-25 chip
-Beetle chip
-etc

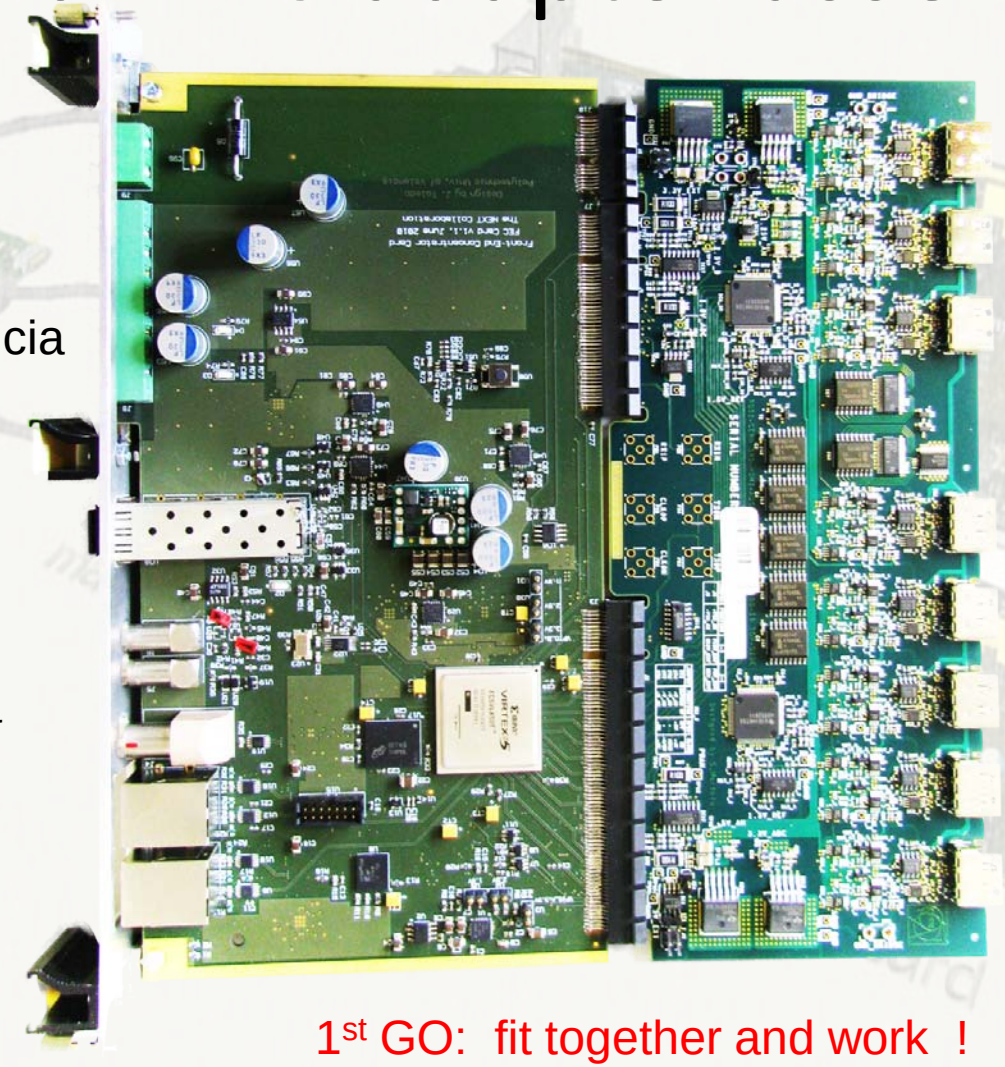
Power:
3V3 ~ 1.2 A + No APV x 0.25A
-5V0 ~ 0.4 A
+5V0 ~ 1.4 A
-12V0 ~0.01A

8 inputs for 16 hybrids
ADC: 12 bit@40 MHz

FEC and ADC adapter assembly

FEC card
designed @UPV-Valencia
by J.Toledo

Firmware:
Gigabit ethernet
Alfonso Tarazona



Octal ADC card
designed@cern
by S.Martoiu

Firmware:
Data processing
and buffering
S.Martoiu

1st GO: fit together and work !
minor modifications for volume production

HDMI cables*

(standard consumer items)

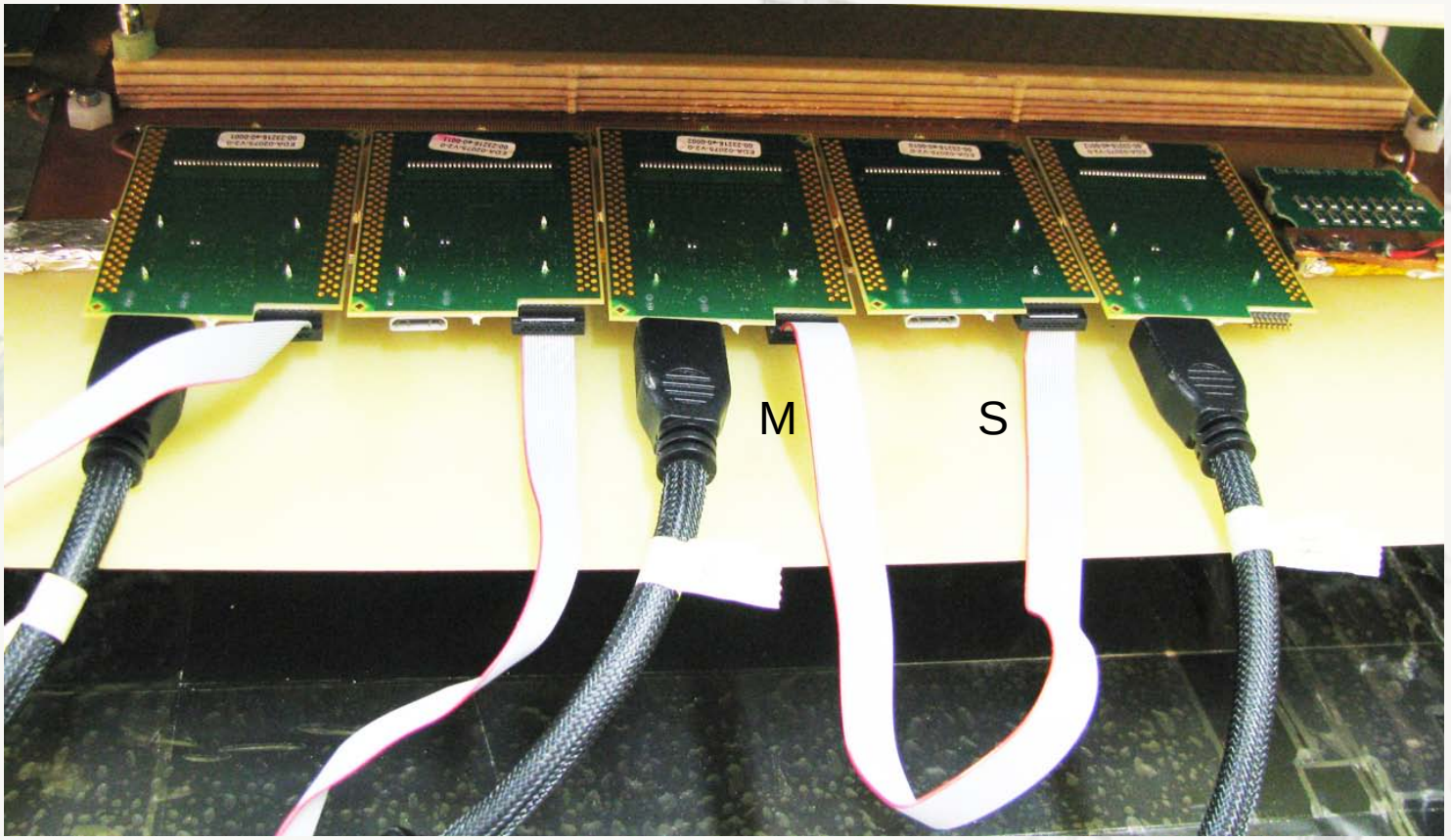
Mini-HDMI
on hybrid

Standard HDMI
on ADC

Coupler for long cables up 20m

*Note: we do NOT use the HDMI protocol

Hybrids on GEM chamber

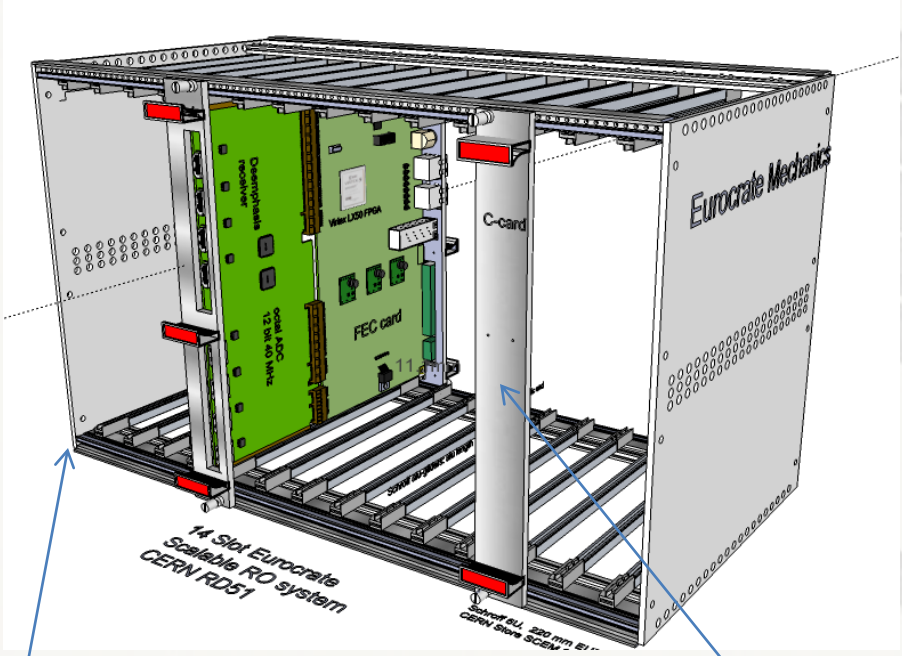


Flat cable 4 inch
Samtec FFSD-08-D0401N

Master-Slave configuration:
1 HDMI cable= 2 hybrids

Note: M and S hybrids are different !

Eurochassis 6U x 220



A and B cards:
41.6 mm: SCEM 06.61.62.143.0

C-cards only:
155.6 mm: SCEM 06.61.62.143.1

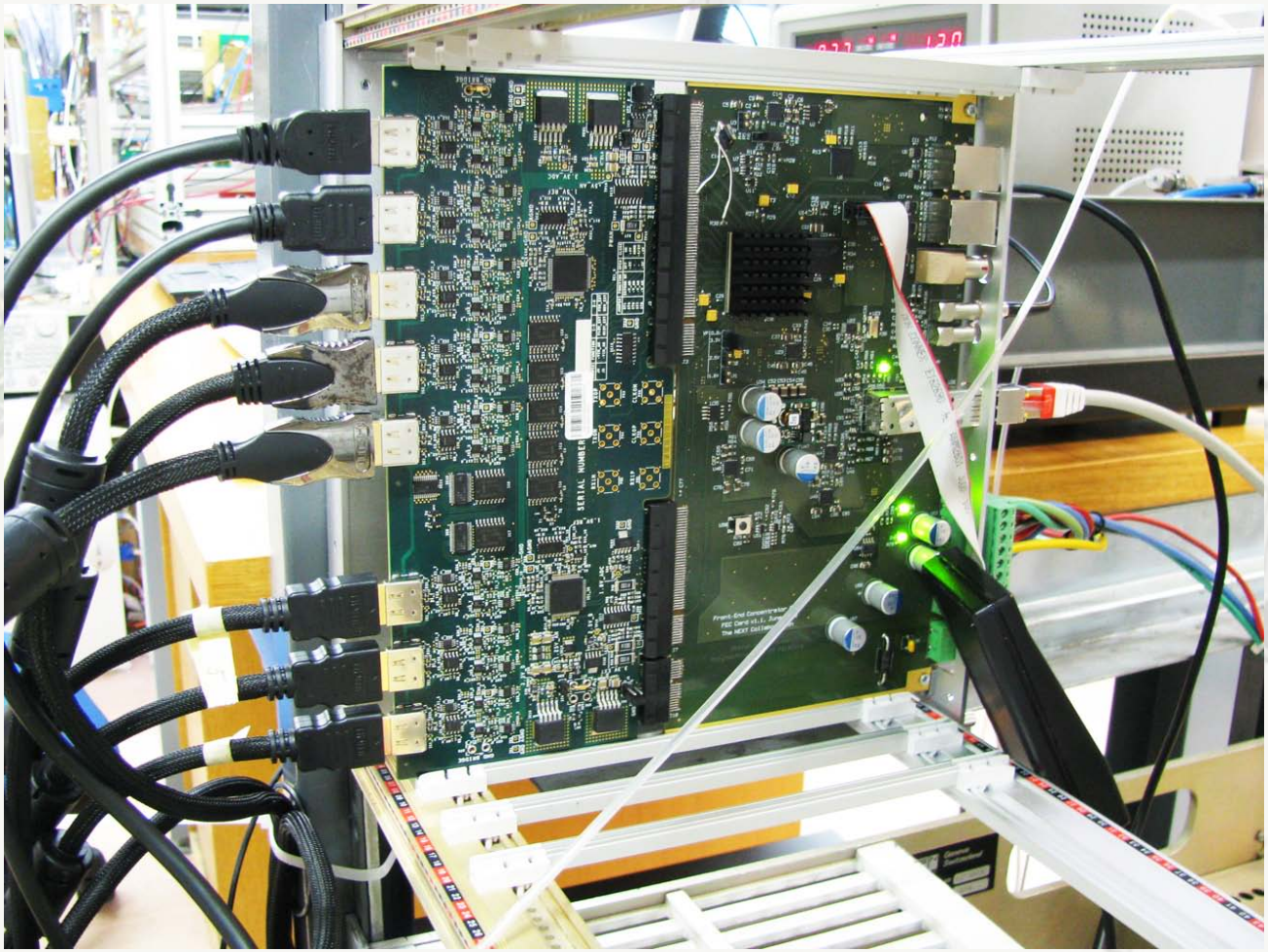
Chassis: 6U x 220 mm, CERN SCEM 06.61.61.045.7
Fabricant ATOS
http://www.atos-racks.com

Card guides for SRS CERN store:

C-cards and FEC cards:
Front panel set 6U-6TE with fixations:
CERN SCEM 06.61.63.156.3

A-cards and B-cards
Front panel set 3U-6TE with fixations:
CERN SCEM 06.61.63.056.6

1st small SRS* on GEM detector



8 HDMI cables
to GEM chamber

Trigger input
(NIM)

GB ethernet
to DAQ computer

Power

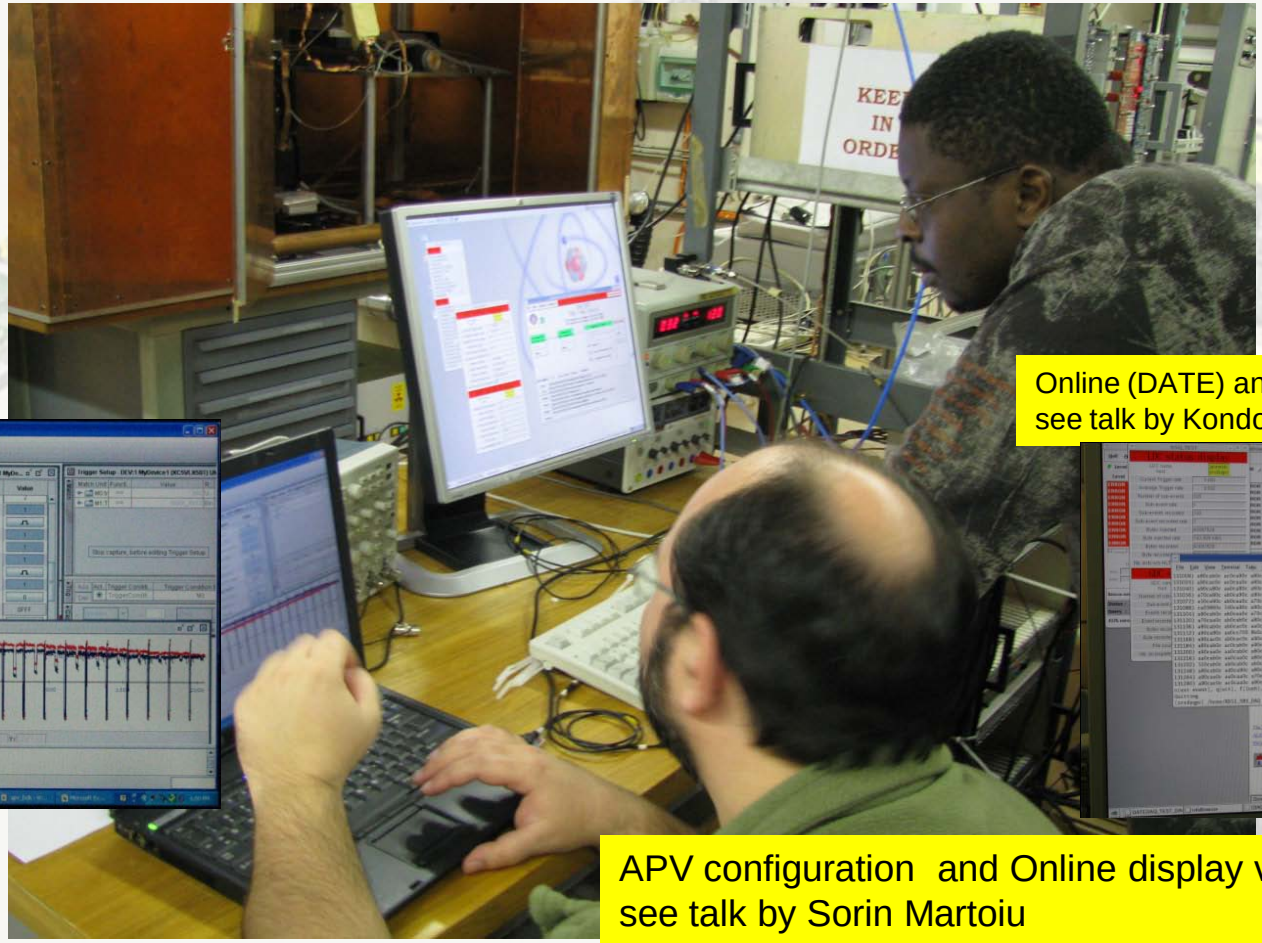
16 hybrids ~25 Watt

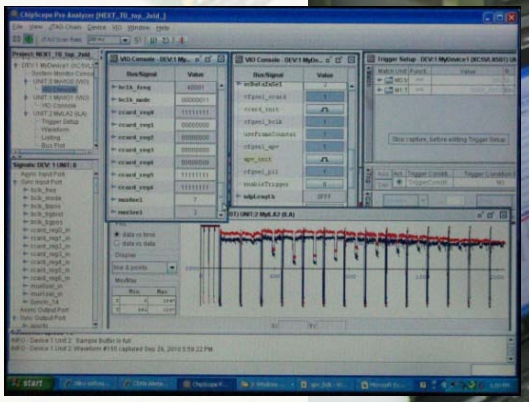
12.5 Watt hybrids
12.5 Watt FEC+ADC

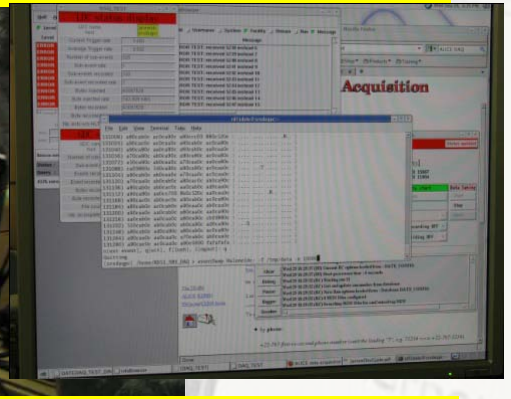
Eurocrate

* 1408 channels connected via 11 hybrids

1st SRS data with cosmics*





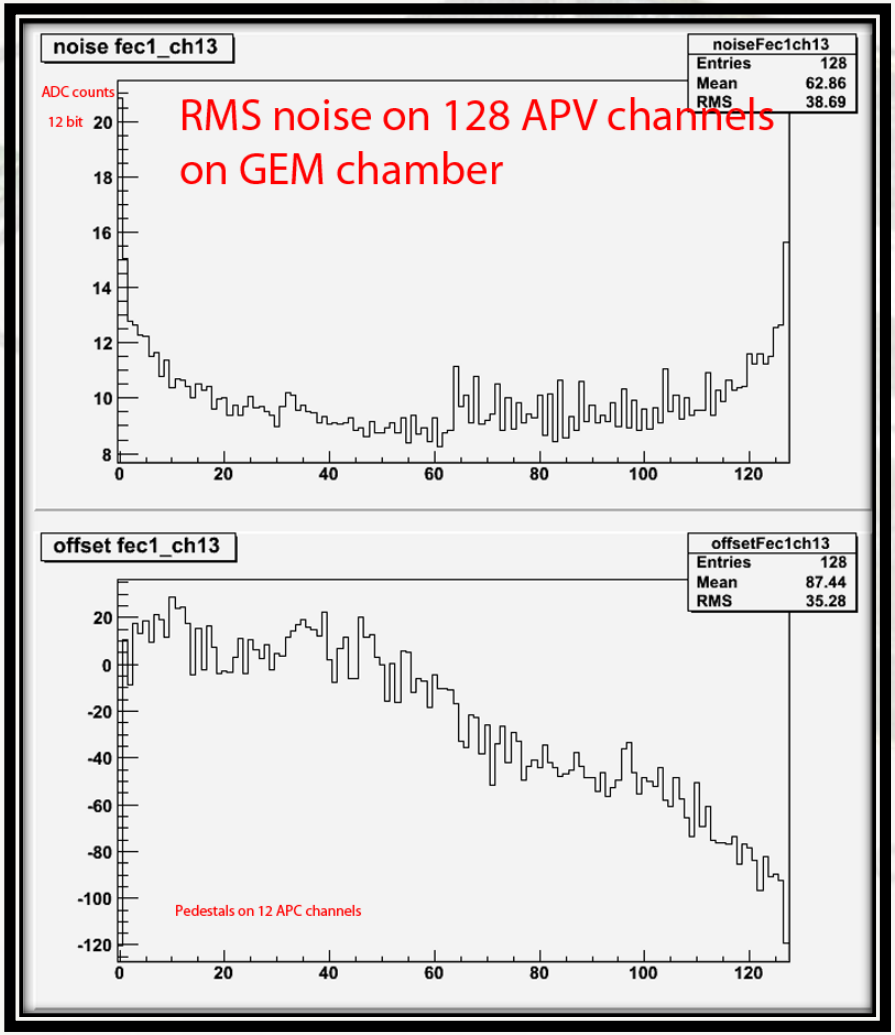


Online (DATE) and Offline (Amore): see talk by Kondo Gnanvo

APV configuration and Online display via Chipscope: see talk by Sorin Martoiu

* 3 days after moving SRS electronics to the RD51 lab

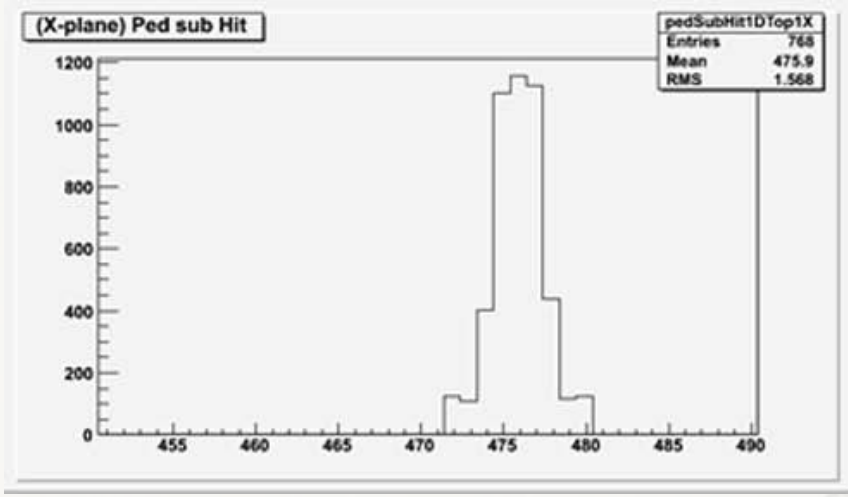
Offline noise and pedestals

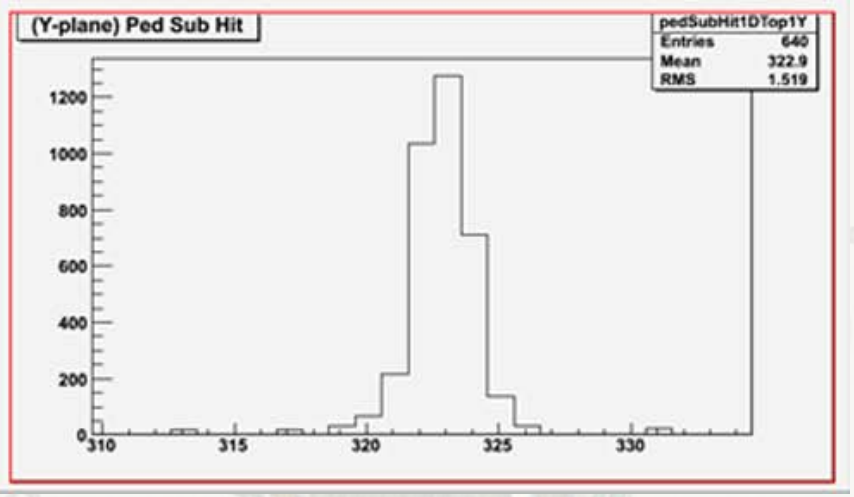


1 ADC count = 0.5 mV

RMS noise Order (5 counts)
12 bit ADC

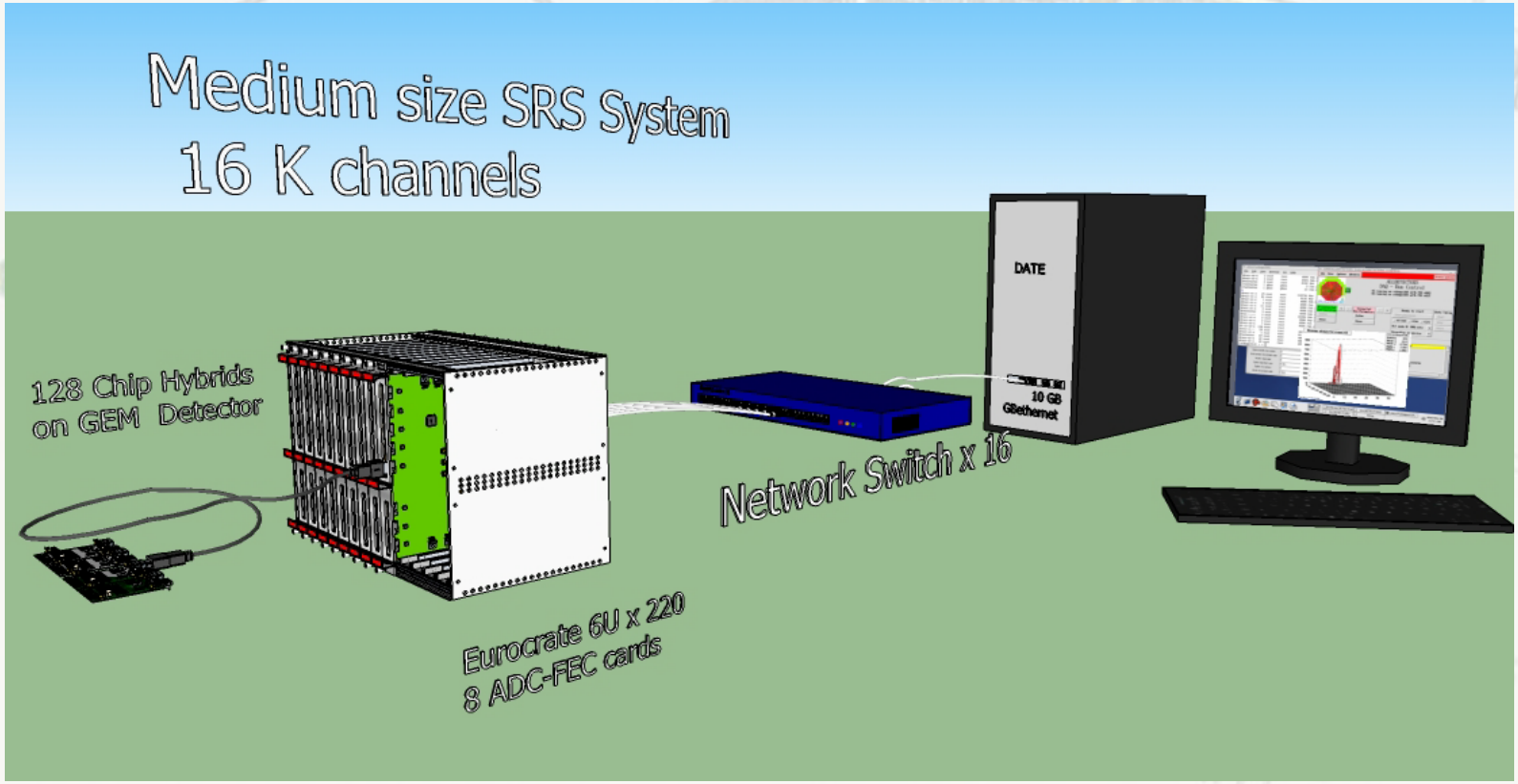
Cosmic event on GEM x-y planes





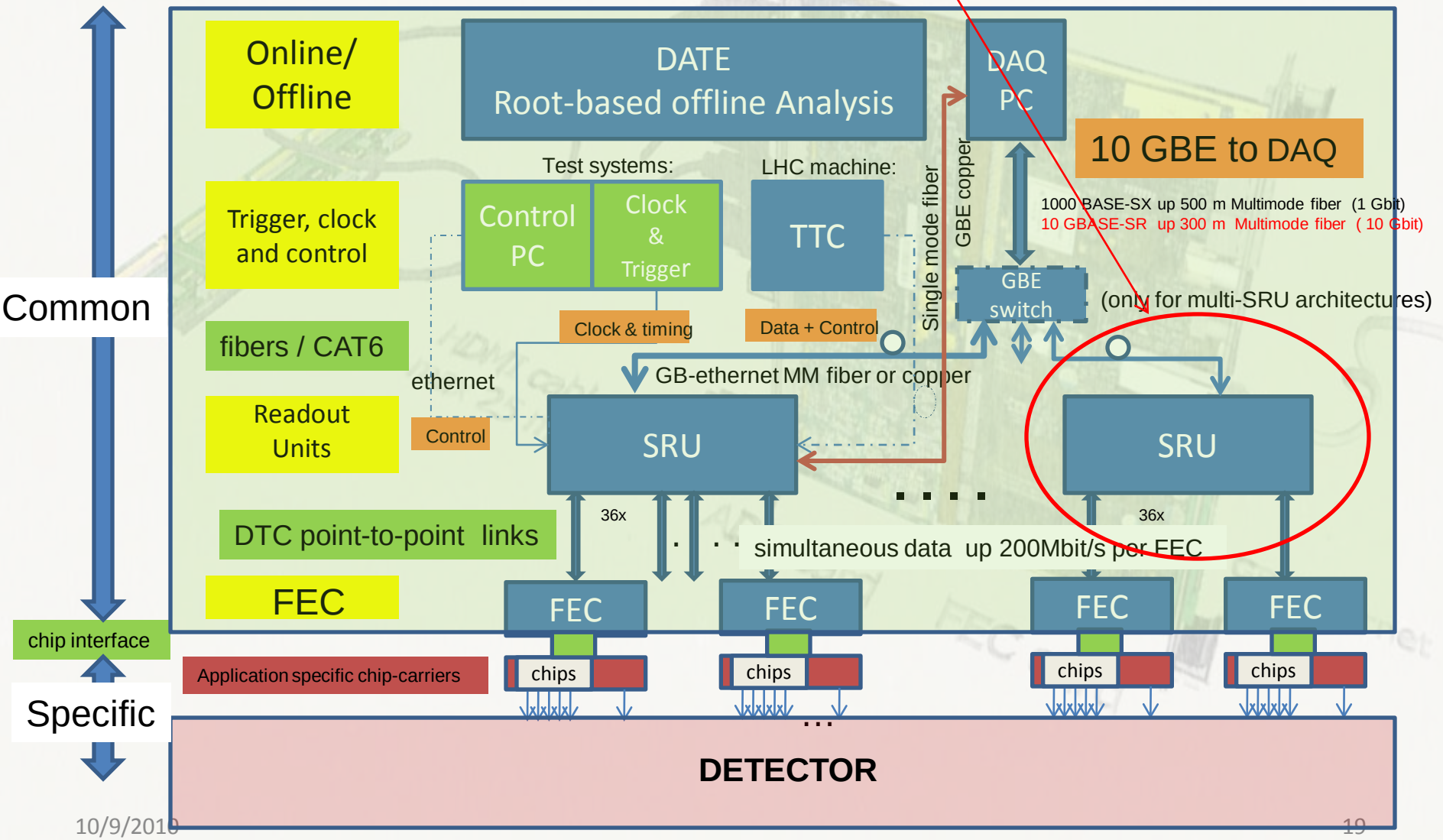
Conversion in electrons:
1 ADC count ~ 0.5mV
gain Order(80)mV/fC (to be defined)

SRS target by end 2010: 16 k channel system

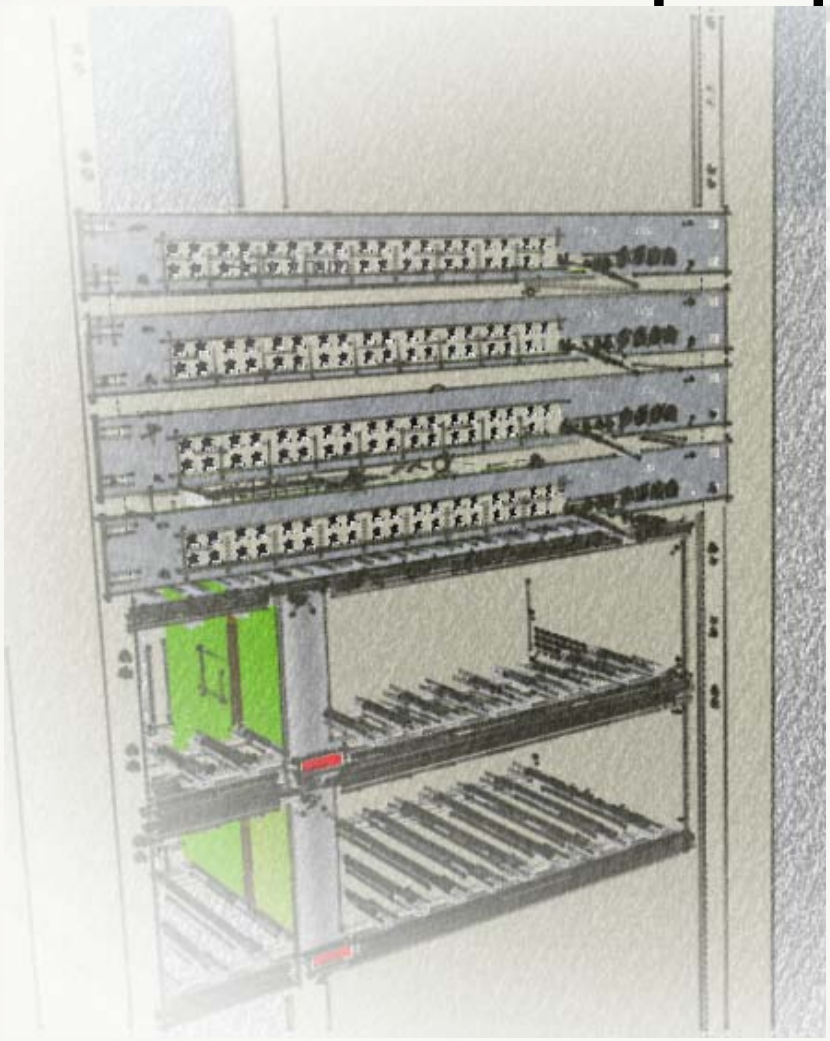


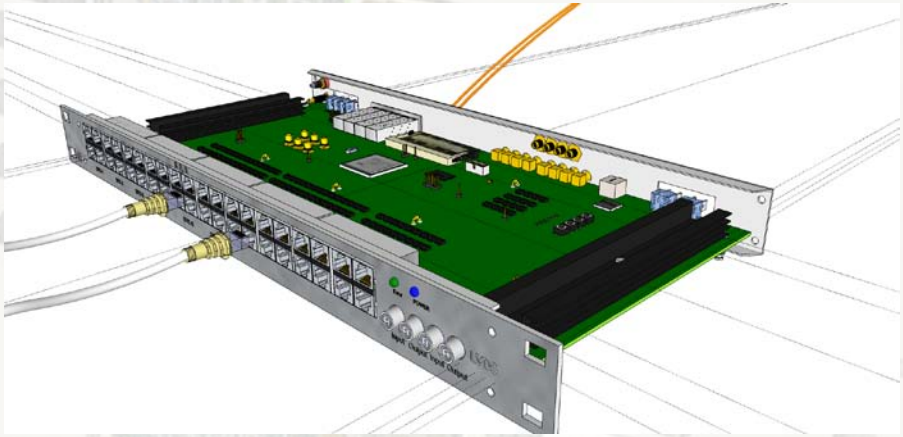
Scalable architecture > 16 k channels

➔ requires SRU



Large SRS system in preparation





Scalable Readout Unit

- 40 x FEC's via DTC cables
- 4 x SFP+ fibers 5 Gbit/s each
- Rack-mountable for large systems

Status:

11 PCB's halo-free produced in China
component mounting in Switzerland in Oct.
3 clients so far
Alice Calorimeters to order 20 more

User questionnaire SRS

Status received so far

Experiment/Team	Detector	Activity	Contacts	SRS need 2011	SRS need 2010	Manpower	Status	Trigger rate	Event size	% Chann
DAQ team ALICE	ALICE DAQ upgrade	Extension of DATE to Gigabit Ethernet Slow controls Program for SRS	Pierre.vande-Vyvre@cern.ch Filippo.costa@cern.ch		1 ADC, 1 FEC, 1 Hybrid 1 SRU, 1 Crate	20% CERN staff	Developer USER	10 kHz		
and	Detector upgrade ALICE (DAQ, CALO etc)	R&D and management of SRS	Hans.Muller@cern.ch			50% CERN staff	P.L. -SRS			
RD51-CERN	SRS system modules	Electronic design SRS hybrids, ADC, SRU, Firmware etc	Sorin.Martoi@cern.ch			100% CERN fellow RD51	DVELOPER			
ALICE , CCNU Wuhan, CN and	ALICE DCaL and PHOS Calorimeters	DTC link protocol and Adapter, Firmware, SRU Electronics Design	dczhou.iopp@gmail.cn		2 SRU	PhD, ass. Professor @cern 13 mo 1 year student @cern	USER,Developer	10 kHz	<100 kByte	5120 ch.
ALICE ORNL Oak Ridge, USA	ALICE EMCaL and DCal Calorimeter		Terry.awes@cern.ch		25 SRU, 700 DTC adapters	ORNL staff at CERN	Implementor	10 kHz	<100 kByte	20 kChanne
ATLAS Coll, MM, short term, CERN, CH	Micromega (Res. Strip) protos	Hybrid adapter to MM chamber	joerg.wotschack@cern.ch		1 ADC, 1 FEC, 8 hybrids 1 Crate	x% PhD on Firmware	USER,Developer	1 kHz	x kbyte	1000 ch.
ATLAS Coll. MM, med. Term, CERN USA	N x MICROMEGA DETECTORS	New Hybrids and Adapters	venetios.polychronakos@cern.c johns@physics.arizona.edu joerg.wotschack@cern.ch	BNL adapter, 1 FEC card x BNL hybrids, 1 crate		x % Fellow, x% PhD stud.	USER, Developer	< 75 kHz	x kbyte	10-20k ch.
Bonn and Mainz Uni. DE	TPC	Timepix adapter to SRS FEC	kaminski@physik.uni-bonn.de uschaefe@uni-mainz.de		1 FEC, 1 ADC ? 1 Crate	PhD stud. 50% Bonn/50% CERN	DEVELOPER Timepi	1 kHz		
Florida Inst. Technology, USA	GEM for Muon Tomography (MTS)	Offline and Online developments link for DATE users RD51	kgnanvo@fit.edu hohlmann@fit.edu		9 FEC,9 ADC,1 Crate 130 hybrids APV	1 postdoc @ CERN 6 month	USER,Implementor	< 1 kHz	small	16 k ch.
LIP, Coimbra, PT micropatterned RPC for s. animal PET upcoming application in		Tester...Can take some technical work (manual soldering, cables,etc)	fonte@coimbra.lip.pt	1 FEC, 1 ADC, 2 APV hybrids, 1 crate		?	USER	15 kHz	samples*2	160 ch.
HELSINKI, HIP, Finland	GEM detector and Si- 3D	Online and Offline	Francisco.Garcia@cern.ch	1 FEC, 1 ADC, 1 crate 16 APV hybrids		10 months student @ home inst	USER	10-50 kHz	50 kbyte	2048 ch
Istituto Superiore di Sanita INFN Roma, IT	GEM TRACKER	share information, common dev.	evaristo.cisbani@iss.infn.it	none	none	n.a.	OBSERVER	5 kHz	20 kbyte	?
Budker INP, Novosibirsk, Russia	triple-GEM & small angle stereo readout for DEUTRON experiment	R&D on two-stage cryogenic GEM (THGEM) de See comments	L.I.Shekhtman@inp.nsk.su A.F.Buzulutskov@inp.nsk.su	2 ADC, 2 FEC, 20 hybrids M 1 crate	none	2 senior scientists, 1 postdoc, 1PhD student for 3 years, 3 students for 2 years	USER	1 kHz	5kByte	2560 ch.
LAPP, Annecy, Fr	bulk MicroMega	hybrid design for SRS with MICROROC chip	gaglione@lapp.in2p3.fr	use ATLAS SRS infrastructure			USER,Developer	2 kHz	50 - 100 kbyte ?	
MEXICO, UNAM, MX	TGEM	?	guypaic@nucleares.unam.mx	1 ADC, 1 FEC, 1 crate 20 hybrids M/S		6 month student CERN/MEXICO ?	USER	2 kHz	?	2500 ch.
SAHA Inst Nucl Phys,KOLKATA, IN	MICROMEGAS	?	nayana.majumda@saha.ac.in	2012		?	USER	?	?	?
UPV Valencia, NEXT Collaboration, ES	Xe-filled TPC with PMT and SiPM readc via SRS	FEC card design, Firmware modules Online and Offline	JTOLEDO@ELN.UPV.ES	1 SRU	1 FEC, 1 LVDS adapter 10 ADC adapters 1 crate	2 students CERN+home inst.	USER, DEVELOPER	3 kHz	5.5 Mbyte	350 ch.
USTC Shanghai, CN GEM and MIcroMegas		work on hybrids	shenji@ustc.edu.cn zhaozg@ustc.edu.cn licheng@ustc.edu.cn	1 FEC,1 ADC, 2 hybrids 1 crate		PhD stud. 3-6 month @cern	USER,DEVELOPER	x kHz	x kByte	2x64 ch. 256 ch.
Zaragoza Univ, ES	MicroMegas	test and assembly of MM	Igor.Irastorza@cern.ch	1 FEC, 1 ADC, 8 hybrids		student @home inst	USER	10-100 Hz		1000 ch

Sheet1 Sheet3 Sheet4 Sheet5 Sheet6 Sheet7 Sheet8 Sheet2 Sheet9 Sheet10 Sheet11

17 replies
15 requests
4 to 6 SRS developers
+ more coming in

2011 requirement	2010 requirement
7 ADC cards	22 ADC cards
8 FEC cards	13 FEC cards
78 hybrids	139 hybrids
1 SRU	28 SRU
	700 DTC adapters
7 crates	5 crates

2012 production, testing integration and support..

SRS commercialization see talk by H.Hillemanns

Updated after talk: proto cost X consumed by RD51

Cost of SRS

pure production, no manpower, no profit*

1.) Investment cost prototyping X (cost advanced by RD51)

2.) Number of Prototypes N

3.) Cost of Volume production Y

4.) Number of RD51 Volume production* = M

5.) raw cost** C = (X+Y)/(M+N)

6.) RD51 cost for contributing RD51 members C =M/Y

7.) add 10% for handling, shipment etc. CC = M/Y +10%

* Limited volume according to user requirement questionnaire

** commercial cost may be considerably higher

Updated after talk, proto cost X consumed by RD51

SRS channel cost (prelim. RD51 users only)

Cost for RD51 users according questionnaire

1.) ADC card (2048 ch)

X =12kEu, N=12, M=20, Y=6.6kEu

C-**Cost (ADC)= 330 +33 = 363 Eu ➔ 0.177 Eu/ch**

2.) APV hybrid (128 ch)

x =15kEu, N=18, M=140, Y= 17kEu*

Cost (hybrid) = 121 +12=133 Eu ➔ 1.04 Eu/ch

3.) FEC card (2048 ch)

x = 9.5kEu, N=4, M=30, Y=35kEu

Cost(FEC) = **1167 + 117 = 1284Eu ➔ 0.627 Eu/ch**

Total small SRS system cost: 1.84 Eu/ch

NOT included:
HDMI cables
Power supply
Computer
Crate

*estimated for a hybrid PCB cost of max. 50 Eu

Minimal cost SRS:

1 ADC……363
1 FEC……1284
1 hybrid (128 ch)….133

1780 Eu

Add cost for : HDMI cables
Power supply
Computer
Crate

SRS cost estimate fast RD51 users

1 minimal SRS system 128 ch + PC + Crate + Power + PC

~3000-3500 Eu

add 150Eu per 128 ch hybrid + cables

SRS developers current status

Firmware

1. Firmware V5 FPGA on FEC:
   Gb ethernet, ADC Deserializer, Slow controls, Trigger, Buffering and formatting for DATE, Z-suppression, Other chips, etc..
   UPV Valencia, CERN-RD51, (INFN Napoli ?) , ...
2. Firmware on V6 FPGA on SRU:
   10 GBethernet, Subevent building, Slow controls, Trigger, Buffering and formatting, DTC links, Online Algorithms
   CERN-RD51, UPV Valencia, CCNU Wuhan, ...

Hardware

1. Adapter cards C format
   ADC card, LVDS card, BNL card, (MicroROC?), (Timepix ?)
   CERN-RD51, UPV Valencia, Univ. Arizona,
2. Adapter cards A and B format
   N channel HV bias 10 bit for APD/Si-PM (planned), ...
   tbd.
3. FEC card V1.2
   UPV Valencia
3. SRU Rev 2
   CERN-RD51, CCNU –Wuhan, ORNL
4. SRS Power
   ATX adapter/RMI filter (advanced design)
   tbd

Software

1. DATE Online for SRS
   Gigabit Equipment for DATE, SRS integration with DATA formats, RD51 User contact
   CERN-ALICE, FIT Florida,
2. Online Quality Monitoring
   AMORE / Root based
   CERN-ALICE, FIT Florida
3. Slow Contols via Online DAQ system
   CERN-ALICE, UPV Valencia

About chip candidates for SRS

SRS was designed to allow choice of frontend chip

the optimal chip interface is serial (analogue or digital)

RD51 maintains a chip matrix under
https://espace.cern.ch/rd51-wg5/chipmatrix/default.aspx
please tell us if you want to add a chip to the knowledgebase
popular chip candidates: APV25, Beetle, VFAT, AFTER

The first SRS chip adapter implementation was made
this year for the APV25 (+Beetle)

VFAT is on hold until it becomes available (
AFTER and NX-YTER would require some team to build the adapter
Adapter for BNL chip was started by ATLAS/Univ. O. Arizona
Adapters for emerging chips, MICROROC, Medipix are considered

More chips possible, their integration in SRS is user-driven

SRS users and plans far

GEMs

1. FTI Florida, GEMs for MUON Tomography , 16 kCh, SRS (see talk by Kondo Gnanvo)
2. Budker INP, Triple GEM Deteron Exp. 2.5 kCh, SRS
3. HIP Helsinki, GEM and Si-3D, 2kCh, SRS
4. ISS, INFN Rome, GEM Tracker, inhouse VME
5. UNAM, Mexicao , THGEM, 2kCh, test system SRS
6. UST, Shanghai, GEMs, 256ch, test system SRS

MicroMegas

1. ATLAS MM upgrade 1K res. Strips -> 20 kch with BNL chip on SRS (see talk by V.Polychronakos)
2. LAPP Annecy , MicroROC chip test with ATLAS MM, 1k ch
3. SAHA Kolkota, 1k ch test system (2012)
4. Zaragoza Univ, R&D on MPGD for rate event search

TPC

1. UPV Valencia, TPC with PMT and Si-PM, 350 ch SRS (see talk by Jose Toledo)
2. Bonn and Mainz Univ. Medipix/Timepix adapter SRS

PET detectors

1. LIP Coimbra, Micropatt. RPC for s.animal PET, 160 ch SRS

Calorimeter

1. ALICE Calorimeters, new readout backend via DTC links and SRU, 20k ch SRS

Contest

looking for a new name of SRS

Proposals so far (dinner yesterday)

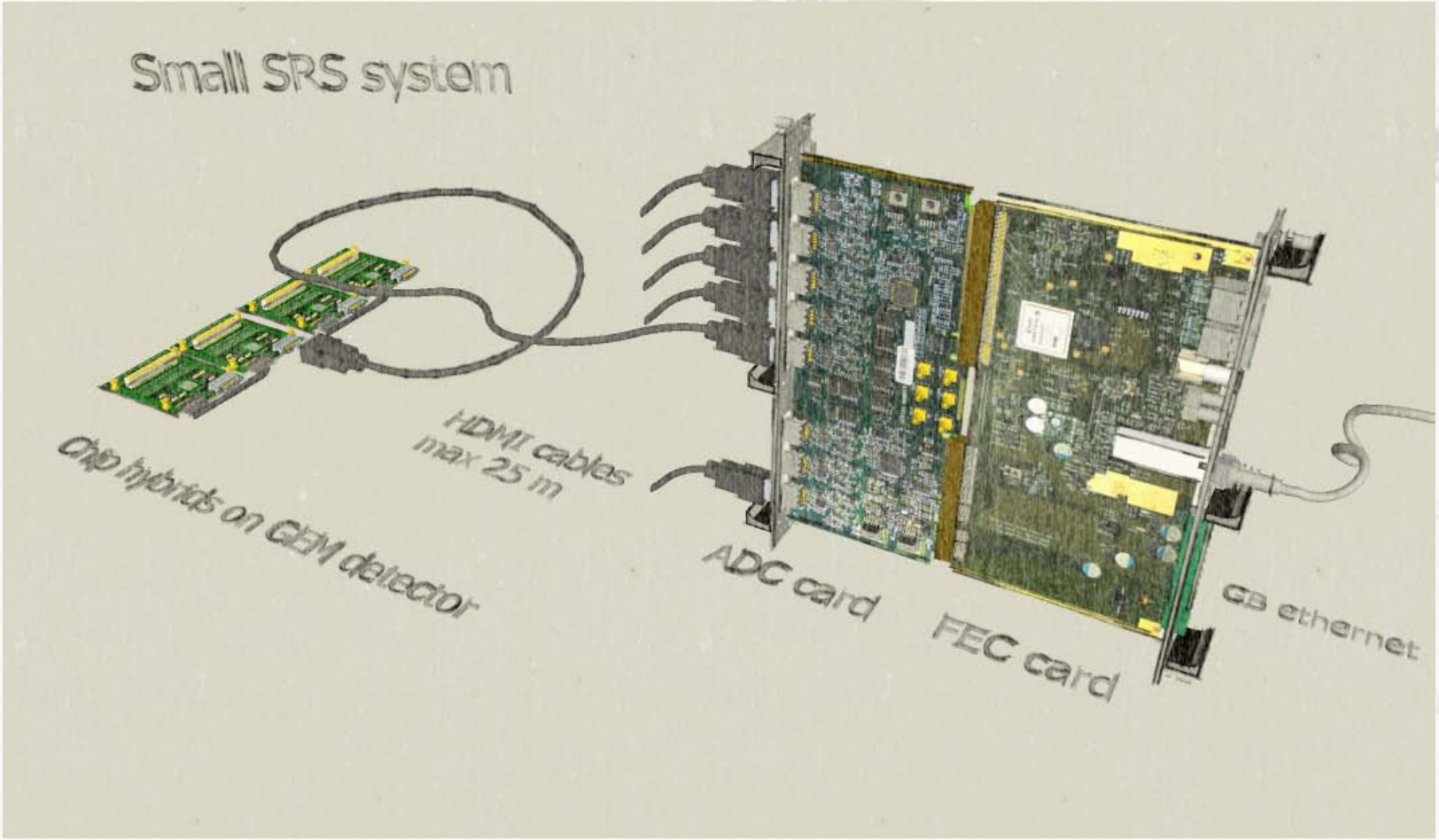
MuScaT Multichannel Scalable Technoloy

Please send ideas

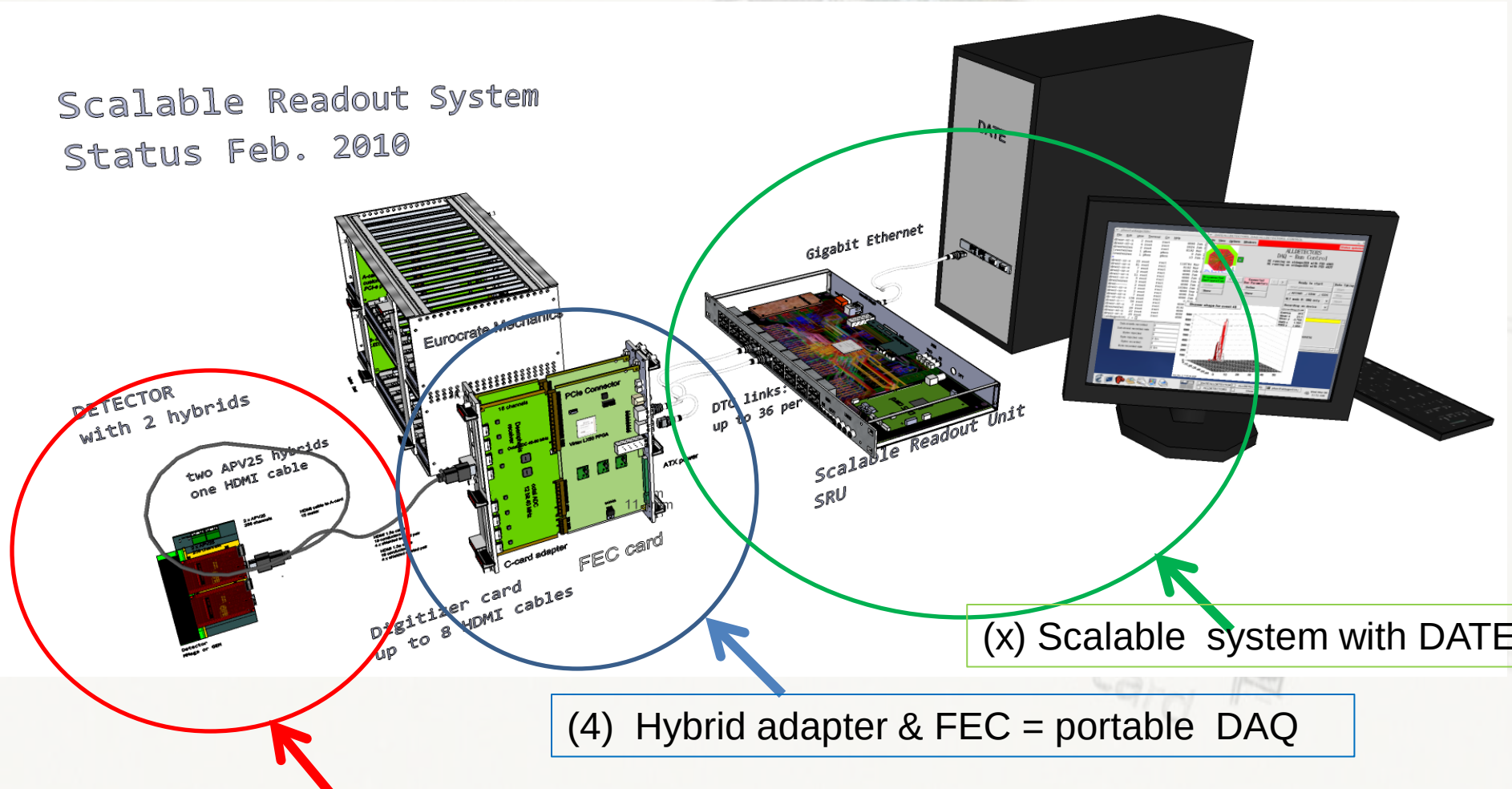
Summary

- First SRS modules and hybrids available for RD51
- First DATE SRS Online system successful (RD51 contact K.Gnanvo)
- Larger SRS production being prepared (based on questionnaire)
- First small SRS systems established FTI-Florida and NEXT Valencia
- FTI system taking cosmics in the RD51 Lab with DATE and AMORE
- More small systems in preparation (2010: ATLAS MM with INFN Napoli)
- SRS developer base is increasing on all levels HW, FW and SW
- new SRS HW cards (APV bias, 1ns LED system) possible, contact us
- Collaboration with related projects and input from users welcome
- Large Scalable System (SRU, DTC) in preparation (Alice Calorimeters)
- SRS became case for Technology Transfer to Industy (CERN TTN)
- Interested as user, developer ? Please fill in the RD51 qestionnaire

BACKUPS


Small SRS system
HDMI cables
max 25 m
chip hybrids on GEM detector
ADC card
FEC card
GB ethernet

physical overview SRS



(x) Scalable system with DATE

(4) Hybrid adapter & FEC = portable DAQ

(1-5)Hybrids: user –specific front end electronics with discharge protection