Status report on the 1 m^2 Micromegas prototype for Digital Hadronic Calorimetry

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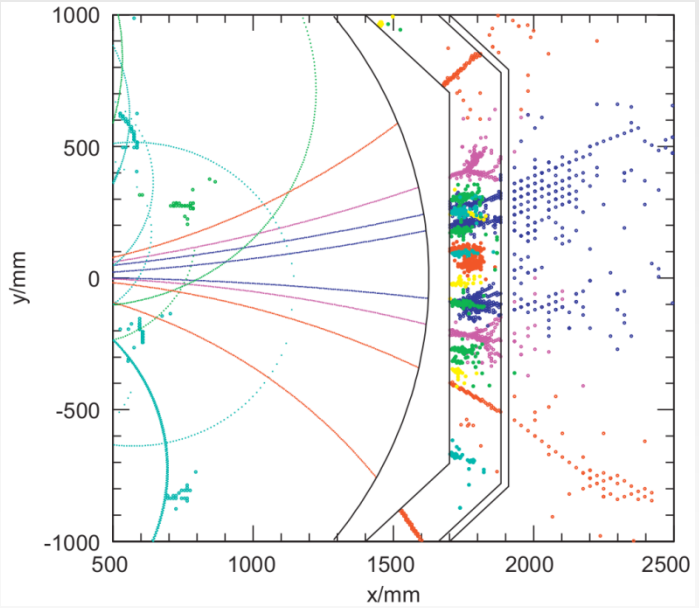
Outline

- Calorimetry at ILC
  Performance of small size prototypes
- Large board test and 1 m^2 prototype assembly
- Test in a beam @ CERN/SPS
- New front-end electronics
- Conclusion

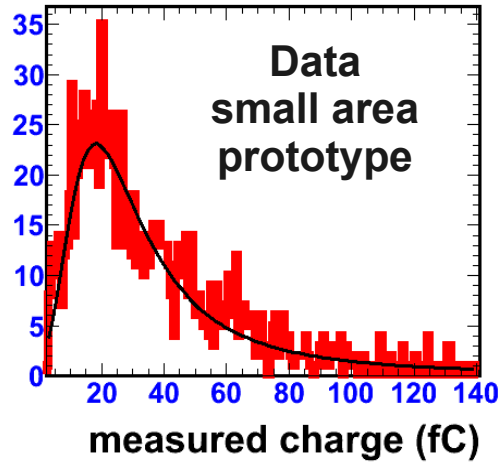
Introduction

- ILD/SiD calorimetry at ILC is based on the Particle Flow
  → granularity more important than resolution
- The ILD concept calorimeter would have 30 millions of channels
  → digital readout of 1 cm^2 cells
- Loss of linearity at high energy (≥ 100 GeV/c)
  → semi-digital readout
- Instrument HCAL gaps with gaseous detectors
  → RPC, GEM, Micromegas

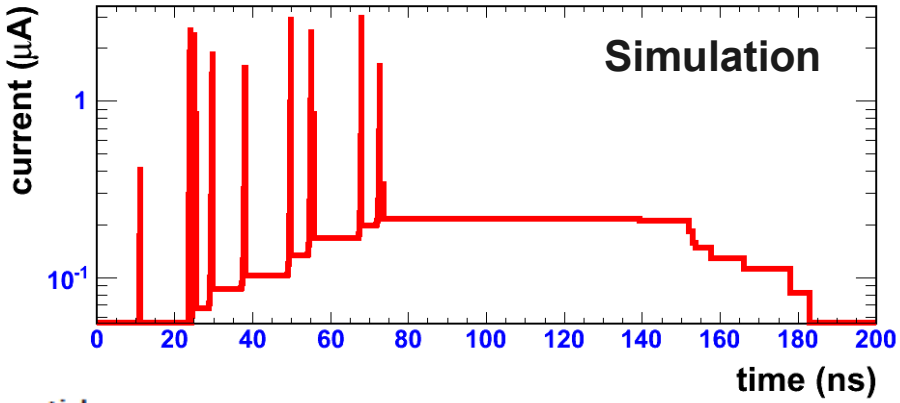


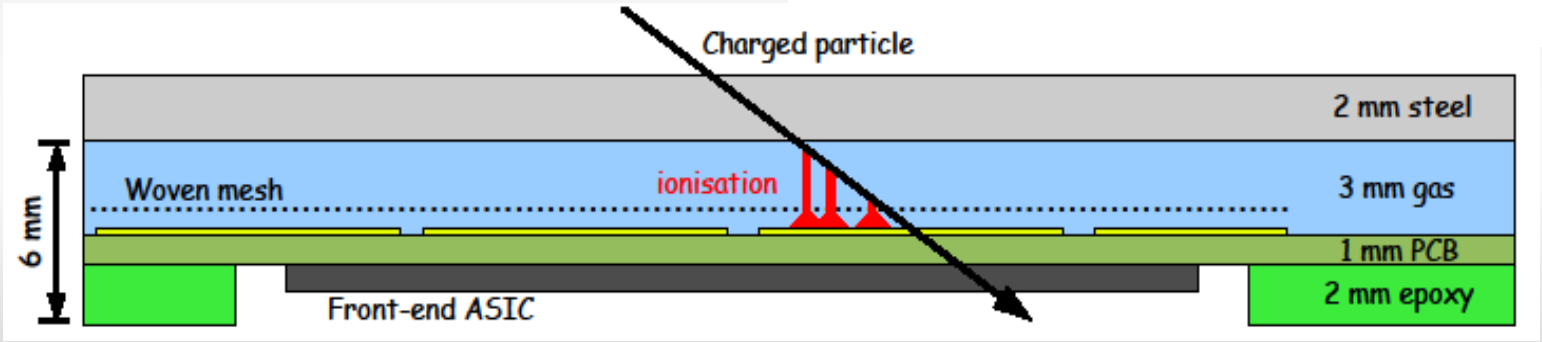
Detector layout and signals

- Layout
  - 3 mm drift gap (Ar-based)
    → 30 primary electrons (10 MPV)
  - 128 um amplification gap
    → gas gain up to 15.000 with MIPs
  - 1 cm^2 pads
  - Embedded frontend electronics
    → Total thickness < 8 mm



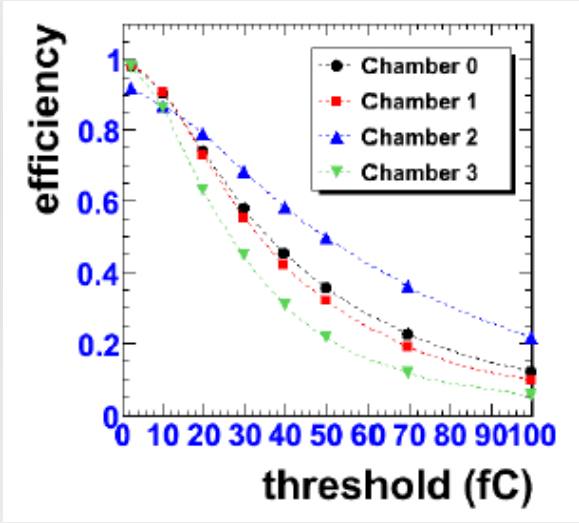
- Signals
  - Collection in 60-80 ns
  - Amplification in 100-200 ns
  - Most probable charge of 20-25 fC

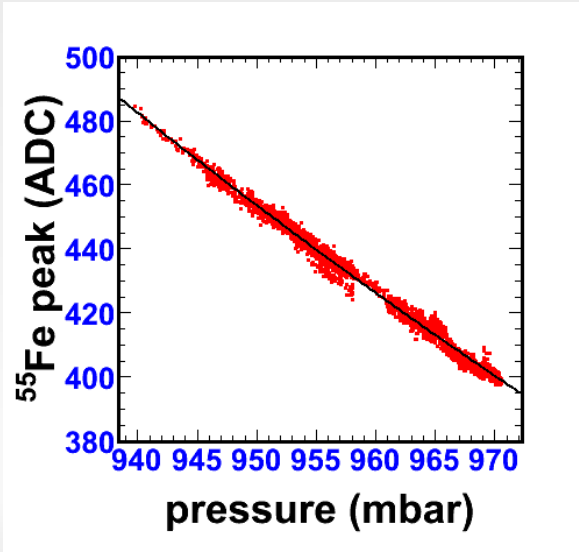


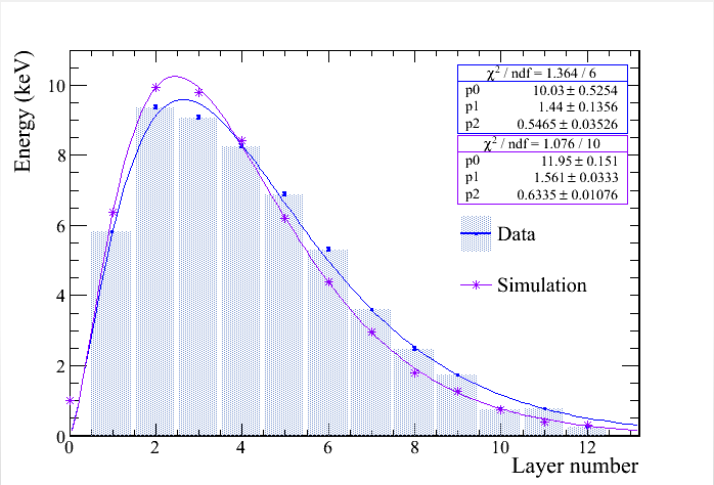


Performance of small prototypes

- Threshold of 1.5 fC – area of 6x16 cm^2
  - Signal uniformity dominated by gap variations **20 fC with 10 % variations**
  - Very good efficiency **97 % with 1% relative variations**
  - Pad multiplicity close to geometric limit **between 1.05-1.10** (decreases with threshold)
- Gain sensitivity to ambiant parameters
  - -0.6 %/mbar & 1.4 %/K
- Successfully tested in showers (CERN/PS)





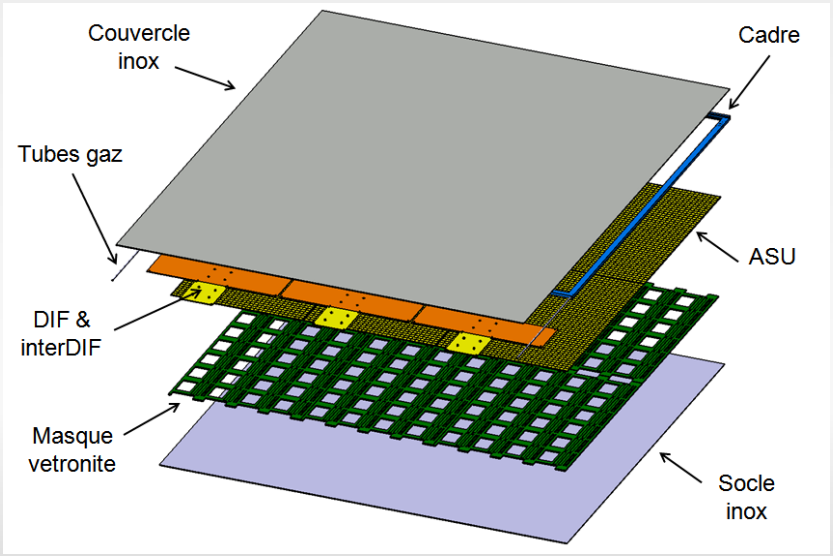


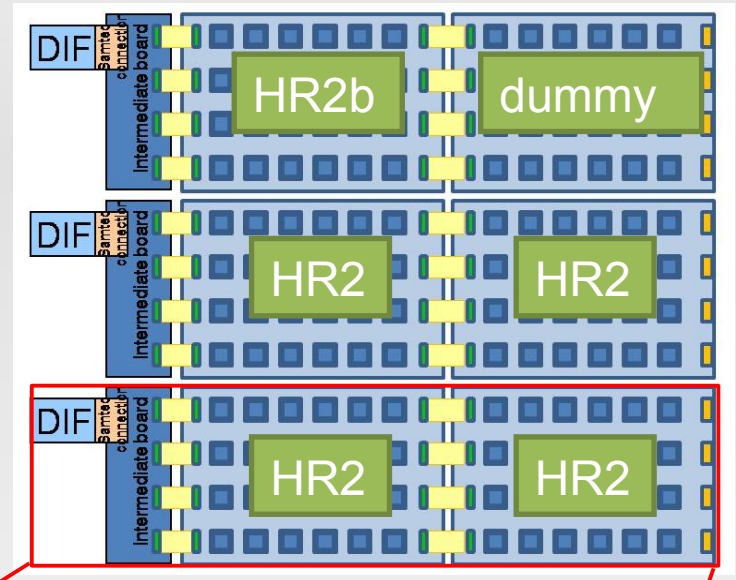
1 m^2 prototype design

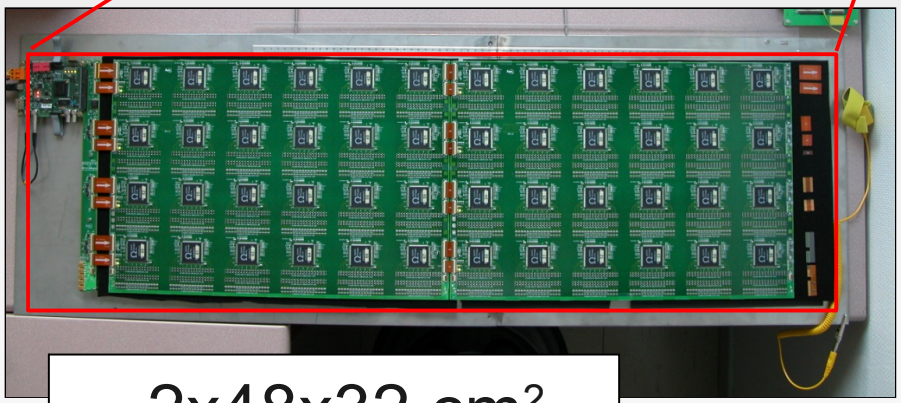
- Choice : 6 meshes of 32x48 m^2 (1536 channels)
  → Active Sensor Unit (ASU)
- 24 ASIC / ASU
  data from 2 ASU (= slab) read out in line (flex cables)
  1 Detector interface board (DIF) per slab
  →3 boards for a 1 m^2 prototype

- 1 mm gap between ASU + cathode spacers
  → 2 % dead area inside gas volume
- Total thickness = 2*2 mm steal covers + 8 mm = 1.2 cm

- Assembly procedure validated with mechanical prototype in 2009







2x48x32 cm^2

Front-end ASIC

- HARDROC2 chip (LAL/Omega)
  - 64 channels with
    preamplifier, fast shaper (20 ns shaping time)
    3 discriminators and a 127 event depth memory
  - Individually adjustable preamplifier gains
  - Global discriminator threshold
  - Power pulsing capability

- 2 bit information (0/1/2/3)
  but 1 threshold used so far

- Channel reponse to input charge
  is an S-curve, at 0 charge:
  - the inflexion point is the pedestal
  - the width relates to the noise

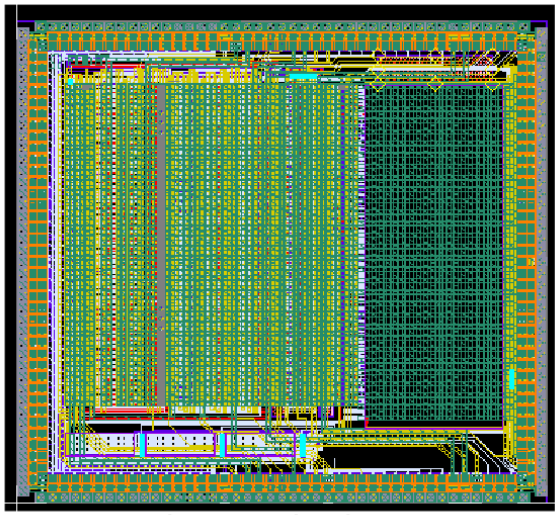
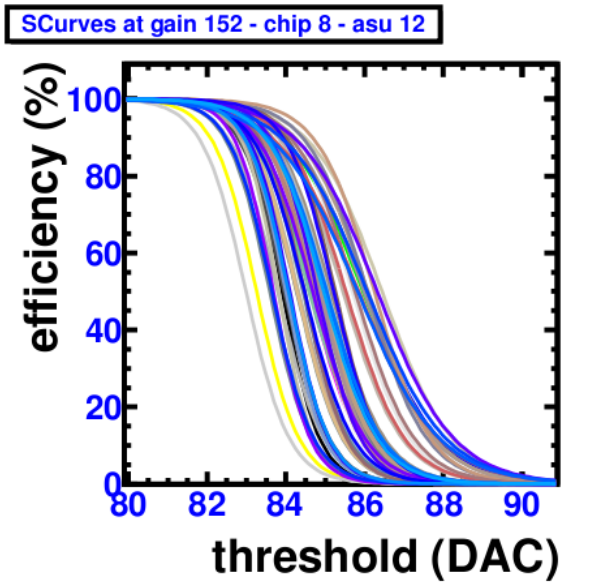


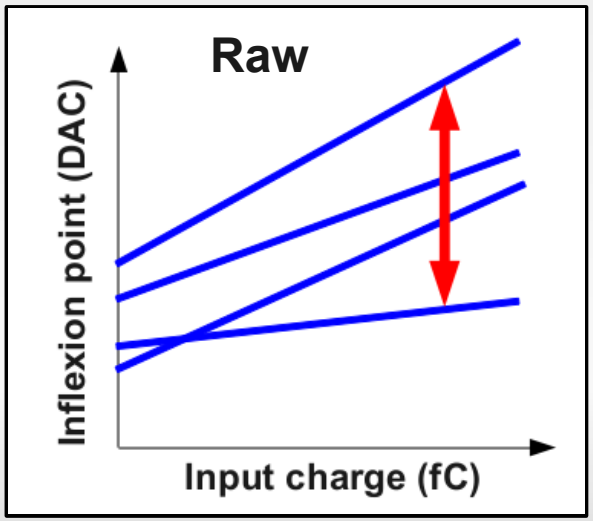
Figure 1 – Hardroc2 layout

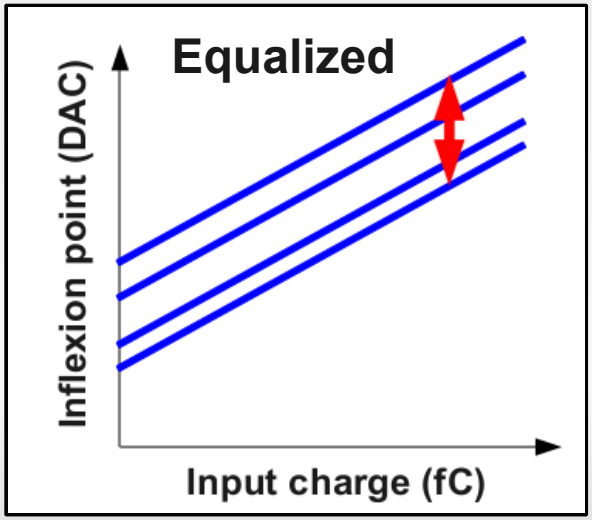


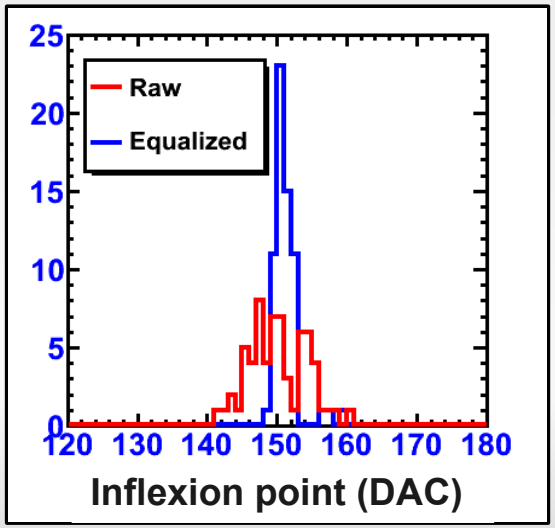
Board test (I)

- After mesh HV training, prior to assembling
  - Measure detector signal uniformity (10 % RMS var.)
  - Correct non-uniformity with individual preamplifier gains

- What was done
  - Preamplifier response measured with test charges
    → Gain correction reduces Scurve spread from 8 to 1 %
  - Detector response inside a gas test box
    Ideally with particle beam, ^{55}Fe quanta used
    Adjust chip parameters to detect the maximum of quanta

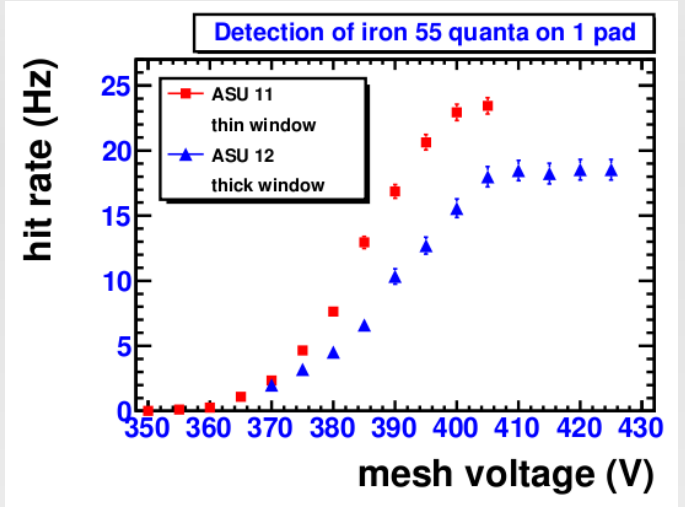


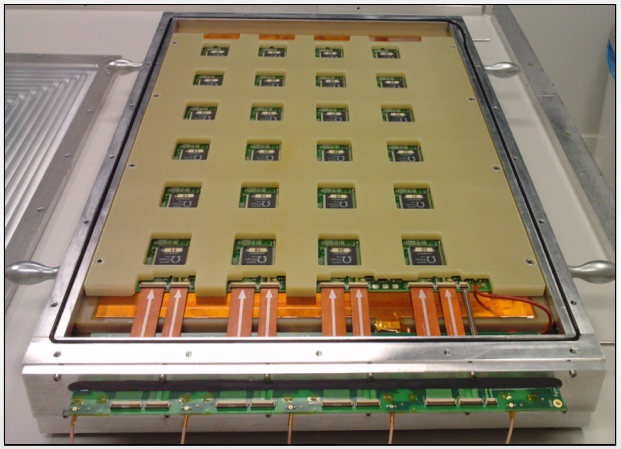


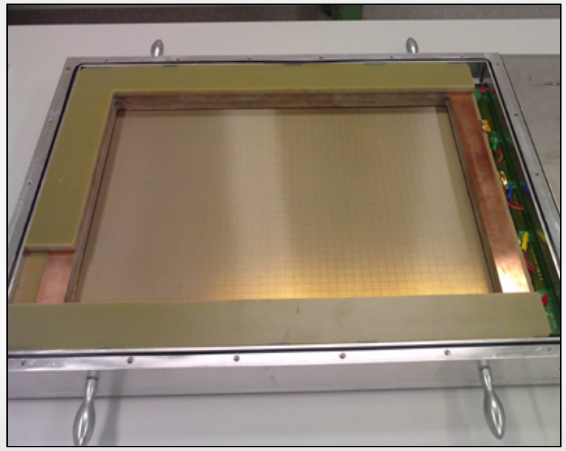


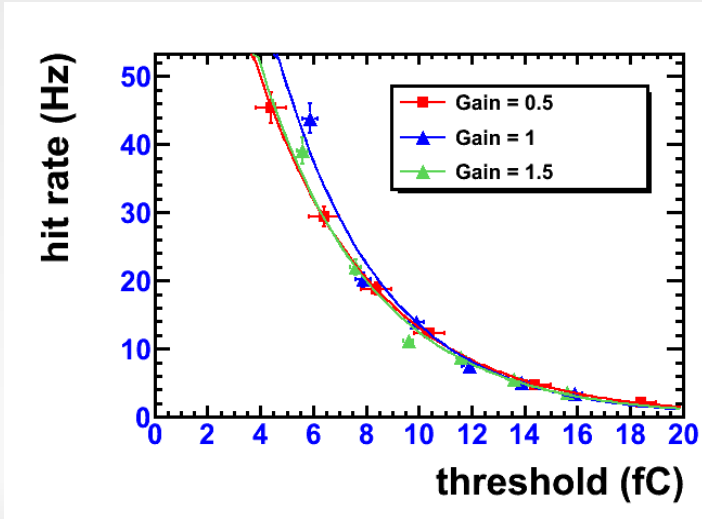
Board test (II)

- After mesh HV training, prior to assembling
  - Measure detector signal uniformity (10 % RMS var.)
  - Correct non-uniformity with individual preamplifier gains
- What was done
  - Preamplifier response measured with test charges
    → Gain correction reduces Scurve spread from 8 to 1 %
  - Detector response inside a gas test box
    Ideally with particle beam, ^{55}Fe quanta used
    Adjust chip parameters to detect the maximum of quanta



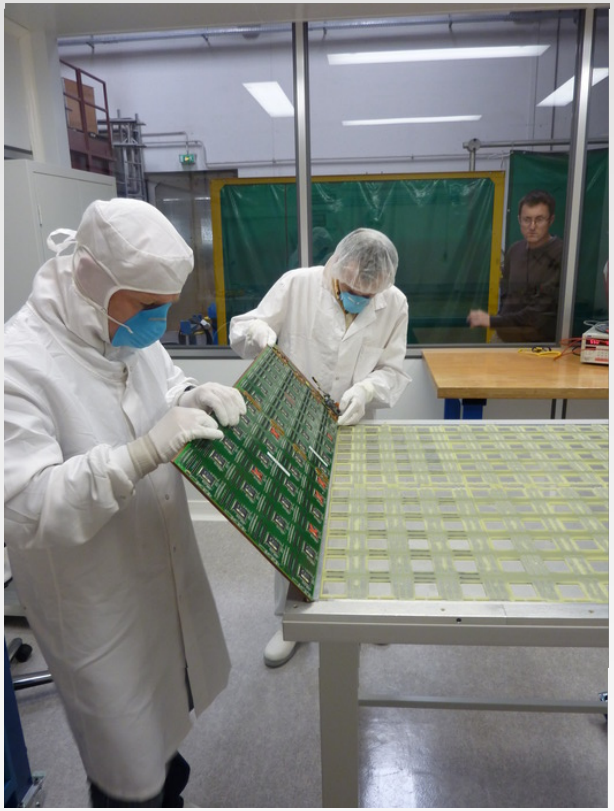


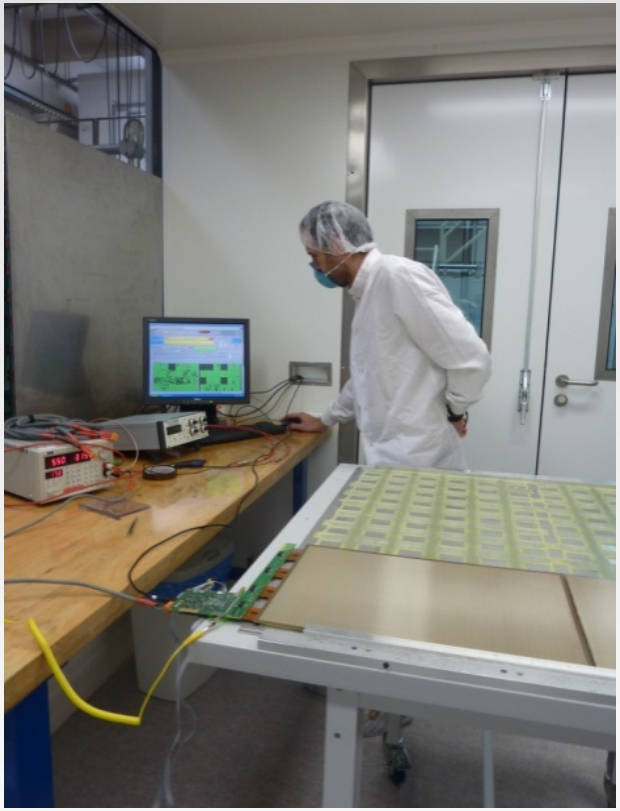




Assembly of the 1 m^2 prototype

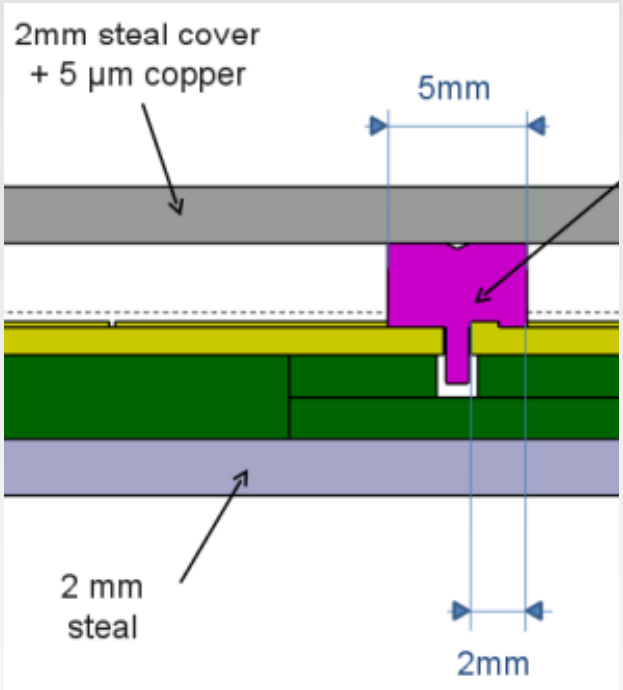
1. Gluing of ASU slabs on vetronite mask

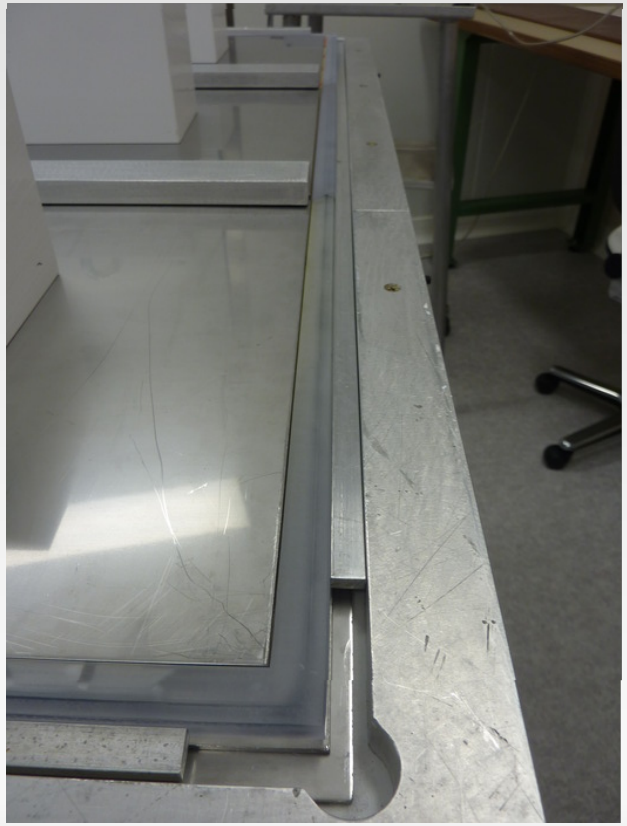




Assembly of the 1 m^2 prototype

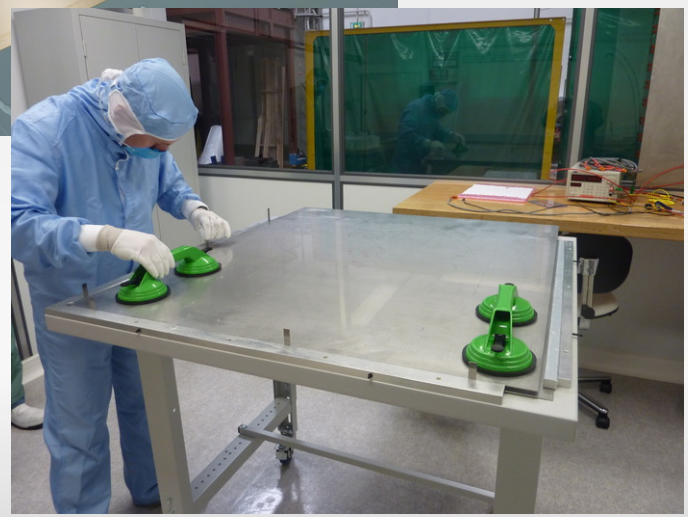
1. Gluing of ASU slabs on vetronite mask
2. Gluing of spacers and frame

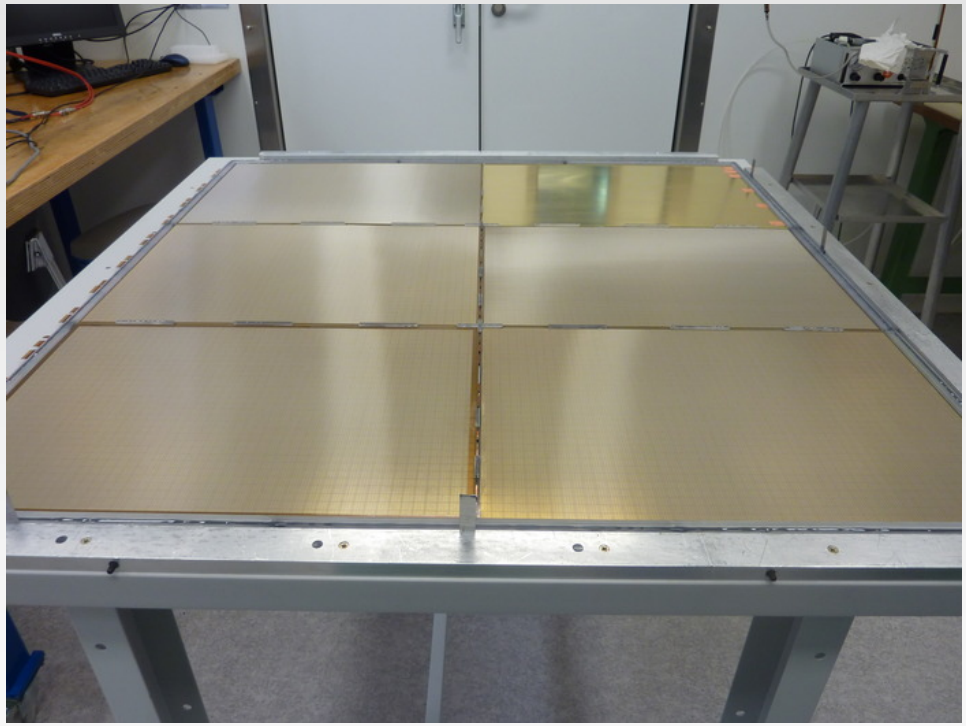




Assembly of the 1 m^2 prototype

1. Gluing of ASU slabs on vetronite mask
2. Gluing of spacers and frame
3. Gluing of cathode cover

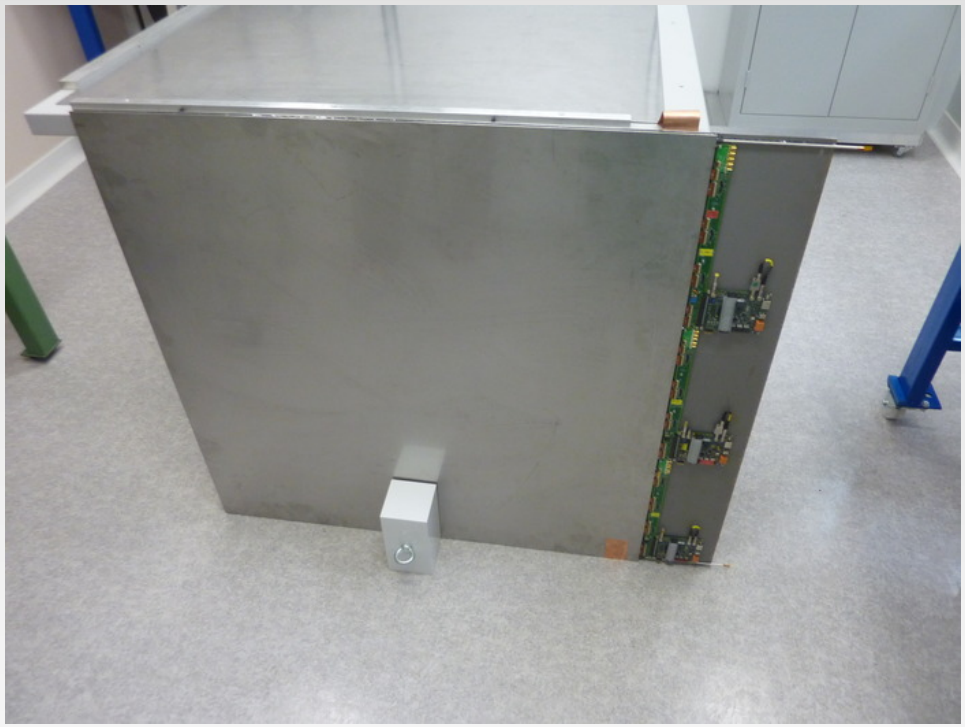


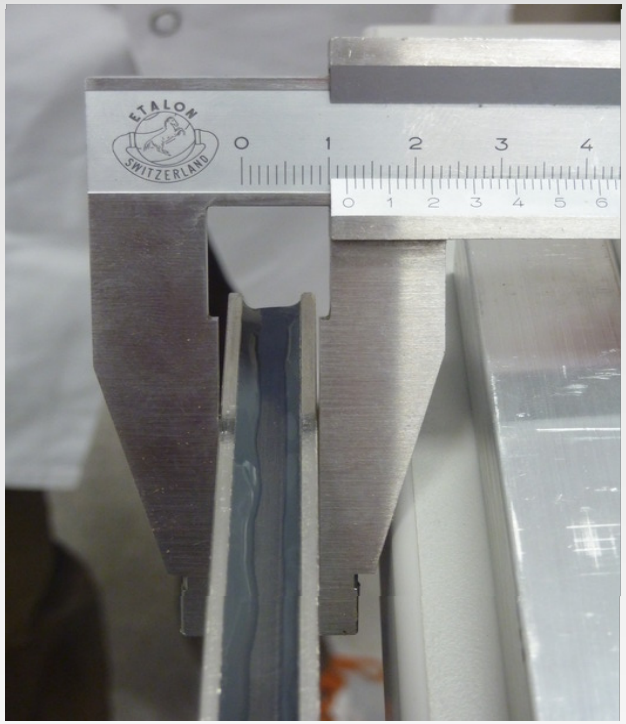


7680 pads!

Assembly of the 1 m^2 prototype

- After 1 week, the assembly is completed





Total thickness is 12 mm which includes 2+2 mm of steel (part of the absorber)
→ 8 mm effective thickness complies with ILC goal
(can be reduced to 7 mm by shrinking the mask from 3 to 2 mm)

Test beam - goals

- 4 weeks on SPS/H4
  - 10th / 24th June 2010, CALICE period
  - Until 8th of July 2010, RD51 period, shared beam
- TB program with 150 GeV/c low intensity muon beam
  - Test overall functionality
  - Reach high gas gain and lowest detection threshold on chips
  - Validate/rule out assembly and technical choices
  - Measure efficiency, multiplicity, uniformity
  - Compare performance with/without power-pulsing of chips

NB : The 1m^2 prototype efficiency will be low (Shaping time short w.r.t. Micromegas signals), nevertheless, several technological choices can be validated and unforeseen problems can be found and solved before the construction of the next prototype with an optimised electronics (MICROROC)

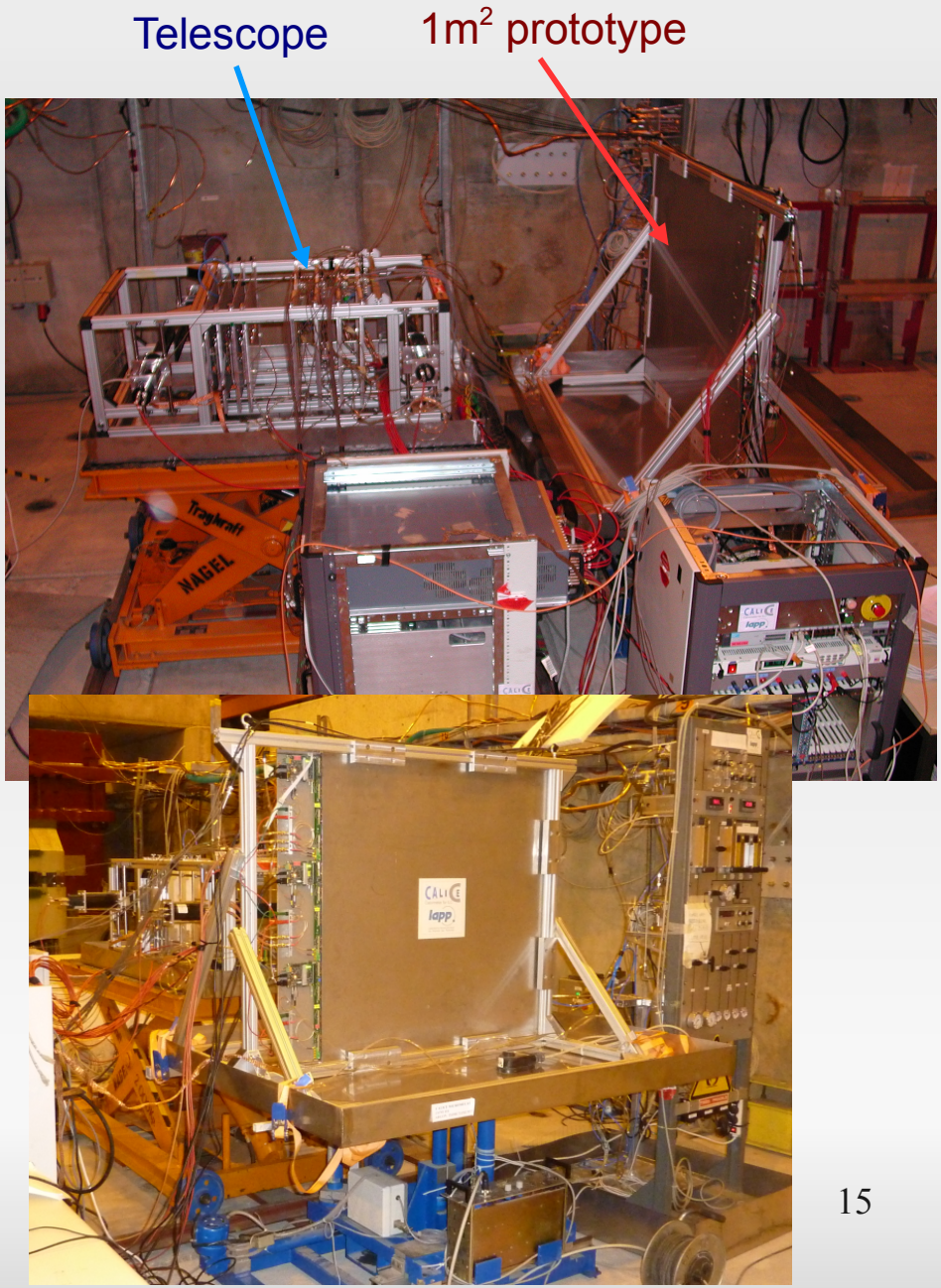
Test beam set-up

SPS/H4 beam
- 4 weeks in June/July 2010
- 150 GeV/c muons

Detectors
- 3 scintillators for triggering
- Telescope with 4 Gassiplex chambers
- 1m^2 chamber downstream of the telescope

DAQ
- CAEN ADC/sequencer VME module and LabView Centaure for telescope
- DIF (synchronized with CCC) and LabView program for 1 m^2 prototype
- Trigger obeys BUSY and READY signal logic → common event numbering for off-line reconstruction

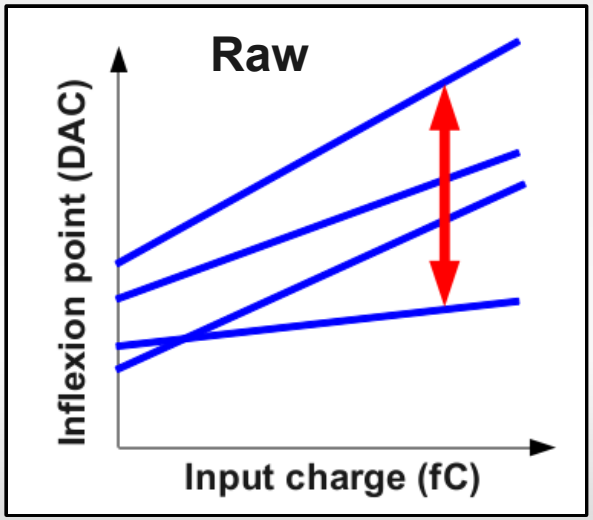
Rates
- Beam rate and scintillator trigger rate < 1kHz
- Acquisition rate ~ 100Hz

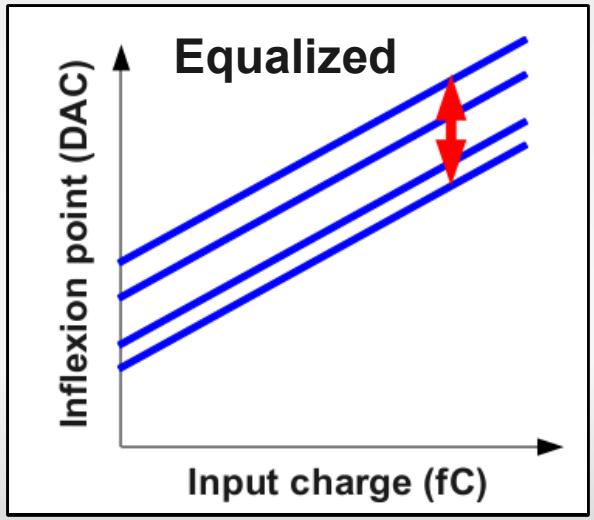


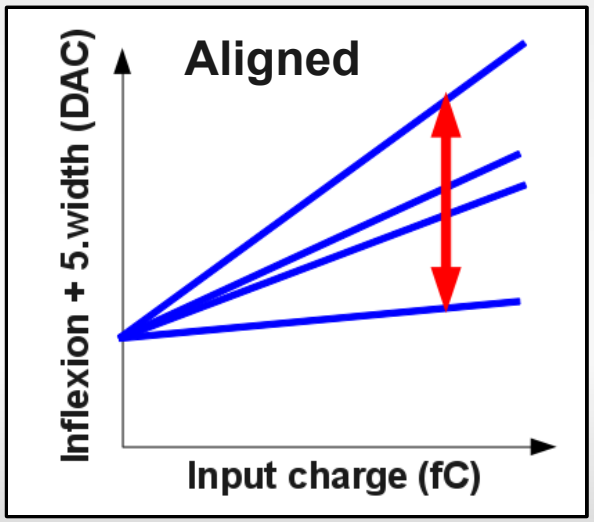
Chip settings

Chip parameters : Shaping time (per chip) set to max ~ 20 ns,
threshold (per chip) above noise limit, preamplifier gain (per channel)

1. Uniform response settings
   - Correct detector non-uniformity with preamplifier gains
   - Proved to work in laboratory
   - Threshold given by pedestal dispersion (~10 fC)
2. Low threshold settings (used during TB)
   - Align Scurve end-points using preamplifier gains
   - Increase gain dispersion but reduce thresholds







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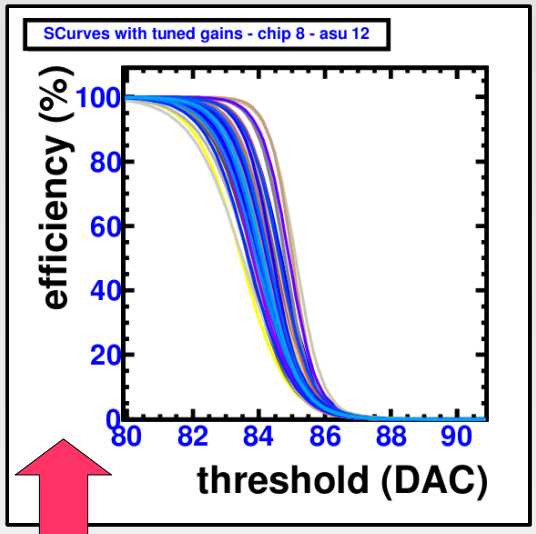
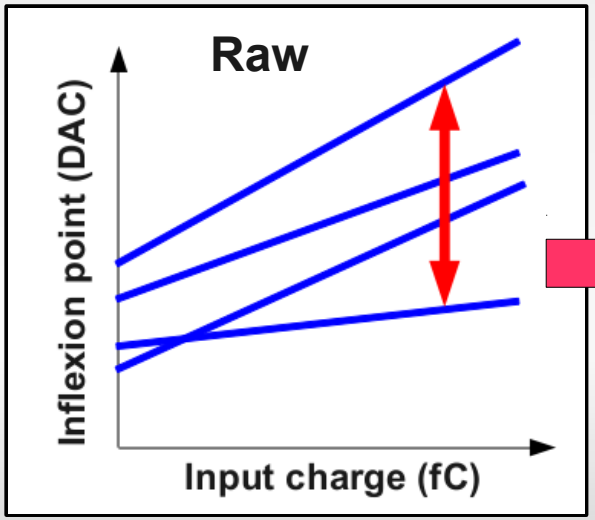
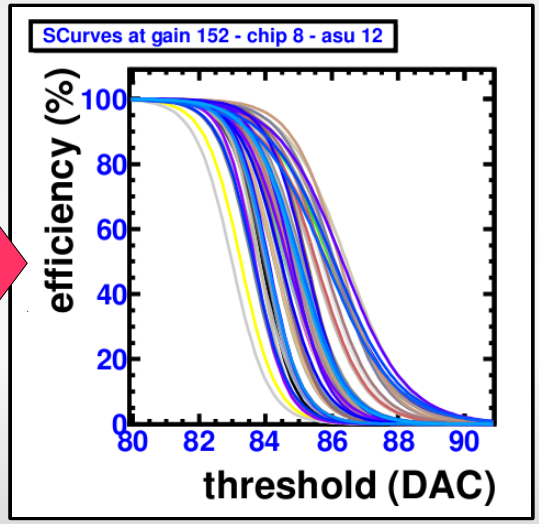
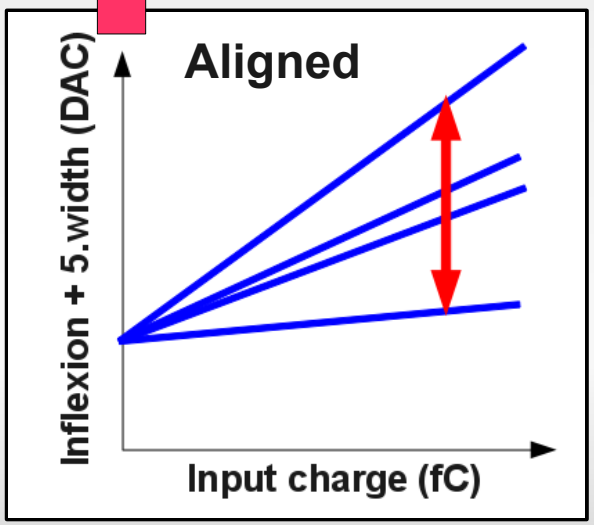


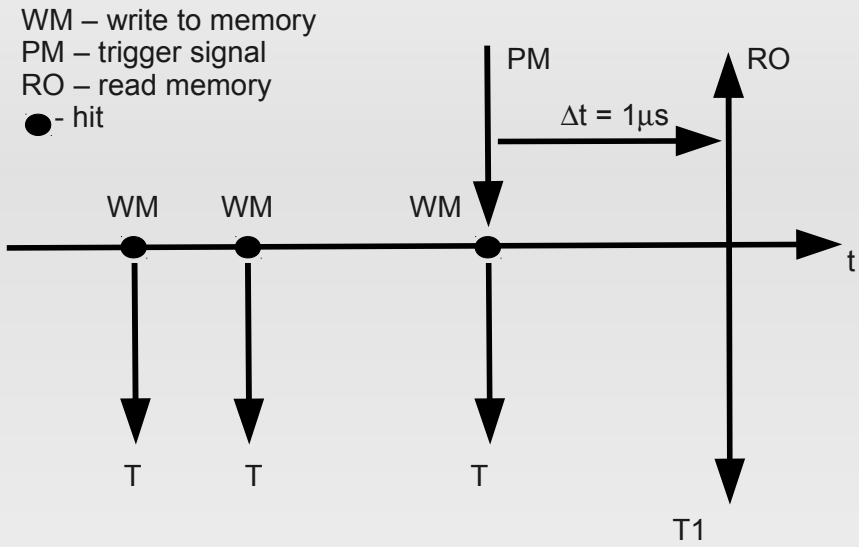


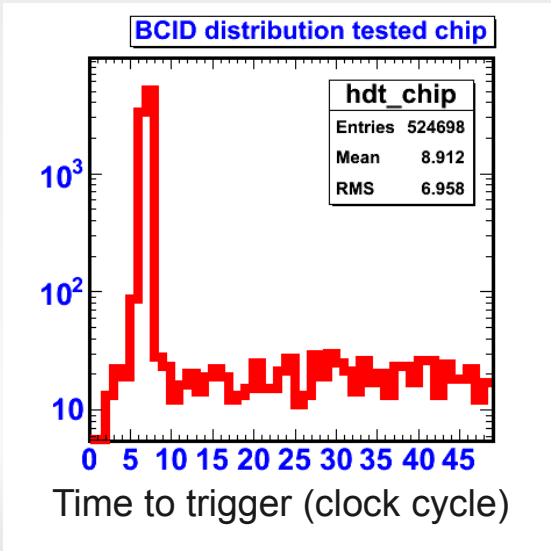




Time-stamping

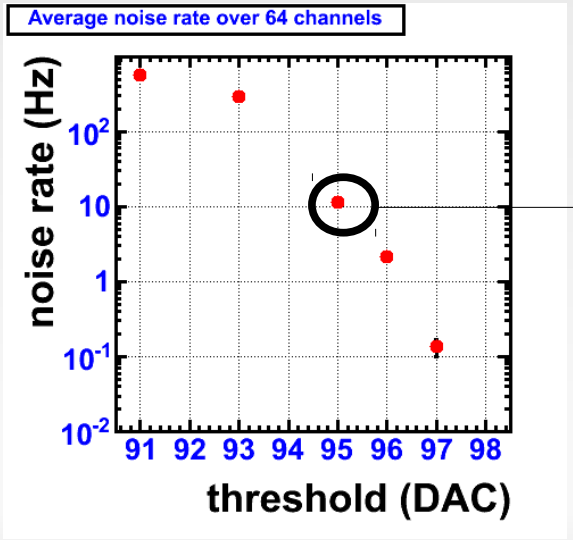
- Timing features
  - Time-stamping with 200 ns precision
  - Clock distributed to DIF by Clock Control Card
  - 127 event depth memory (reset above)
- Time-stamping
  - Time of hits T
  - Time of readout T1
    ~ time of trigger if READY state
- Signal selection
  - Use 2 TIMER modules
    → 1 μs delay between trigger and readout
  - Hits from triggering particles have
    T1 – T = 1 μs = 5 clock cycles

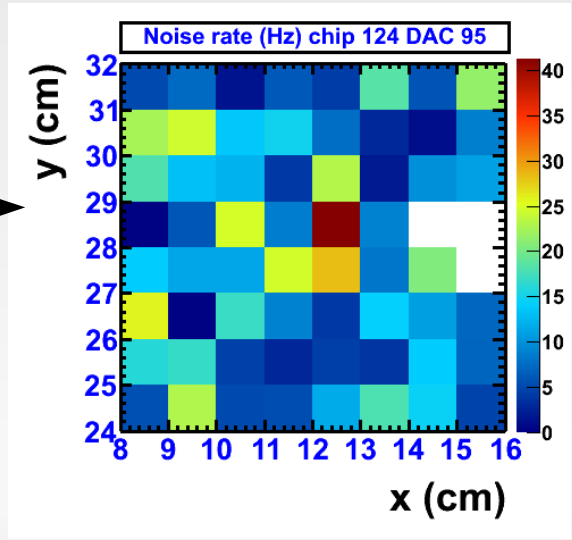


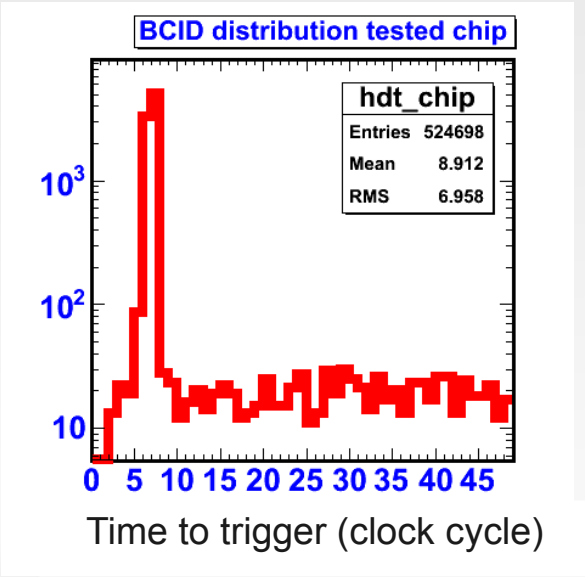


Noise rate

- Low threshold settings
  - Noise hits un-avoidable
- Typical rates per channel of tens of Hz
- After time cut, however, drops to negligible value
  - Chip S/N ratio > 100
  - Noise hit probability/chip < 1 % → tenths of Hz per channel << 500 Hz beam rate



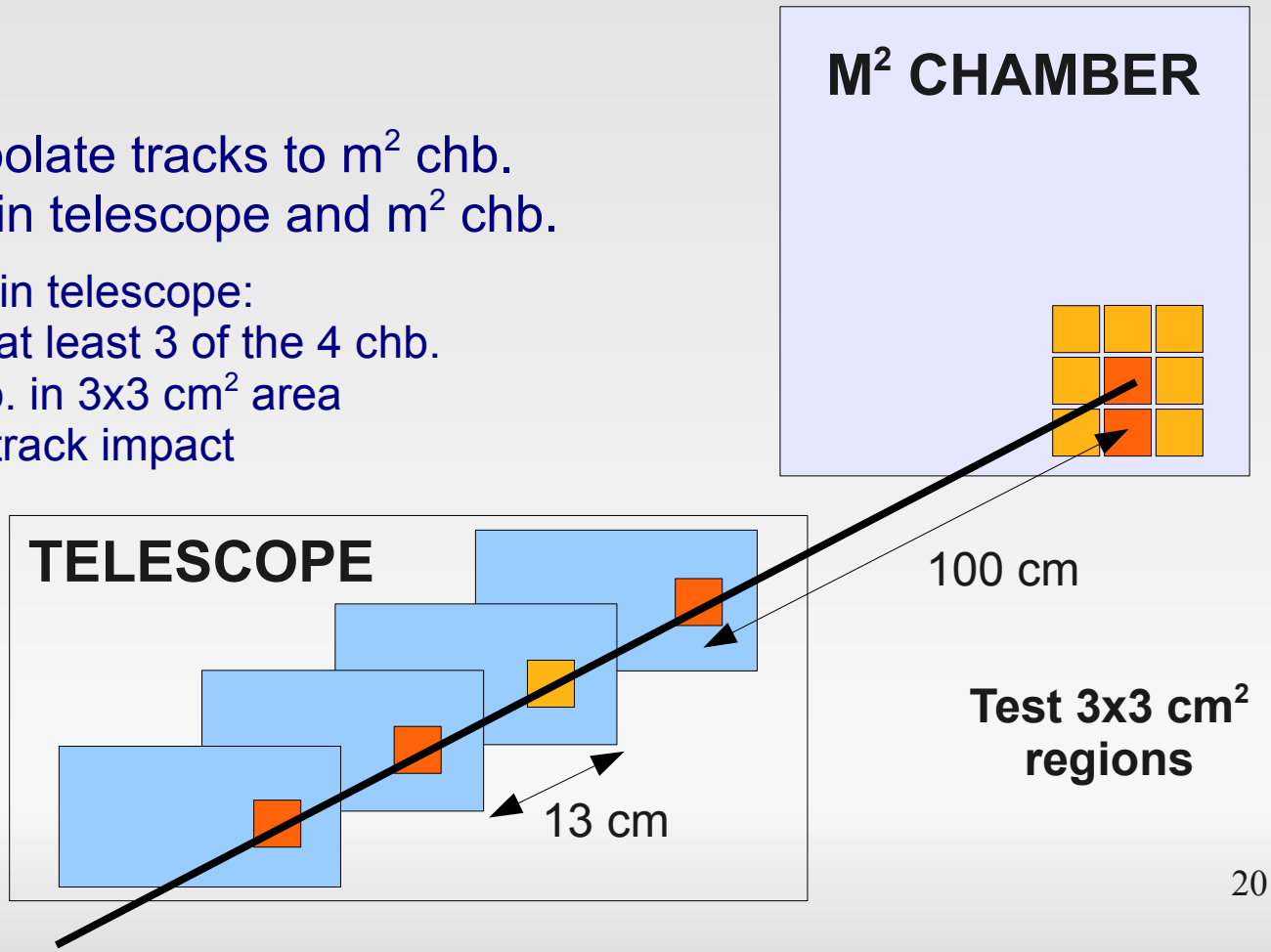




First results

- Runs @ 420 V to determine the maximum efficiency (given the shaping time issue)
- Runs @ 410 V to determine the efficiency/multiplicity values and uniformity

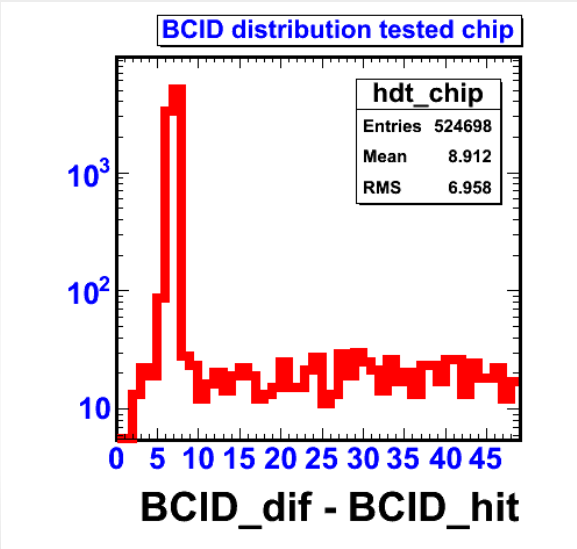
- Use telescope to extrapolate tracks to m^2 chb. Same pad size (1 cm^2) in telescope and m^2 chb.
  - → select straight tracks in telescope: single aligned hits in at least 3 of the 4 chb.
  - → look for hits in m^2 chb. in 3x3 cm^2 area around extrapolated track impact

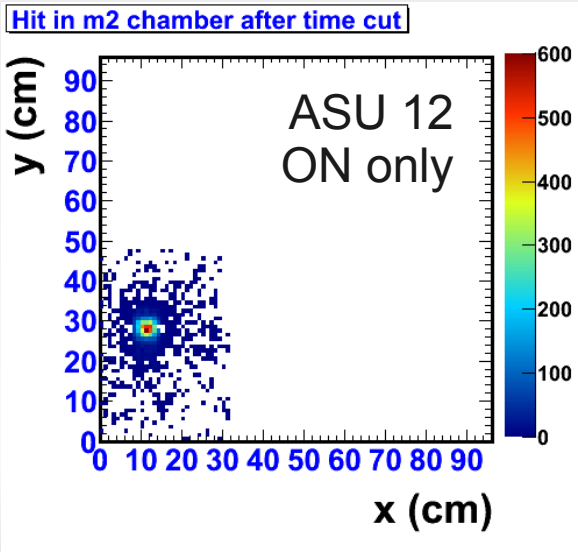


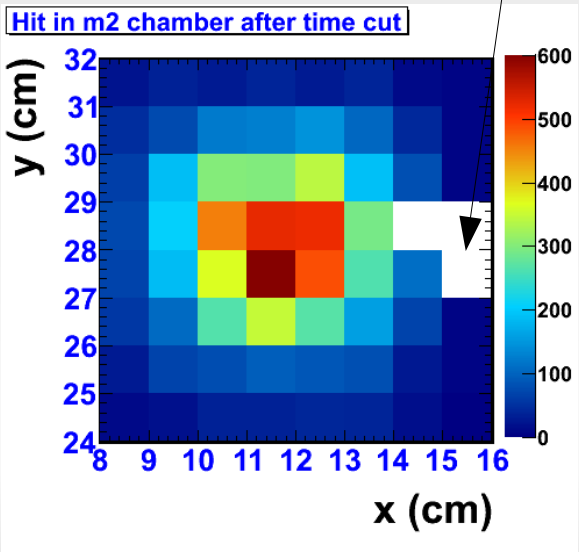
Runs @ 420 V

- Gas gain of 15000 → expected Landau MPV ~ 20 fC
  Remember: due to a too short shaping time, only 10 % of the signal is seen
  → effective signal MPV is 2 fC !

- Approx. 40000 triggers recorded
  - 200 Hz muon beam centered on 1 chip of ASU 12
- S/N ratio in time peak of 208 (3 noisy channels switched OFF)
  - Peak contamination after time cut < 0.5 % for the chip
  - Noise hit probability after time cut ~ 0.01 % per channel



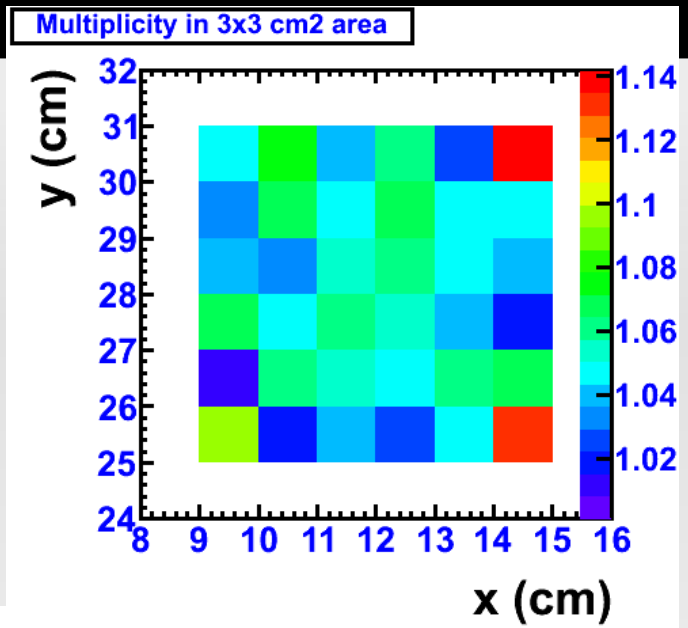


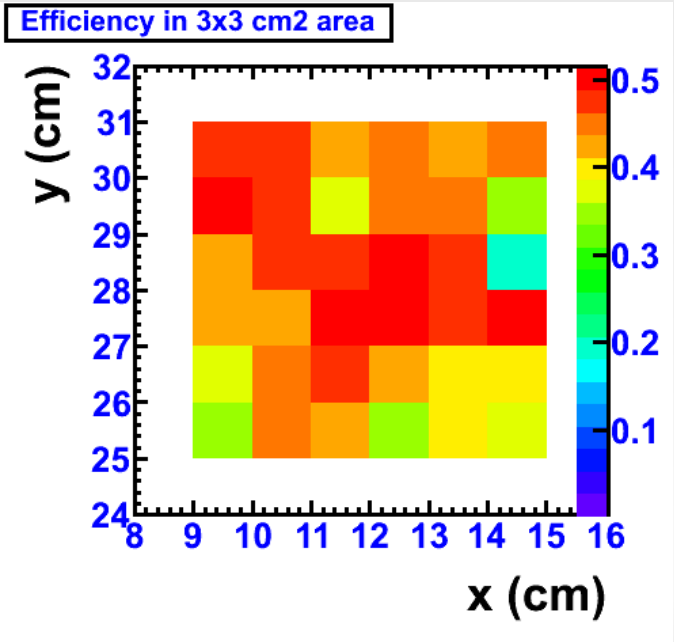


Runs @ 420 V

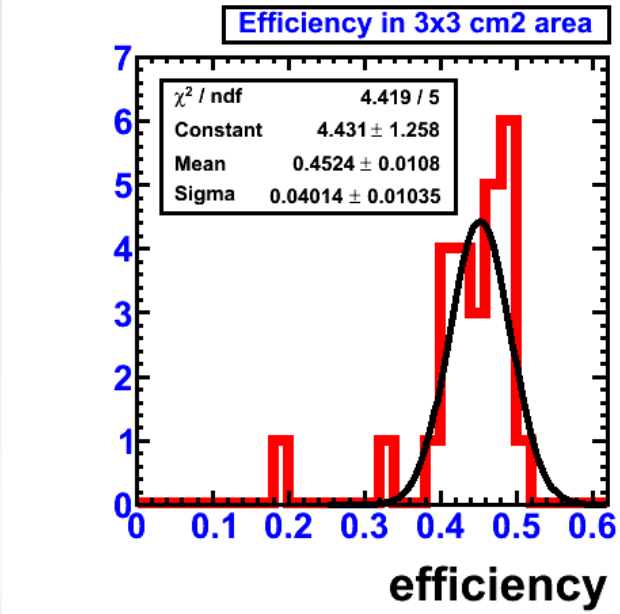
- Average efficiency of 45.2 +/- 4.1 %
  Remember: due to a too short shaping time,
  only 10 % of the signal is seen!
- Average multiplicity of 1.05 +/- 0.02
  Compatible with previous measurements with Gassiplex

  2009 JINST 4 P11023

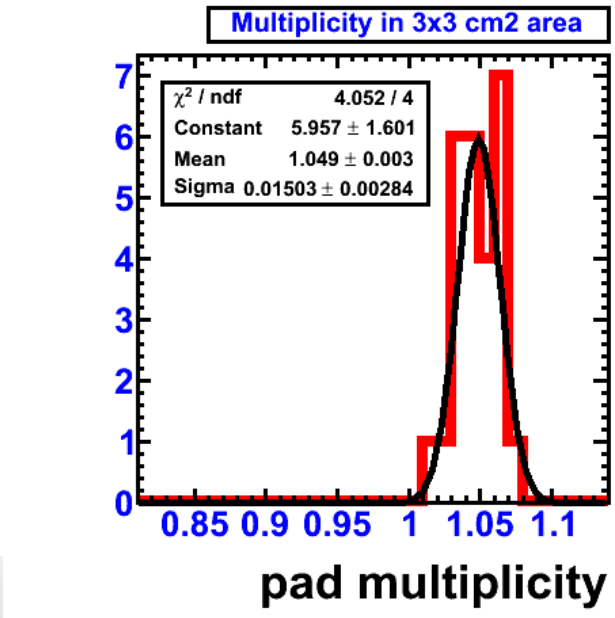




Efficiency error of each 3x3 pad area < 5 %

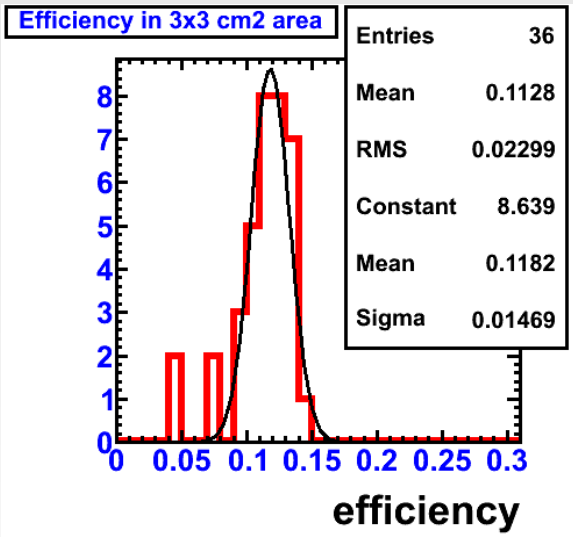


Efficiency error of each 3x3 pad area < 2.5 %

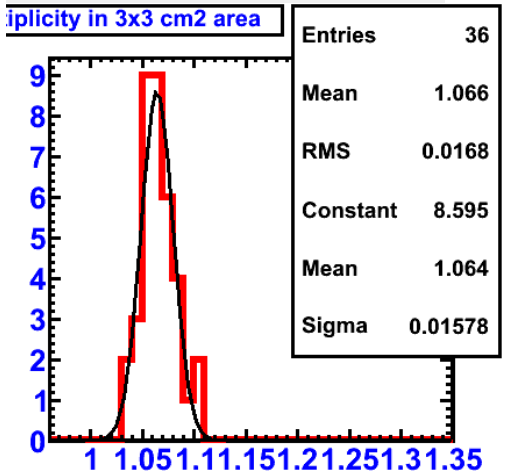


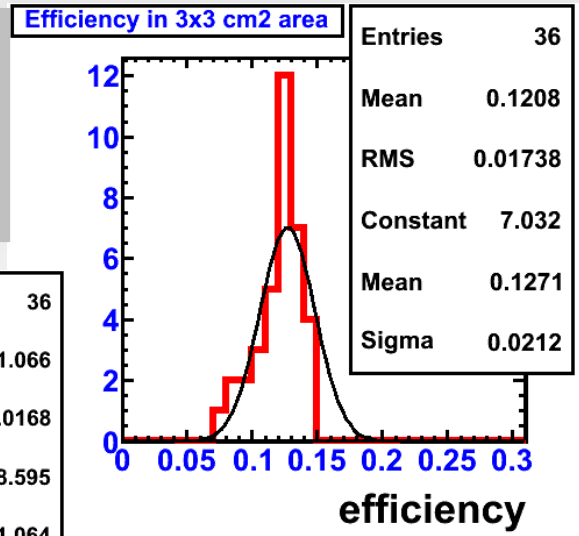
Runs @ 410 V

- Lower gas gain and higher threshold configurations → much lower efficiency
- Determine the uniformity of efficiency and multiplicity over the m^2 chamber area → beam directed at a few chips with 400000 triggers per chip
- First results on 2 chips indicate that the mean values and RMS remain the same
  - To be compared with results from different chips (on-going work)

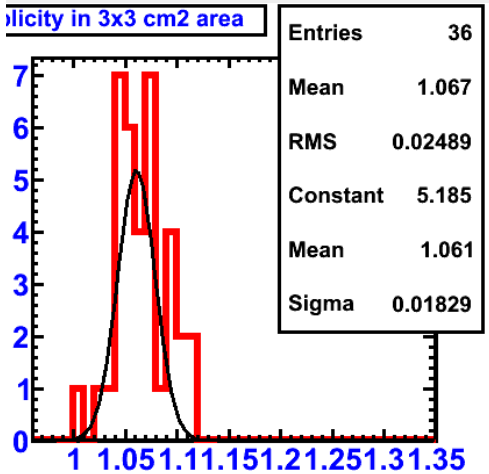


CHIP 124
Close to center
11.2 % +/- 1.5 %
1.07 +/- 0.02



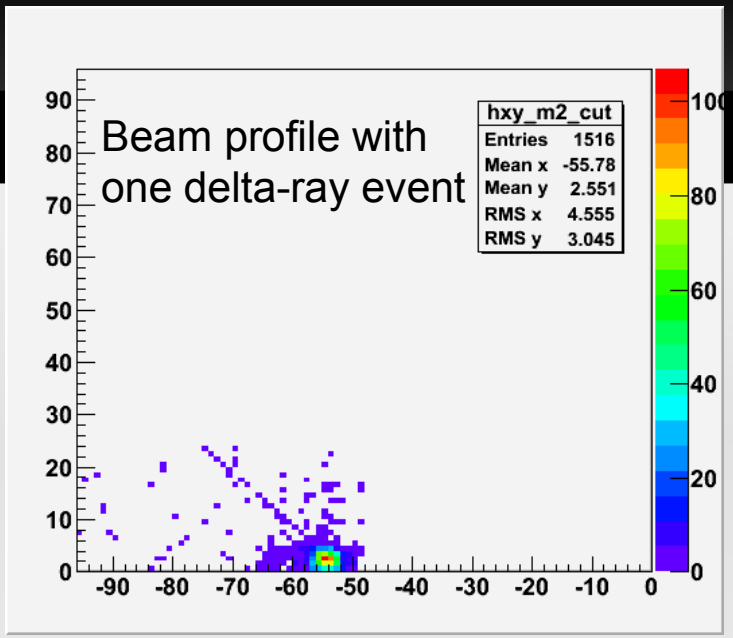


CHIP 114
Close to spacers
12.7 % +/- 1.6 %
1.07 +/- 0.02



Efficiency error of each 3x3 pad area < 1 %

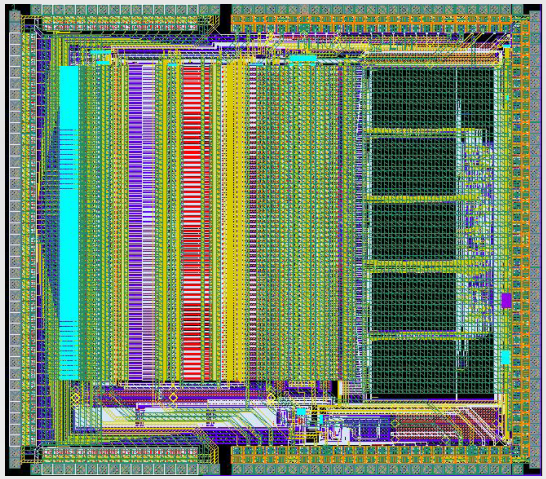
TB summary



- Mechanics
  - The 1 m^2 prototype is gas tight and robust
- Electronics
  - Successfull synchronization between telescope and 1 m^2 prototype DAQ
  - Preamp gain adjustment to lower thresholds works
  - Stable and reliable DAQ
- Detector
  - Very few mesh HV trips (limit @ 1 uA)
  - Gas gain up to 15000 reached (beam intensity kept below 1 kHz)
- Software
  - Reconstruction of simultaneous events from both DAQs realized
  - Data file book keeping under development for next test beam

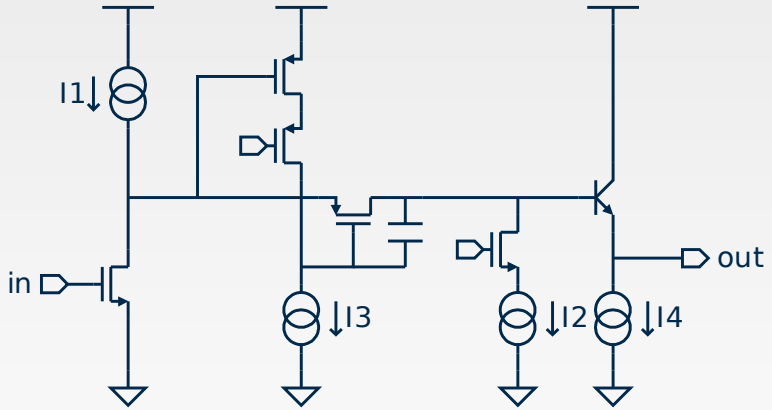
New front-end electronics

- Shaping time need to match the detector signals
  → modify analog part of the chip & keep same digital



- MICROROC
  - Collaboration between LAL/Omega and LAPP/LC
  - Pin to pin compatible with HR
    → very few developments on firmware, software, boards

- Features
  - Charge preamplifier
  - Shaping time of 30, 100, 150 or 200 ns
  - 3 thresholds with 10 bits resolution
  - 400 fC dynamic range
  - Noise RMS (Cdet of 80 pF) of 0.24 fC
    with 200 ns shaping time
  - Consumption for all chip of 6.9 mA (64 channels)

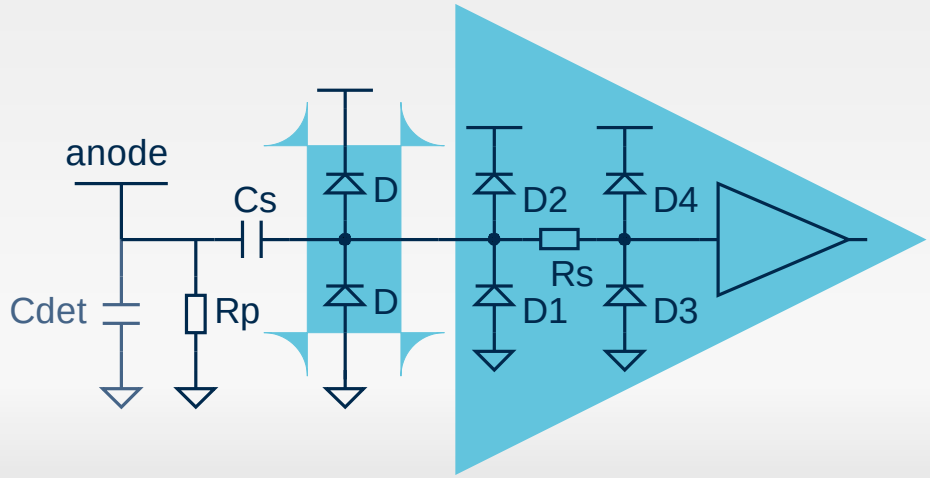


Spark protections

- Some experience gained on spark protection with diode networks
  - Network test setup @ LAPP
  - See presentation of R. Gaglione in WG2 session at previous collaboration meeting (Freiburg)

- MICROROC protections on board (as before) and on chip (new)
  - A serial decouping capacitor (Cs = 470 pF) and a diode network (BSV99 or NUP4114)
  - Two clamping diodes (D1 and D2), the parasitic serial resistor (Rs) and another diode network (D3 and D4)

Protection network :
Cdet=80pF
Rp=1MΩ
Cs=470pF
D=BAV99/NUP4114



Next steps

- Concerning our present 1 m^2 prototype equipped with HR2 chips
  - Finish TB data analysis
    - Mainly thresholds and P/T dependence of detector performance
  - Test behaviour in hadron showers
    - Join TB of AHCAL in 1 m^3 W-structure as last active layer
    - Start on October the 18th on T7 (muon run)
    - Move to T9 on November the 3rd (low energy hadron run)

- Next prototype with MICROROC
  - First chips recieved (25 over 365 produced), testing has just started
  - If all works, fabricate and equip 6 ASU with MICROROC
  - Expect our « first » 1 m^2 plane ready before mid-2011
  - And a few planes available before end-2011

- 2011 TB plans
  - Repeat 2010 TB campaign → efficiency/multiplicity, behaviour in showers + spark rate
  - Within CALICE and RD51 → would like to use RD51 telescope

Conclusion

- Small size Micromegas chambers show very good performance
  and are well suited for an HCAL
  Maintaining these performance when scaling up the detector size is challenging
  - Mechanics, electronics, gas distribution, HV stability, DAQ

- First attempt is satisfactory
  - Front-end chip short shaping time brings the efficiency down BUT
  - No true road blocks, detector operated up to high a gas gain
  - Several technical choises validated
  - Potential improvements for next prototypes found

- Second attempt with new font-end ASIC (MICROROC)
  - Longer shaping time essential to a very good efficiency, first chips are in hands
  - Aim at producing and testing a few prototypes in 2011