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DAQ-ROC4Sens Update

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The purpose of the proposed acquisition system is to provide a all-in-one solution that be able to capture and process the data generated for up to 4 Roc4Sens readout chips simultaneously. In order to achieve this goal, the system is composed of a FPGA Zynq Ultrascale+, a custom PCB and a management software. Thus, the operator will be able to manage the entire acquisition system from the GUI provided by the developed software, reducing the deployment time of the experiment and minimizing risks using a proven platform.
The FPGA chosen is a Xilinx Zynq UltraScale+ (model XCZU3EG-1SFVA625) that implements a processing system (PS) and a programmable logic (PL). Thus, this architecture makes integrate the acquisition as well as process the experiment possible to data on the same device. The PS is composed of a quad-core ARM Cortex A53, a dual-core ARM Cortex RSF and several peripherals to manage external devices such as NAND flash memories, CAN transceivers, or PCIe connections. This block will be in charge of running the operating system (a custom build based on GNU/Linux) that will execute the manage and control processes. The dual-core ARM will be destinated to run those algorithms in real time, taking advantage of the fact that it can read and write data directly from the programmable logic.
In relation to the PL, this part of the FPGA will implement the digital logic to communicate with the Roc4Sens chips in order to extract and store the relevant information in dynamic memory. Subsequently, this data will be collected and processed by the acquisition software.
The last block corresponds to the acquisition software, which will be the interface between the operator of the telescope and the proposed data acquisition system. It will be based on a client-server arquitecture. This program must meet the following requirements:
• GUI to set the different reference voltages
• Represent the data acquired from each Roc4Sens
• Execute commands directly on the operating system
Lastly, it should be noted that the proposed acquisition system is in an advanced design stage. Specifically, the logical design is in a debugging stage to ensure that every module works properly. Additionally, the custom PCB is under testing to validate its performance. Finally, the acquisition software is under developing, defining a proper API that can be easily integrated with other acquisition frameworks.

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