Radiation hardness and development of a large electrode DMAPS design in a 150 nm CMOS process.

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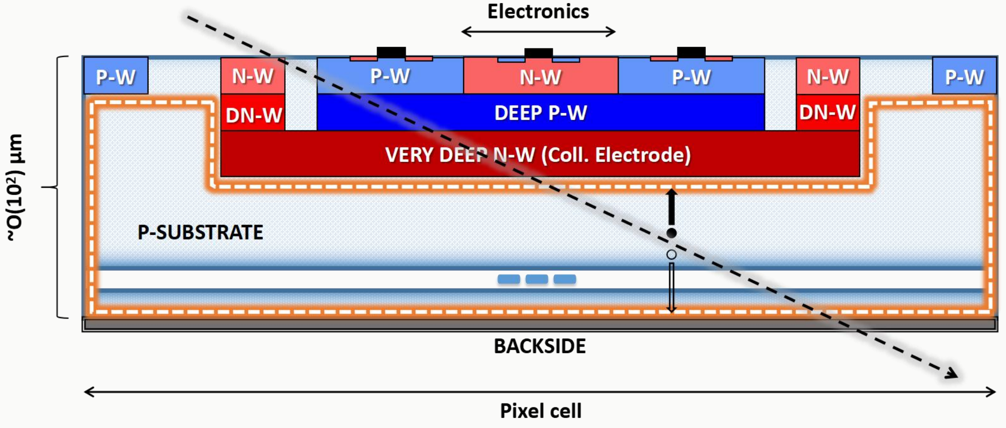
DEPLETED MONOLITHIC ACTIVE PIXEL SENSORS (DMAPS)

Commercial CMOS process (multiple wells for shielding), no hybridization, considerable depleted regions in highly resistive substrates, fast charge collection by drift.

"Large Electrode" design

Large collecting well containing all the in-pixel R/O electronics

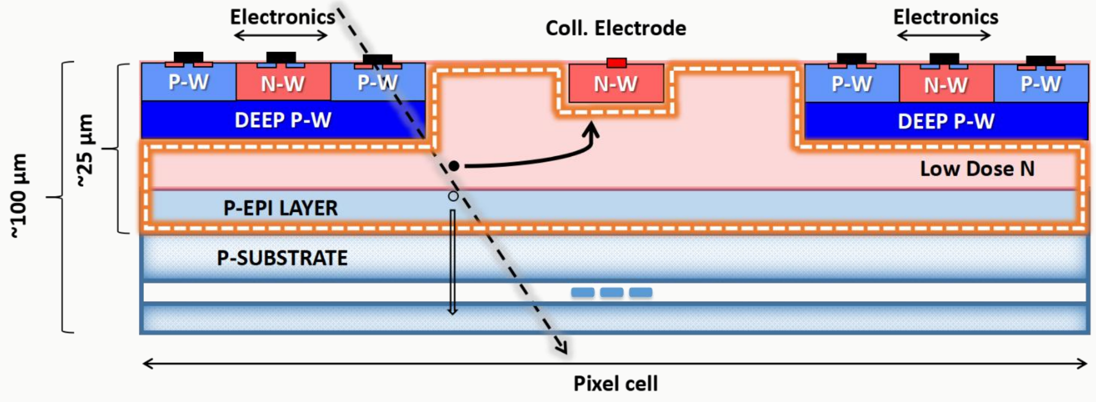


PROS: Short drift distances, strong E-field (Rad-hard).
CONS: Large sensor capacitance, high analog power.

---> Requires design efforts to optimize timing and minimize cross-coupling into the collection node.

"Small Electrode" design

Small collecting well outside the in-pixel R/O electronics



PROS: Small sensor capacitance, low power and noise.
CONS: Weak electrical field compromises rad-hardness.

---> Requires process modifications and small pixel pitch to optimize charge collection.

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BONN

DMAPS FOR HIGH ENERGY COLLIDER EXPERIMENTS

Requirements of future HEP experiments:

	ITk Outer Layer	BELLE 2 Upgrade
Occupancy	1 MHz/mm²	1.5 MHz/mm²
Time Res.	25 ns	O(100) ns
NIEL	10^{15} n_{eq}/cm^2	10^{14} n_{eq}/cm^2
TID	80 Mrad	100 Mrad
Area	O(10m²)	O(3m²)

DMAPS would offer:

- Reduced material budget compared to hybrids.
- Cheaper and less complex module production.

The Monopix DMAPS developments

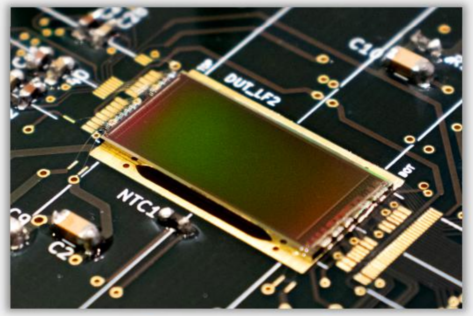
Column-Drain ("FE-I3 like") synchronous R/O architecture and fast front-end implementations

+

Design optimization to preserve charge collection after irradiation

LF-Monopix:

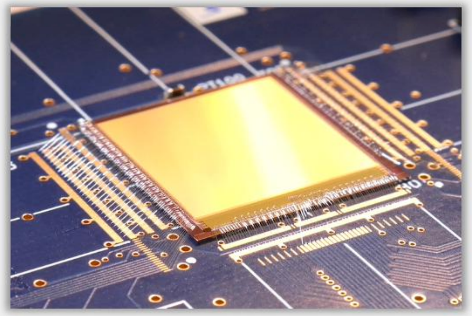
Large electrode DMAPS in LFoundry 150 nm CMOS



(This talk)

TJ-Monopix:

Small electrode DMAPS in Tower 180 nm CMOS



(Next talk by C. Bespin)

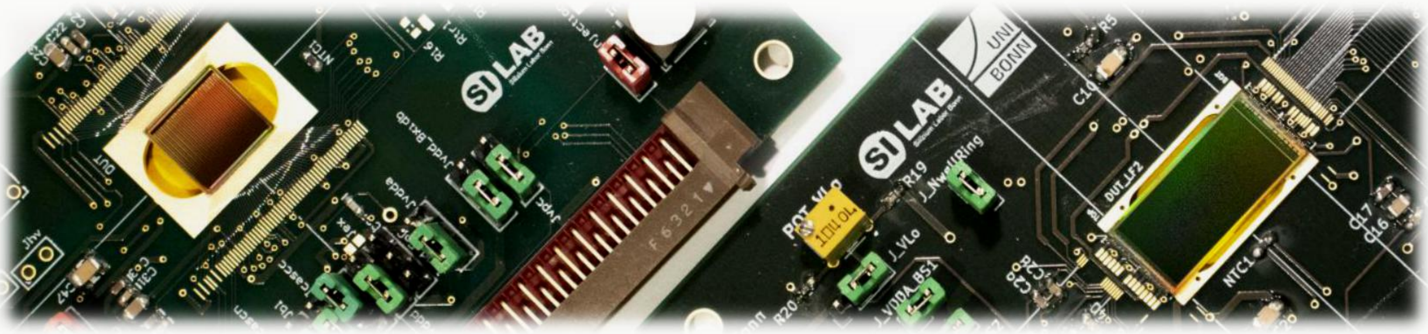
THE LF-MONOPIX PROTOTYPES

- Full-size (~cm²) large electrode DMAPS.
- Functional column-drain R/O architecture.
- In-pixel electronics in >2 kOhm-cm resistive substrates.

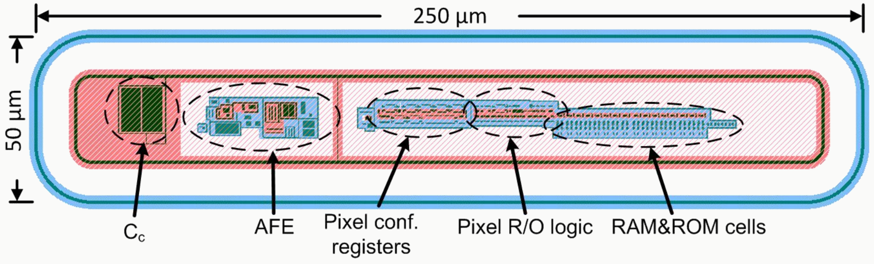
LF-Monopix1
(Mar 2017)

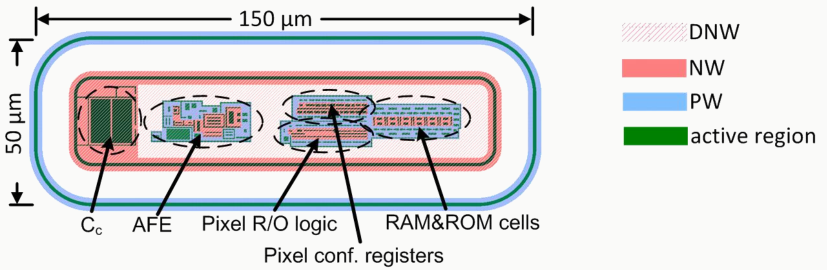
LF-Monopix2
(Feb 2021)

LFoundry 150 nm CMOS process



Pixel layouts (Top view):





DAQ system: Bonn's Multi-I/O 3 ("MIO3") and General Purpose Analog Card ("GPAC")

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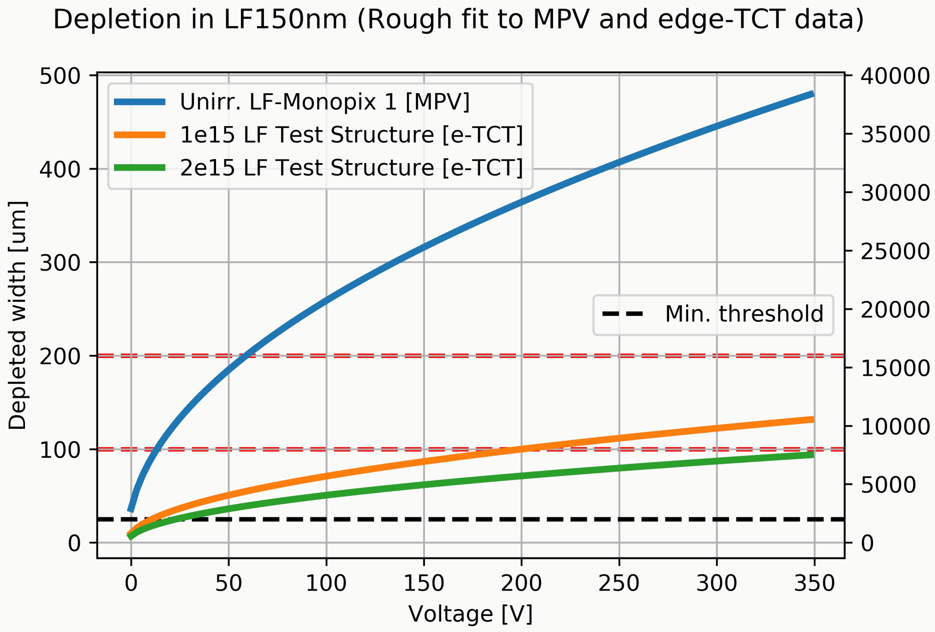
DEPLETION IN LFOUNDRY HR-SUBSTRATES

CMOS DMAPS aim to deplete the silicon bulk and collect charge <u>mainly by drift</u>

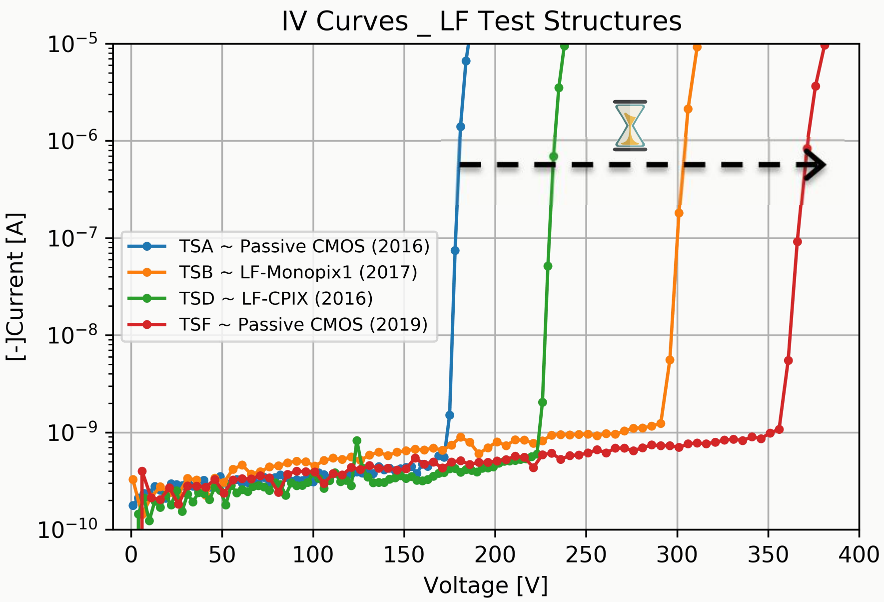
In order to do so, the **LF-Monopix** chips use:

- **A highly resistive substrate:**
  ~7 kOhm-cm, Czochralski processed

- **Large reverse bias voltages:**
  Improved across LF150 prototypes



(e-TcT data from: I. Mandic, L. Vigani.)



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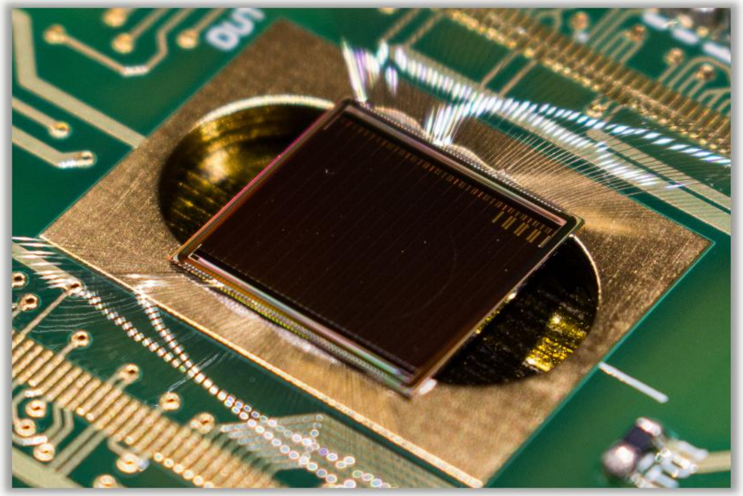
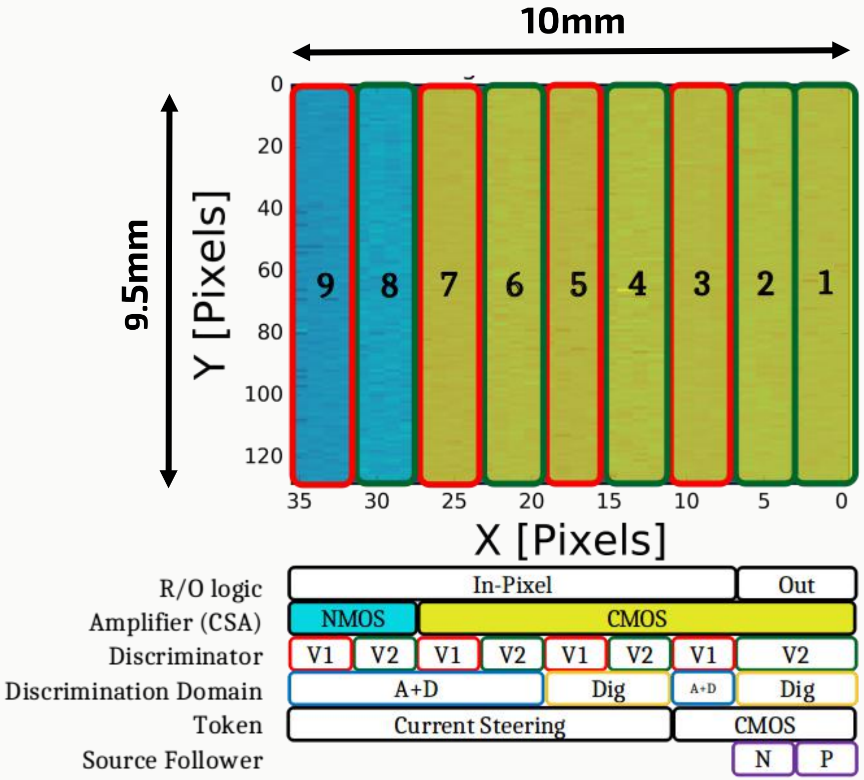
LF-MONOPIX1



- Functional **in-pixel** R/O logic.
- Large **50 x 250 µm²** pixel array (**129 rows x 36 cols**)
- Bunch-crossing clock frequency (**40MHz clock**)
- 40 MHz/160MHz CMOS or LVDS serial output.
- Timestamping: **8-bit LE/TE (ToT) @ 25 ns.**
- Power: **55 µW/pixel (~1.7W/cm²)**

Noise: ~150-200e- **Tuned Thr:** ~1600 ± 100e-

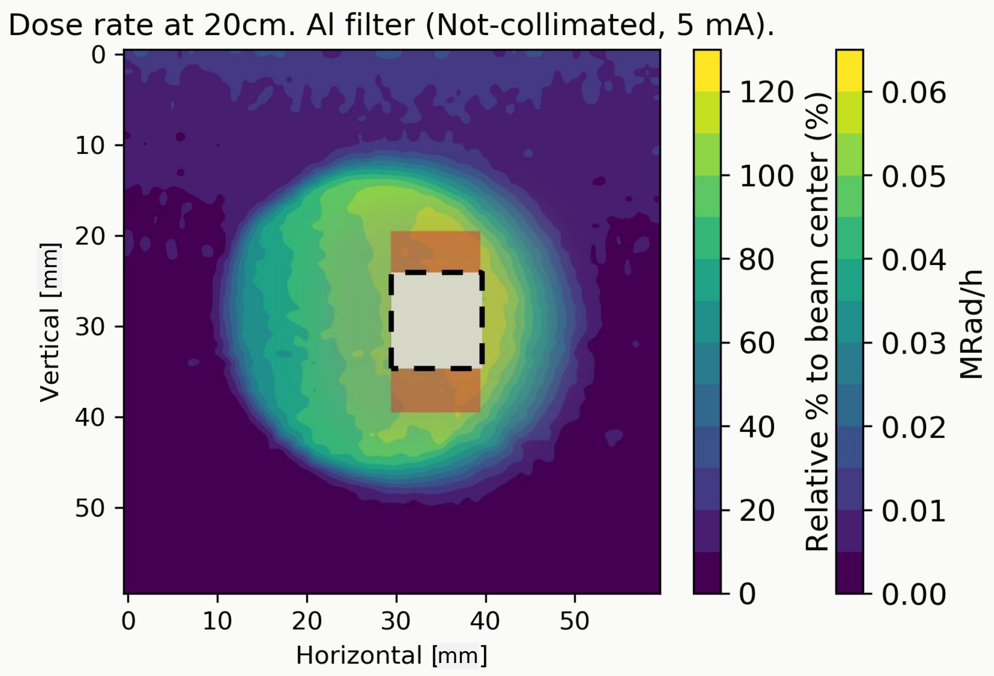


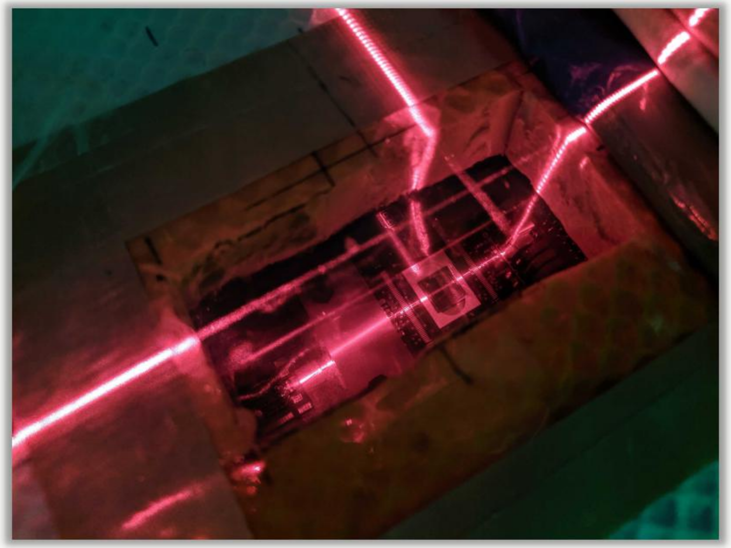
Radiation-hardness and sensor layout optimized in previous prototypes ☑

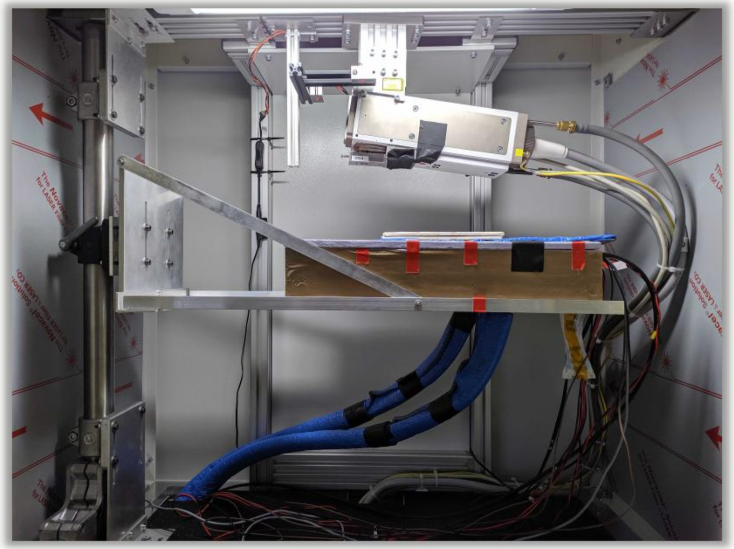
Succesful design efforts for **cross-talk mitigation** in digital lines ☑

Fast and low-power CSA and discriminator implementations ☑

TID IRRADIATION @ SILAB BONN







- **Sample:** 100 um thick LF-Monopix1 (Powered on)
- **X-ray tube settings:** 40 kV, 50 mA ---> 0.6 MRad/h
- **Temperature:** Cooled down with chiller through plate. 0±2 C in NTC
- **15 steps up to 100 MRad**

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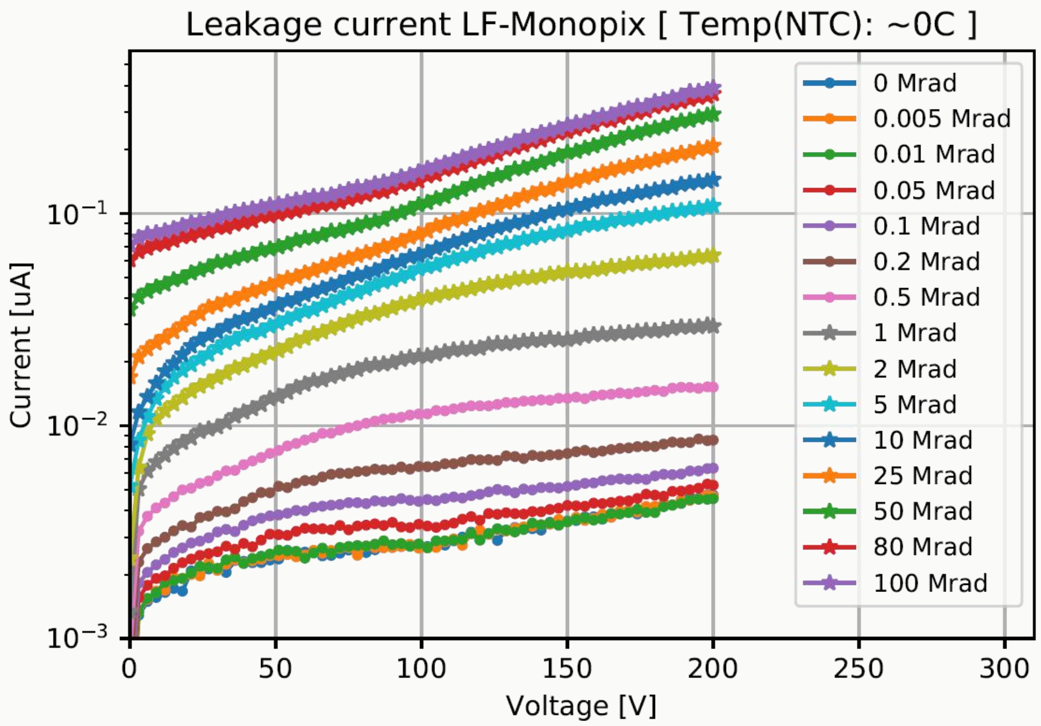
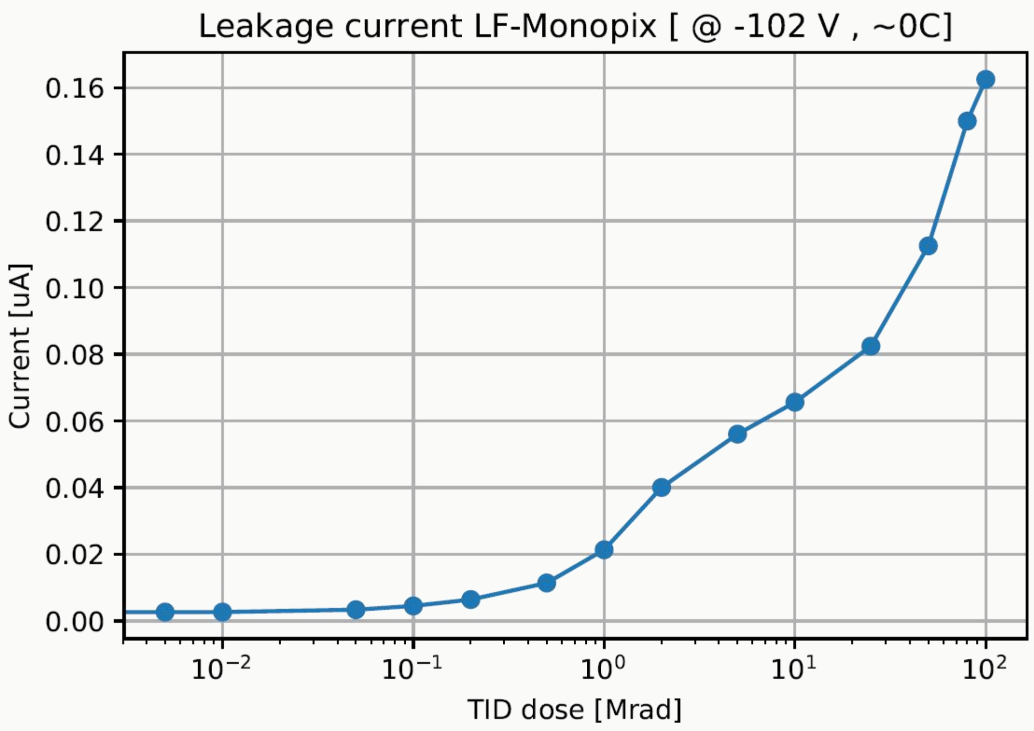
TID IRRADIATION: LEAKAGE CURRENT

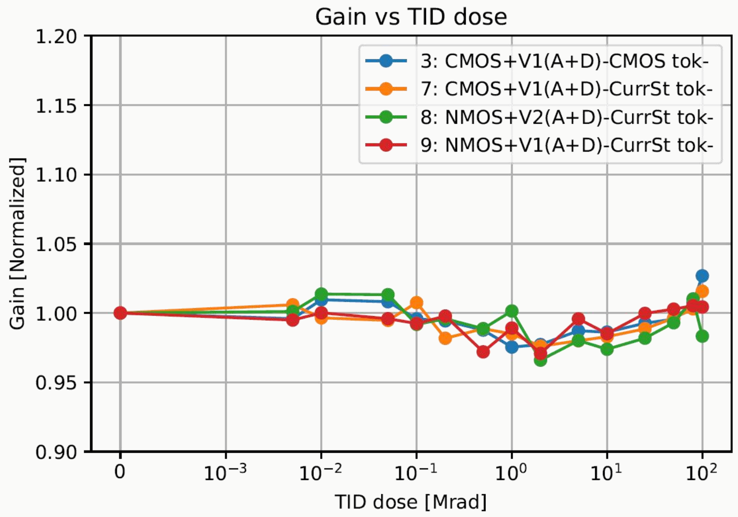




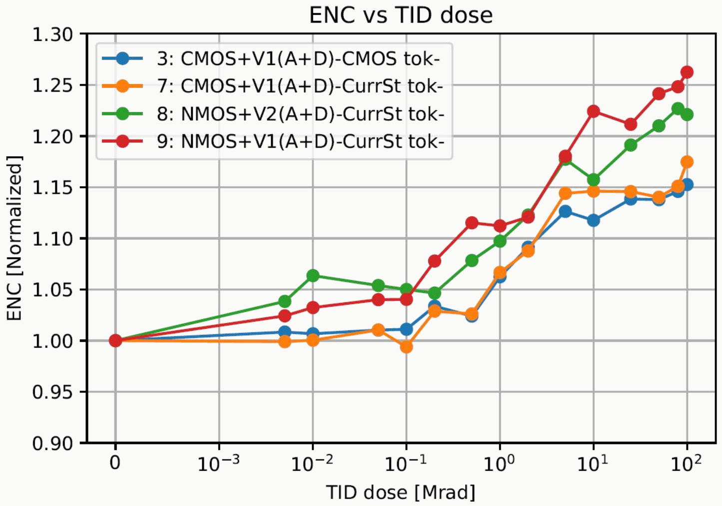
Increase of 2 orders of magnitude after 100 Mrad at 0 ± 2C temperature

TID IRRADIATION: GAIN & ENC

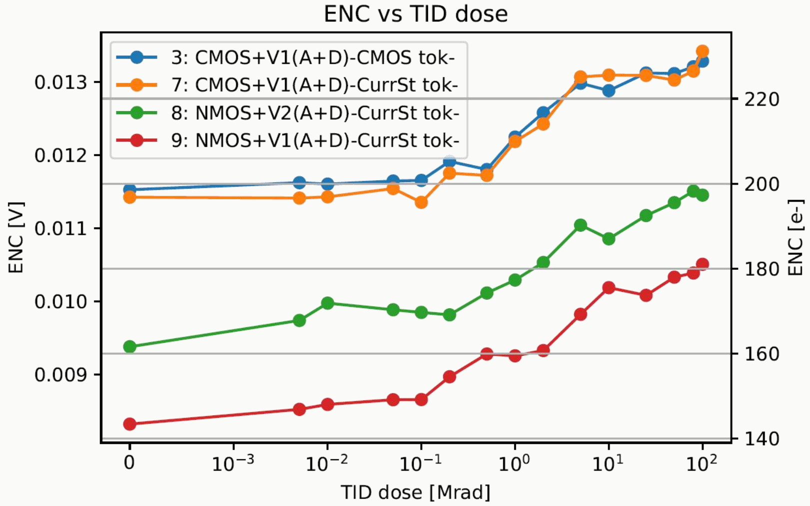
- **Relative Gain variation:** <3%



- **Relative ENC increase:** NMOS (25%) > CMOS (15%)



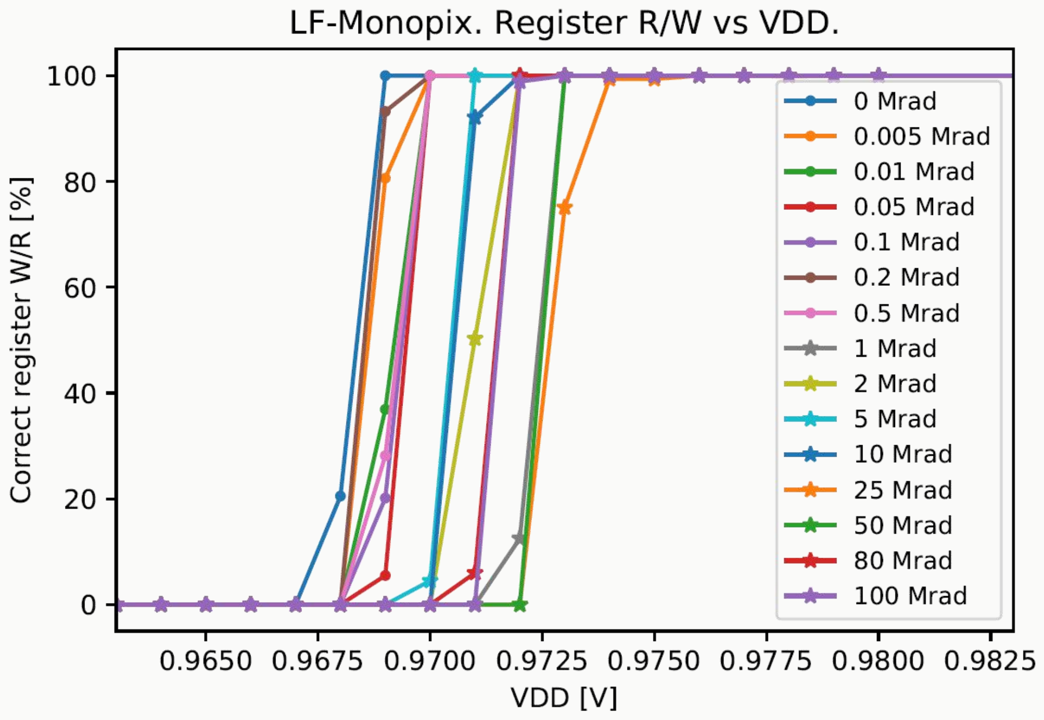
- **Nominal ENC:** CMOS > NMOS



TID: DIGITAL PERFORMANCE

- **Shift register R/W:**

Variation < 0.5% in whole matrix



No degradation of digital performance.

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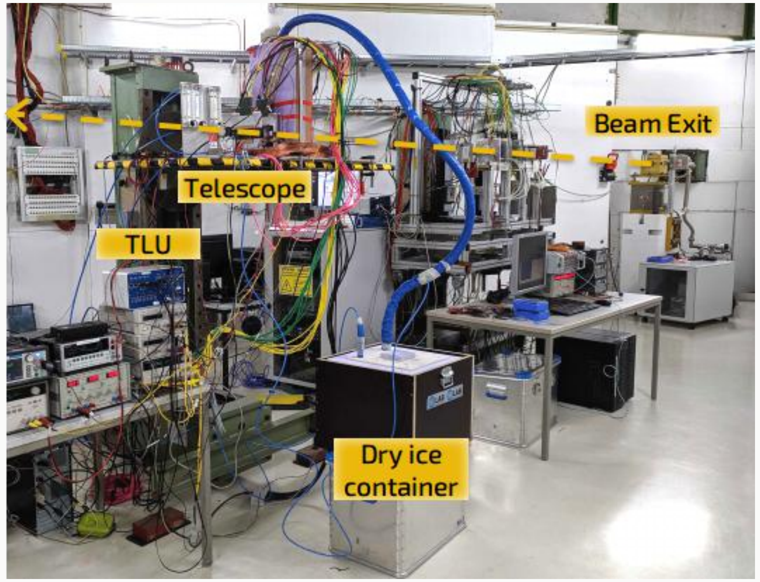
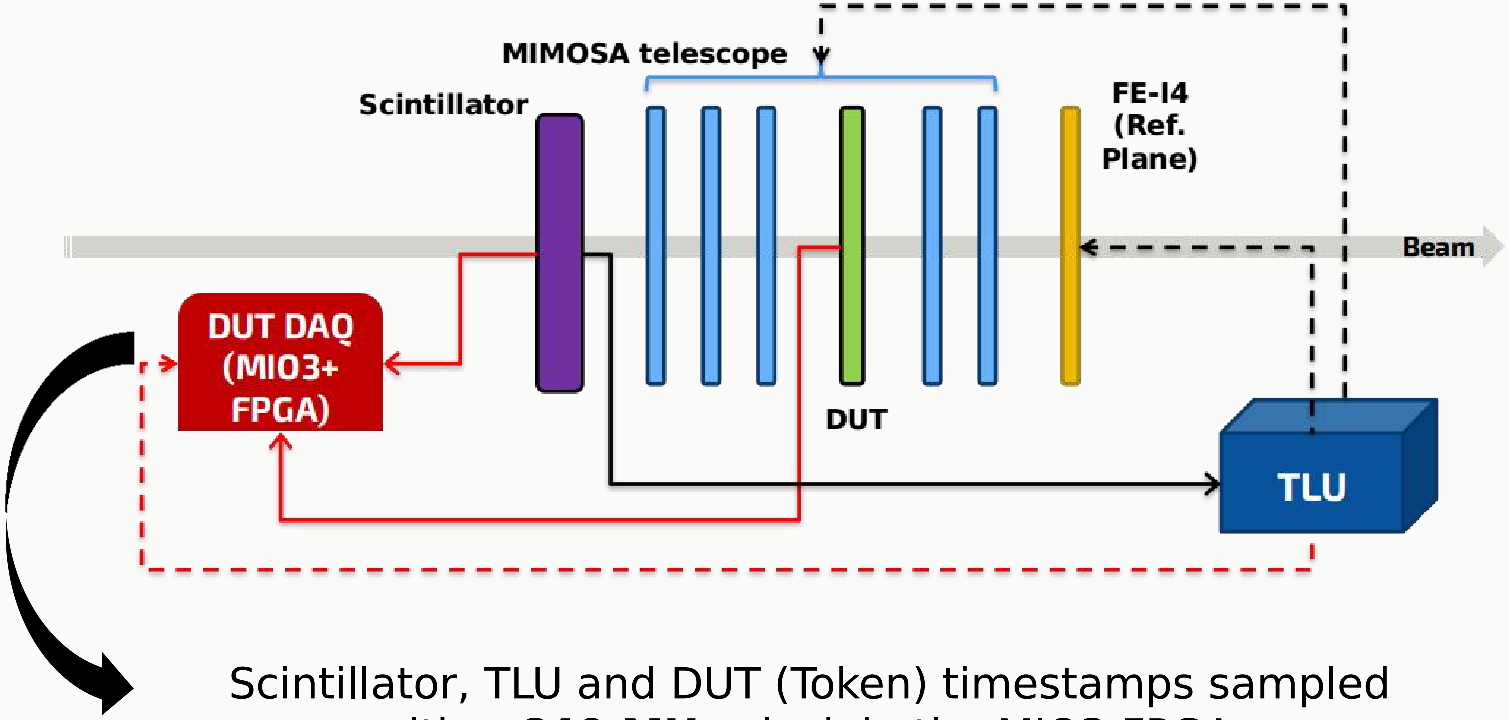
TB DATA ACQUISITION AND SAMPLING @ DESY

Telescope setup:

- 1 LF-Monopix1 DUT
  (200/100 um thickness),
- 5 MIMOSA26 tracking planes
- 1 FE-I4 timing reference plane.
- Triggered by a plastic scintillator through a TLU.

Beam: 5 GeV e- at DESY TB21

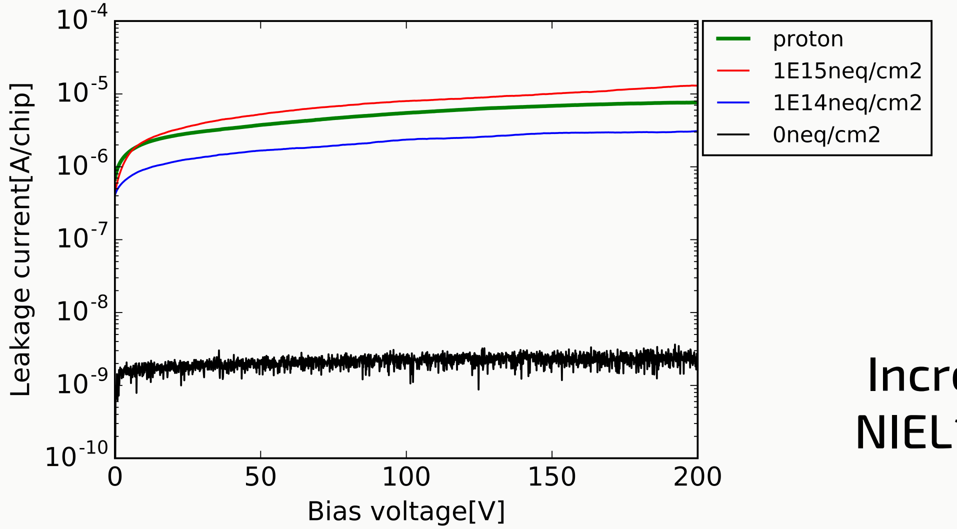




Scintillator, TLU and DUT (Token) timestamps sampled with a **640 MHz** clock in the MIO3 FPGA.

TB data analysis carried out using:
https://github.com/SiLab-Bonn/beam_telescope_analysis

NIEL: BREAKDOWN & DEPLETION IN THIN CHIPS

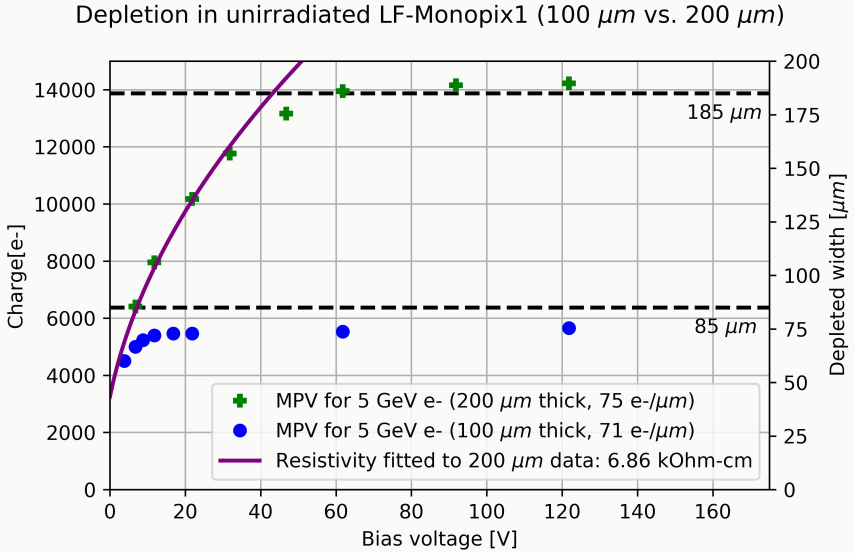


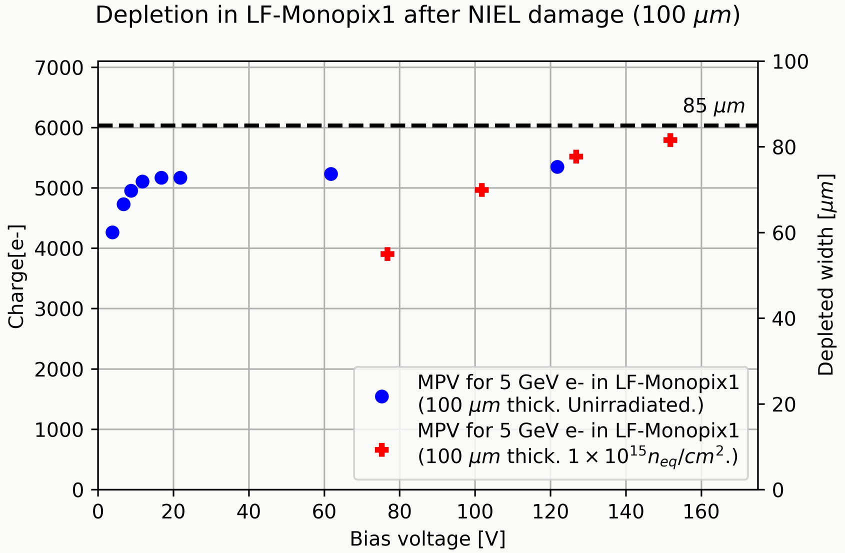
** Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C*

- **Breakdown voltage:**

  >200V

  Increase in leakage current due to NIEL*+TID damage after irradiation





- **Depletion:**

  100um thick chips fully depleted at ~150V after $1x10^{15}\ N_{eq}/cm^2$

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HIT EFFICIENCY

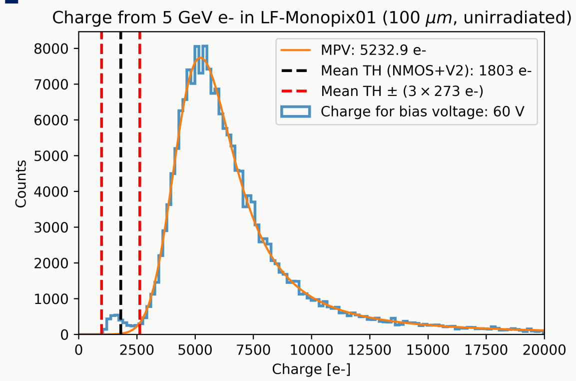
Unirradiated:

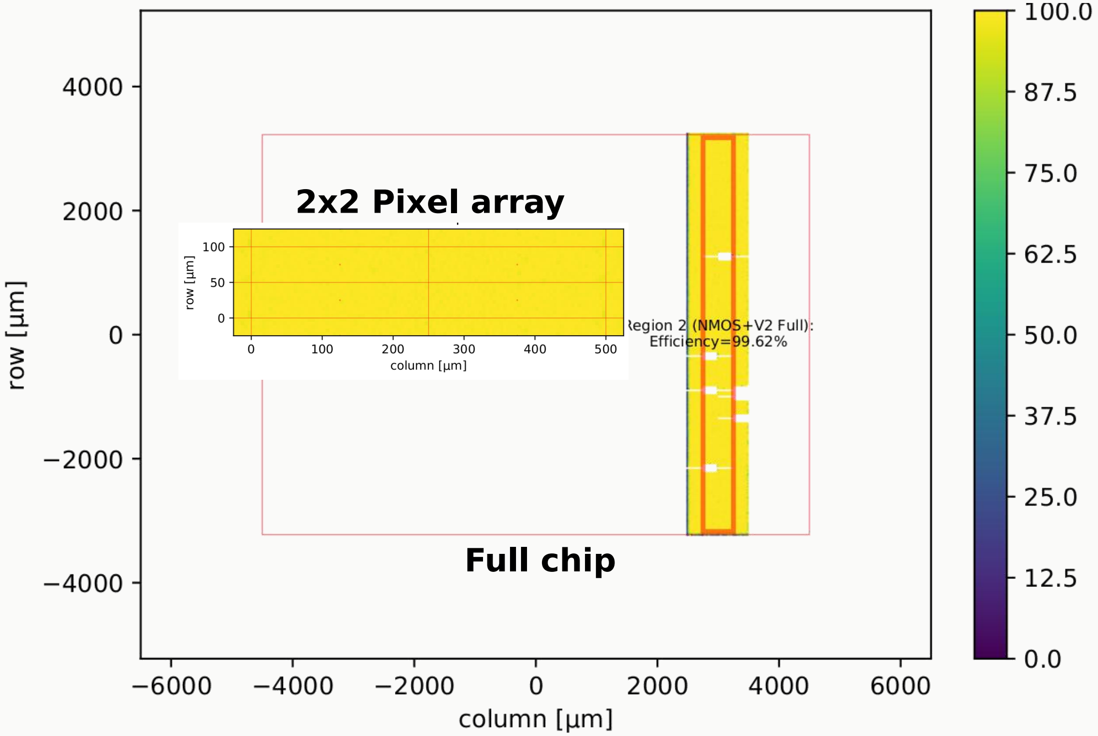
99.62%

(100 um, Bias:60V,

TH: 1885±227 e-)

Noise Occ. < $\mathbf{10^{-7}}$





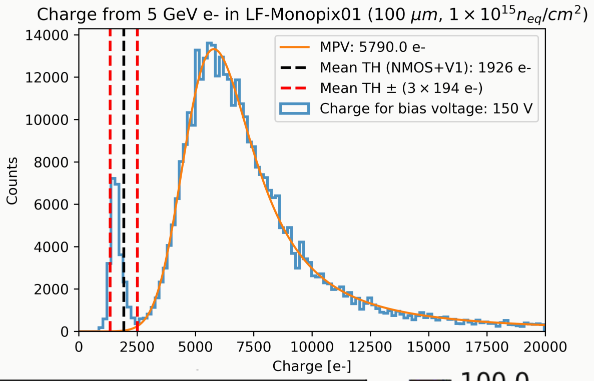
$1x10^{15}$ N_{eq}/cm^2:

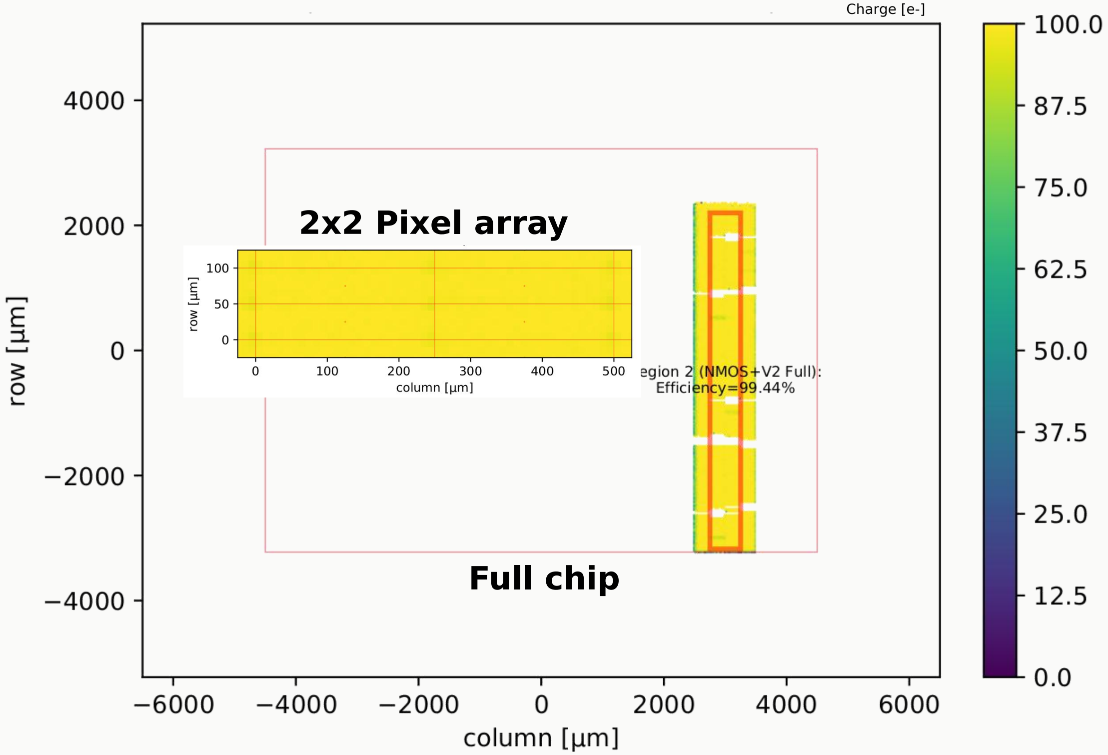
99.4%

(100 um, Bias:150V,

TH: 2336±262 e-)

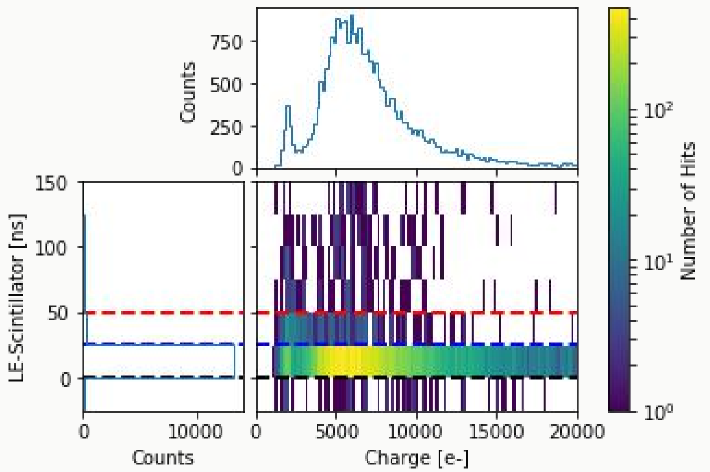
Noise Occ. < $\mathbf{10^{-7}}$





IN-TIME EFFICIENCY

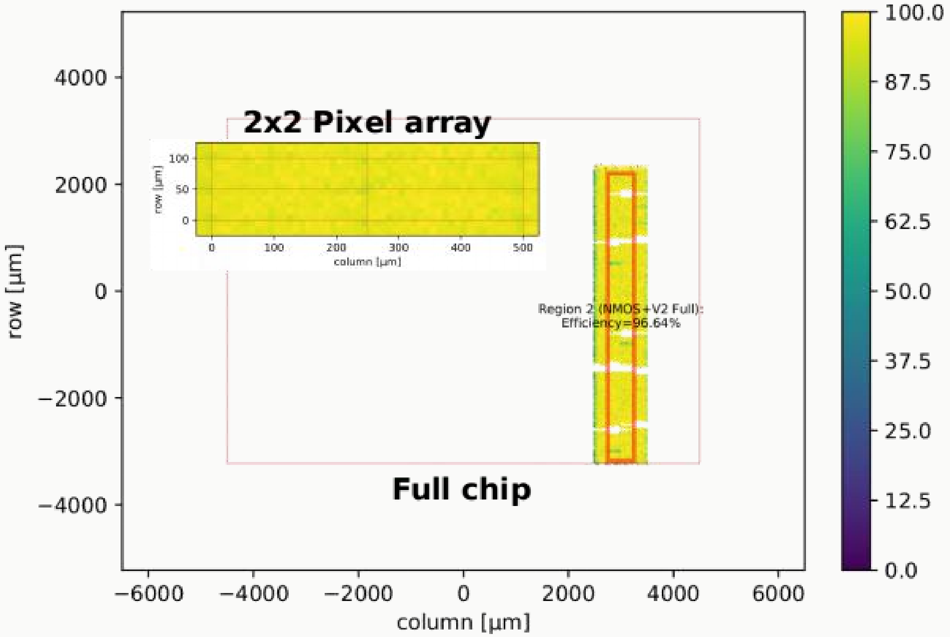
Select only efficient hits arriving within the first 25 ns.



In-time efficiency (1x10^{15} N_{eq}/cm^2): 96.64%

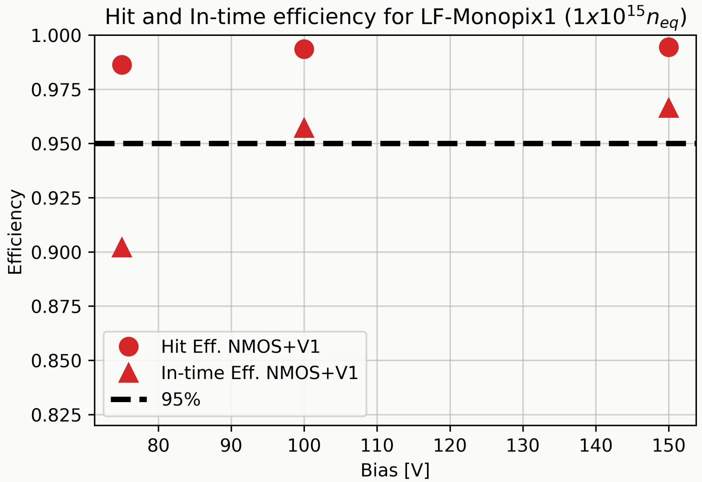
(100 um, TH: 2336±262 e-, Bias:150V)

Noise Occ. < **10^{-7}**



We require at least a **bias voltage of 100V to reach a 95% in-time** efficiency after 1x10^{15} N_{eq}/cm^2

√



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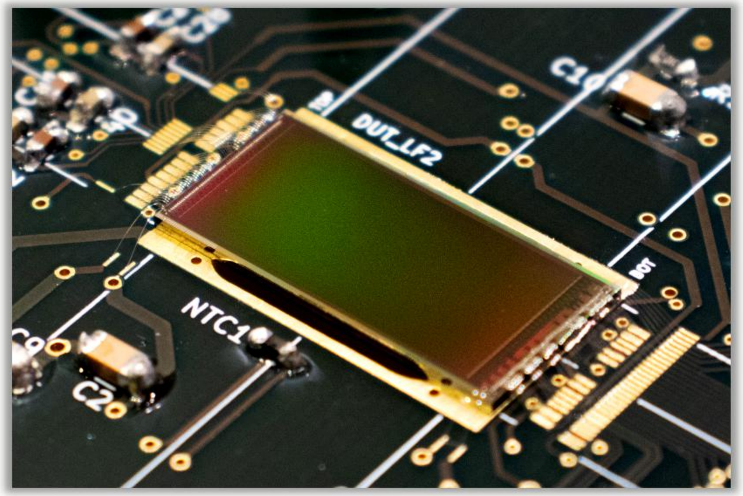
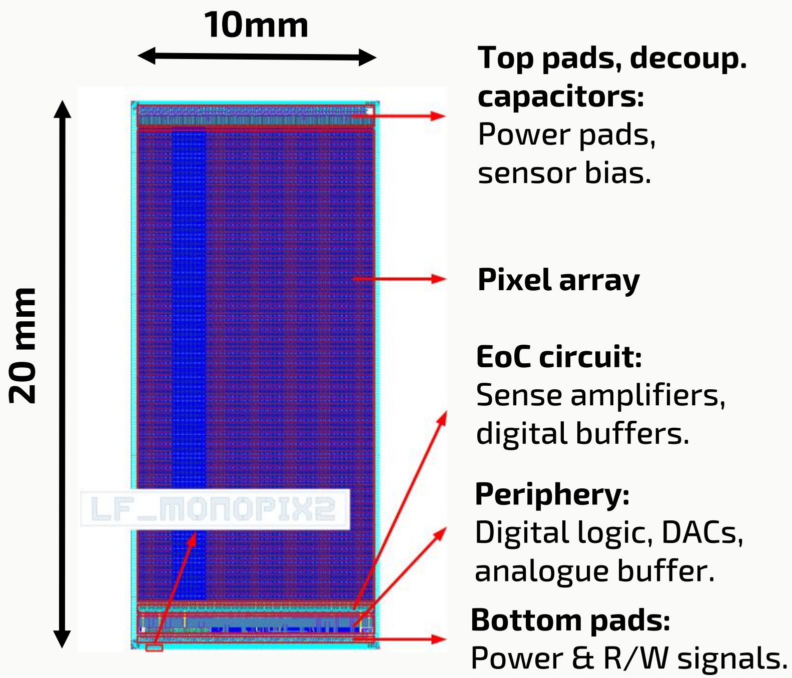
LF-MONOPIX2





- Smaller pixel pitch than LF-M1: **50 x 150 µm²**
  → Reduced C_{det}
  (ergo: lower noise & power)
  → Larger pixel array
  (**340 rows x 56 cols**)
- 40 MHz/160MHz CMOS or LVDS serial output.
- Timestamping: **6-bit LE/TE (ToT) @ 25 ns.**
- Power: **~30 µW/pixel**
- Injection & HitOr: **Digital, at pixel level.**

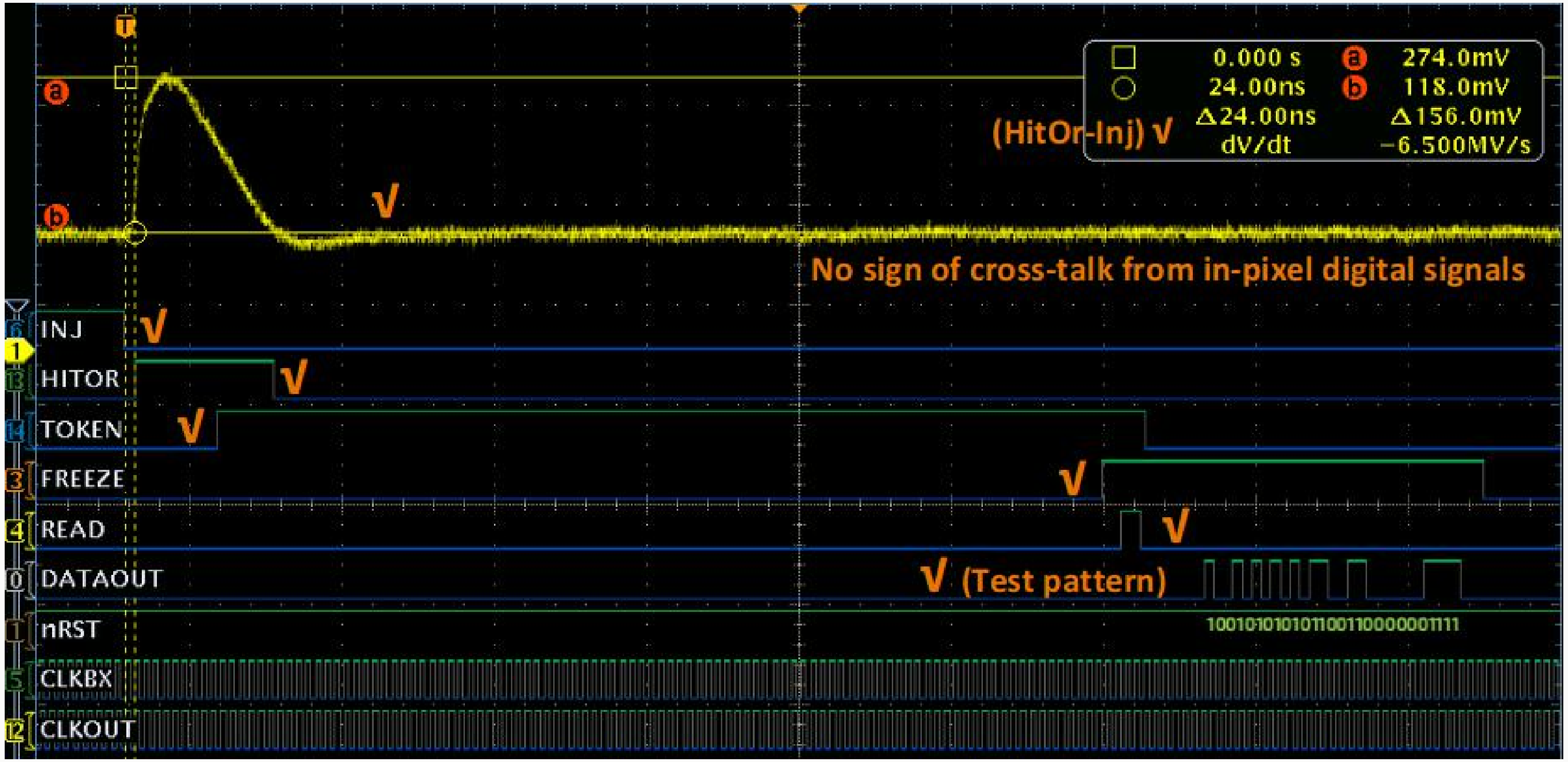
Column-drain R/O in a **2 centimeter long column**, with **full in-pixel electronics.** ☑

Rad-hard: Optimized LF-Monopix1 front-end with best timing and performance after NIEL and TID irradiation. ☑

Improved pixel layout for **further cross-coupling mitigation** ☑

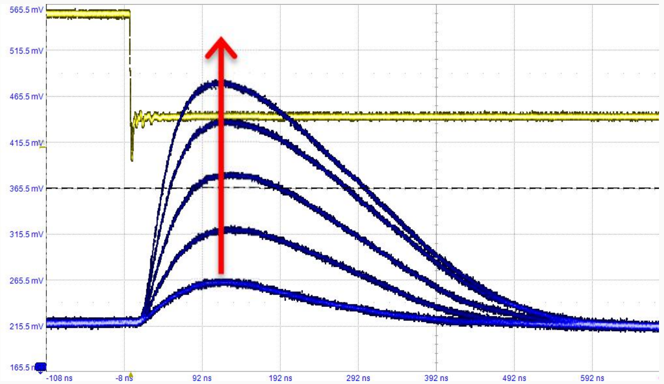
FUNCTIONAL ANALOG MONITOR, R/O AND INJECTION

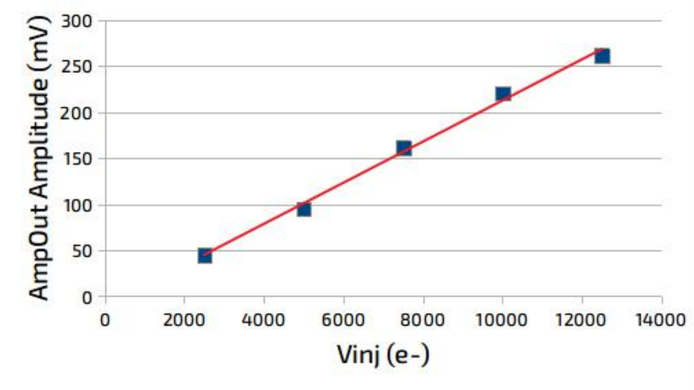
- Correct R/O architecture operation and data output.



Injection of 1V pulse to a single pixel - 40 MHz R/O enabled

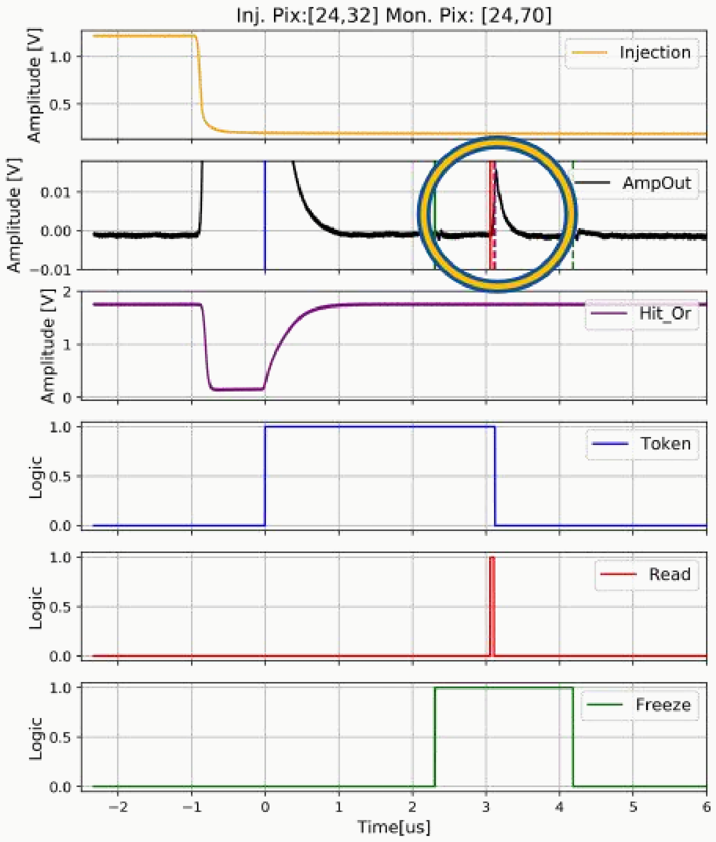
- Linear CSA response.



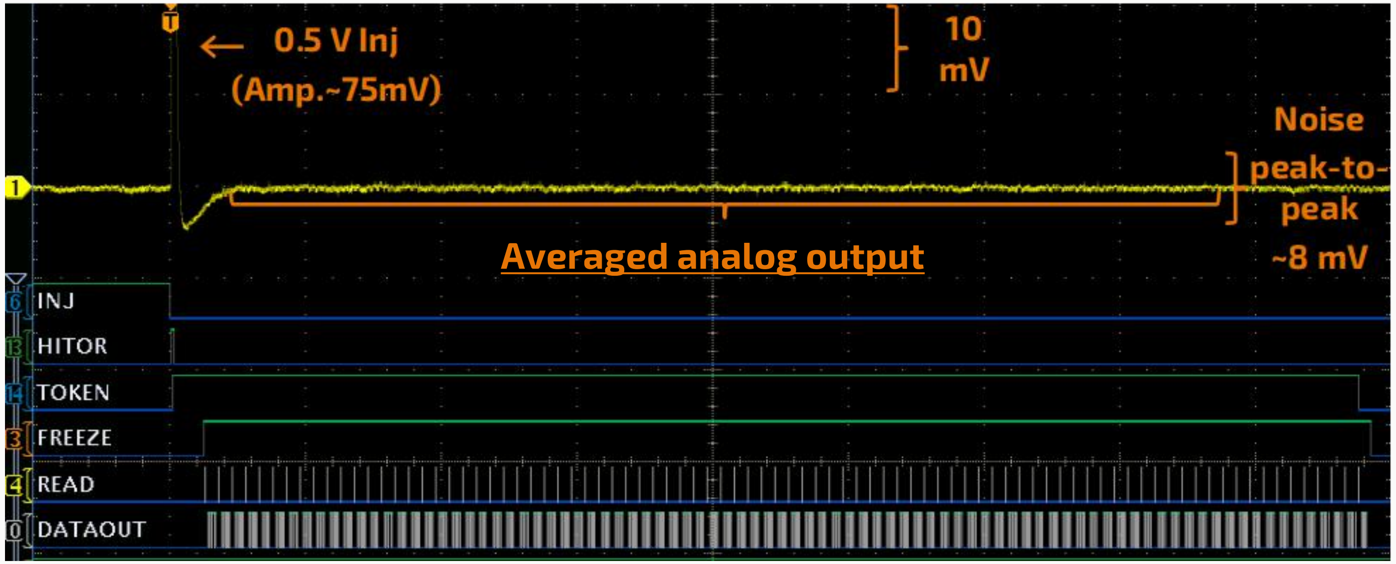


ENHANCED CROSS-COUPLING MITIGATION

- **In LF-M1:** Small coupling signal coincident with switching of READ in R/O



- **In LF-M2,** after improved pixel layout based on observations in LF-M1:



No sign of any coupling coincident with R/O digital switching while carrying signals from pixels across the column

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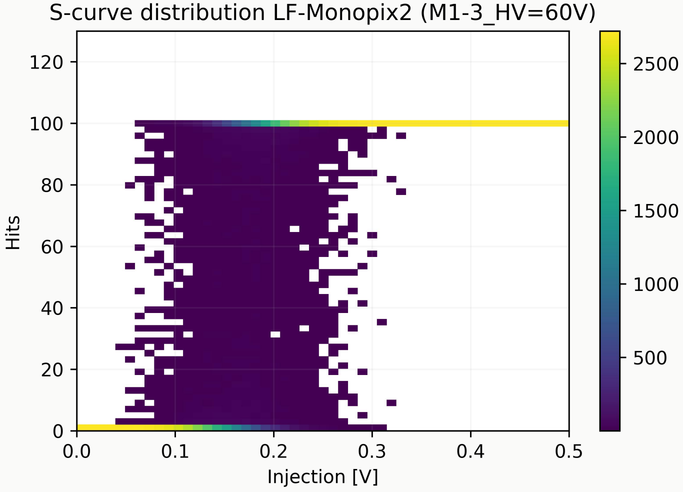
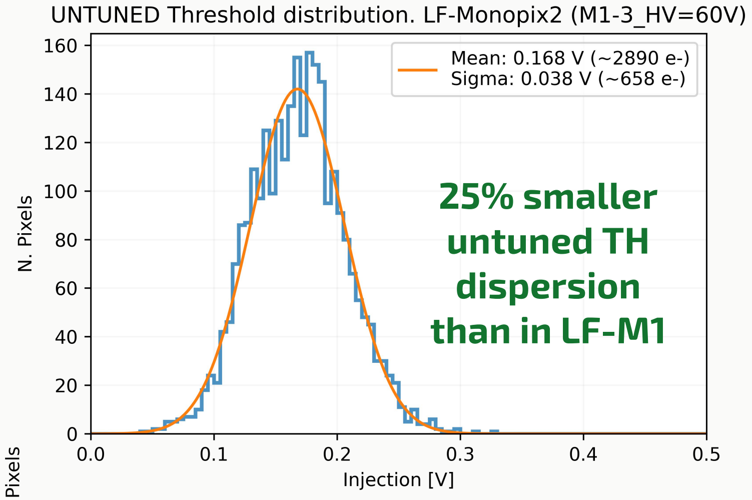
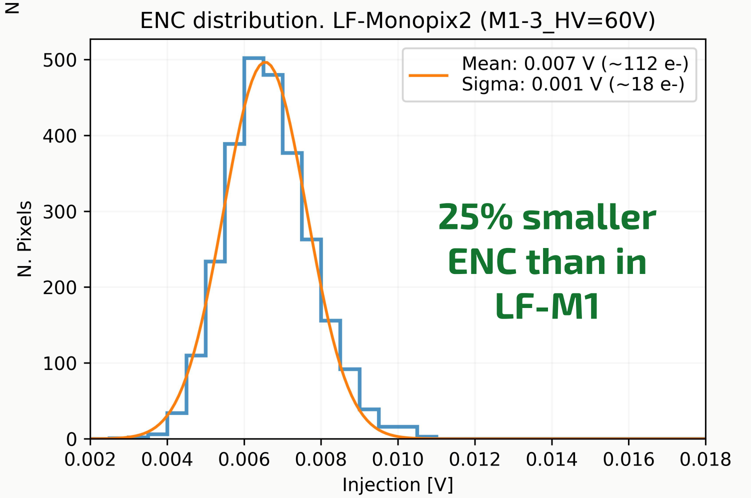
DEFAULT FRONT-END PERFORMANCE

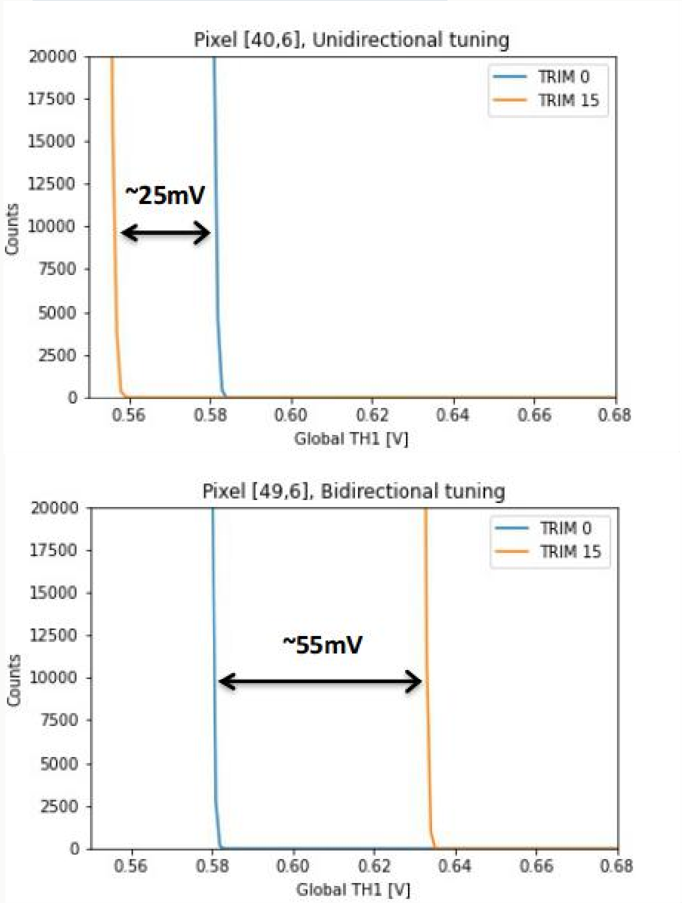
PRELIMINARY:
Untuned front-end, calibrated using the same Cinj as LF-M1.







New Bi-directional polarization of the discriminator: Larger tuning range for the same LSB current in LF-M2.



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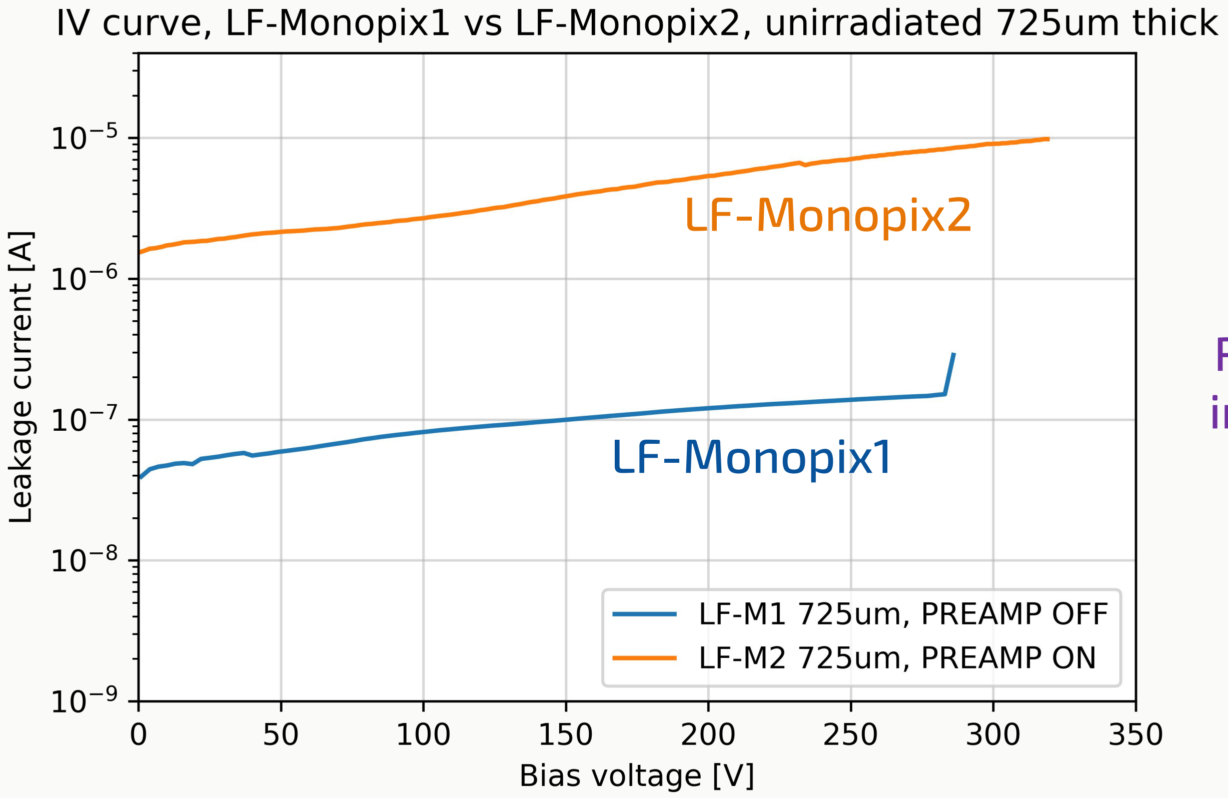
BREAKDOWN IN LF-MONOPIX2

- **Breakdown voltage improved** from LF-Monopix 1 to LF-Monopix2: >320V



Measurements at Room Temperature in a laboratory desk

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CONCLUSIONS

- **Fully functional fast R/O architecture** in large electrode DMAPS chips designed in a 150nm CMOS process on highly resistive wafers.

- X-ray irradiation and test beam measurements have demonstrated that **the LF-Monopix prototypes are radiation-hard**:
  - **Small analog and digital degradation** after 100 MRad TID dose
  - **Full depletion of thinned sensors** after neutron fluences of $1\text{x}10^{15}$ N_{eq}/cm^2
  - **Hit efficiency** after $1\text{x}10^{15}$ N_{eq}/cm^2 **> 99%**
  - **In-time efficiency** after $1\text{x}10^{15}$ N_{eq}/cm^2 **>96%**

- An updated **long-column design ("LF-Monopix2") with smaller pixel size** is back from submission and it is **fully functional**.

- Design efforts towards **improved cross-coupling mitigation and front-end performance on LF-Monopix2** are promising.

Thanks.

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