Status of the design of the RD50-MPW3 ASIC

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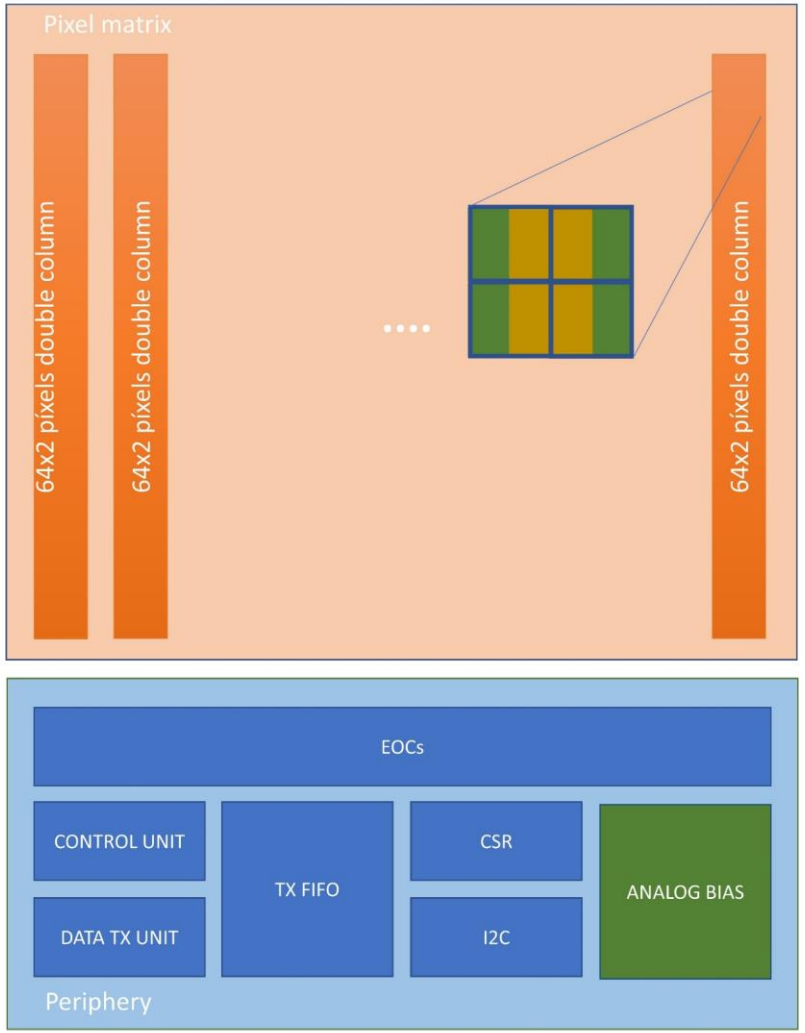
Overview

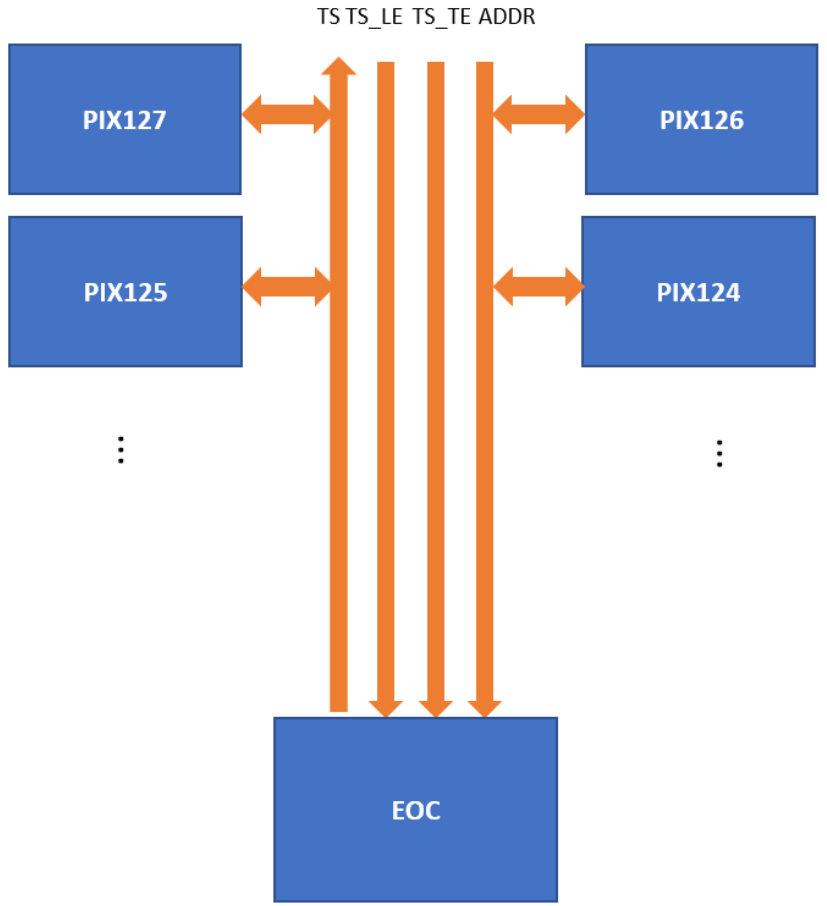
- **Motivation:**
  - RD50-MPW3 incorporating all the lessons learned from RD50-MPW1/2
  - Improve in-pixel readout circuits where possible
  - Improve routing (signals/power)
  - Develop a more optimized peripheral readout circuitry to facilitate data transmission

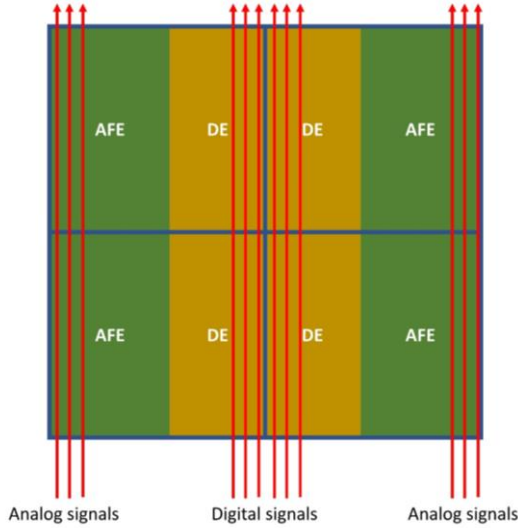
- **Features:**
  - Technology: LFoundry 150 nm CMOS
  - 64 x 64 pixel matrix
  - Pixel size: 60 x 60 μm^2
  - Sensor type: large collection electrode
  - Column drain architecture
  - Readout:
    - Synchronous
    - Zero suppression
    - Triggerless
  - Slow control with I2C interface
  - Serial data transmission at 640 Mbps



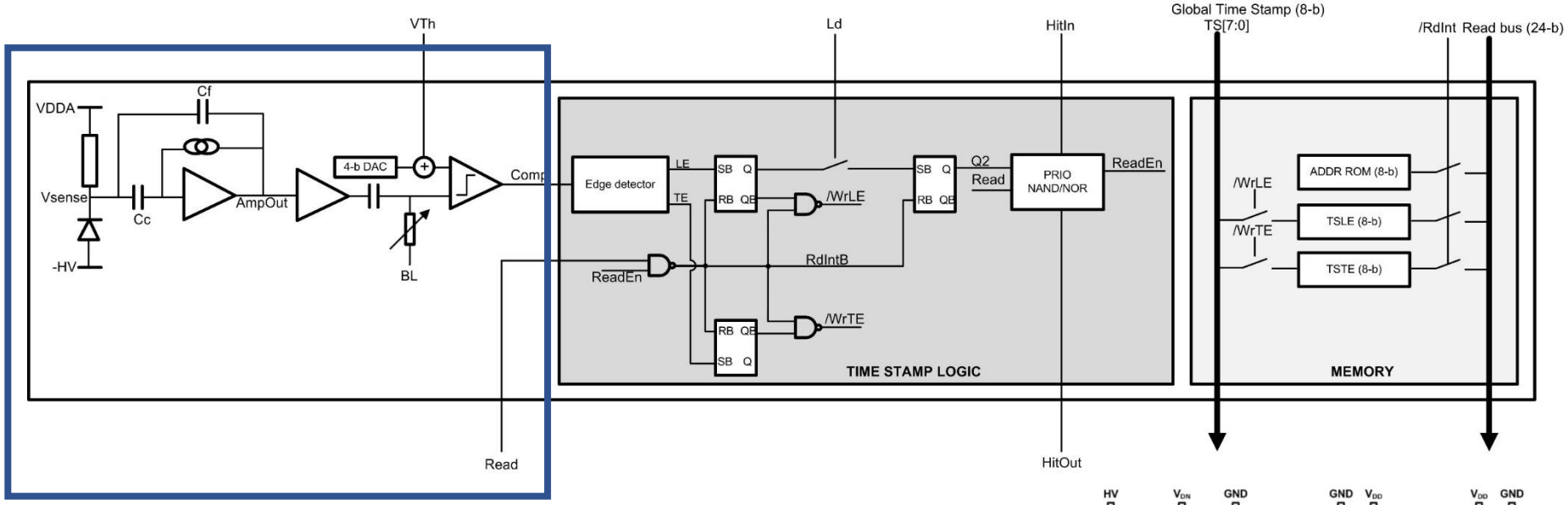
Pixel matrix

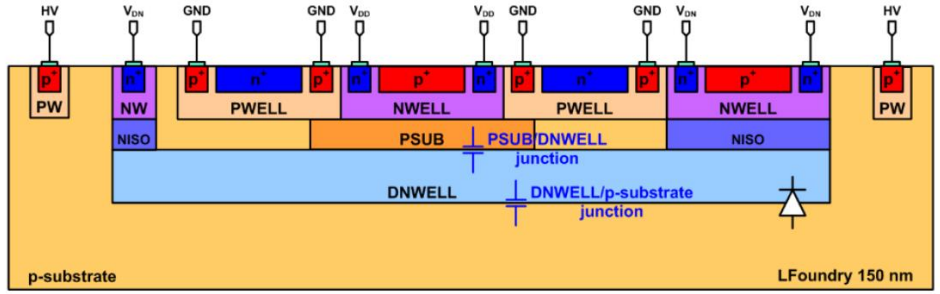
- Double column architecture:
  - signal sharing to reduce routing congestion and minimize crosstalk
  - analog and digital signals separated
- Power signals floorplan to minimize IR drops
- Simplified double column priority circuit





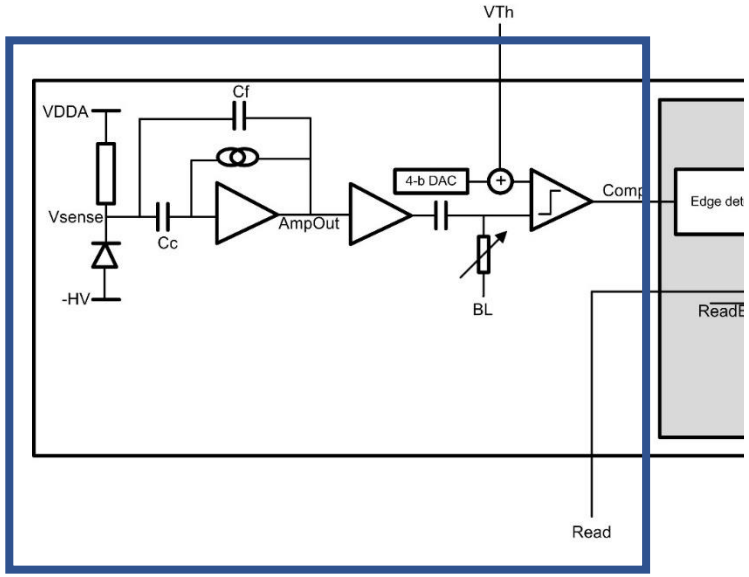
Analog front-end electronics in pixel

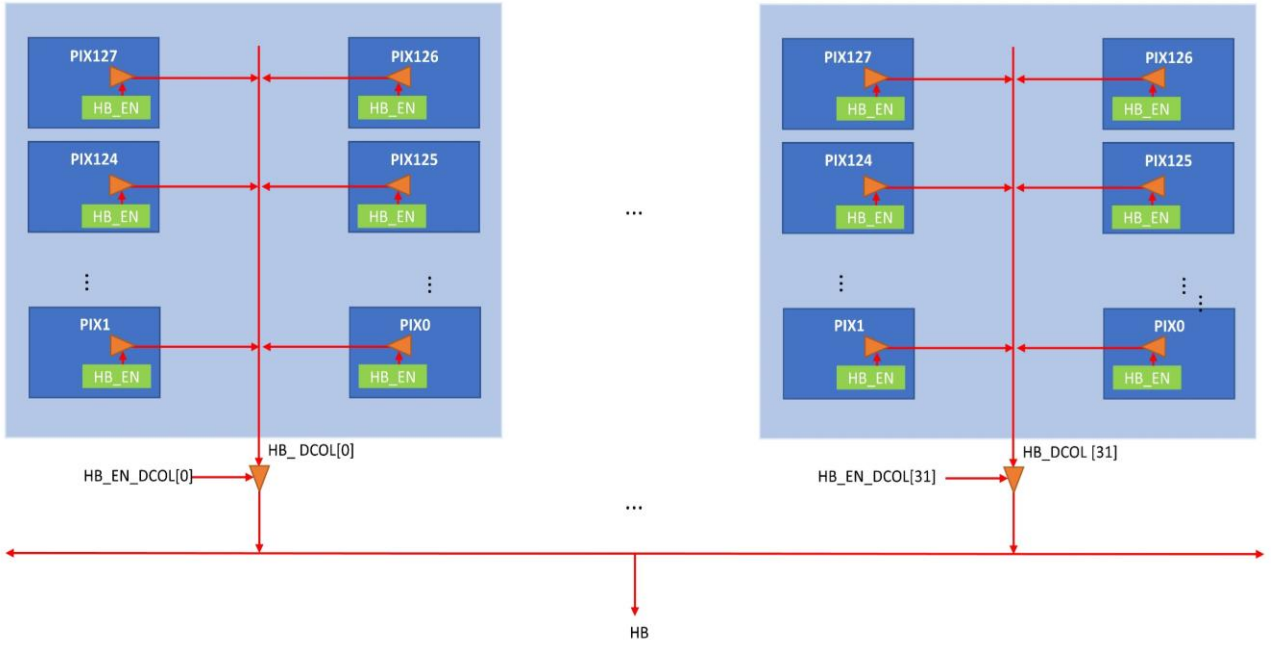




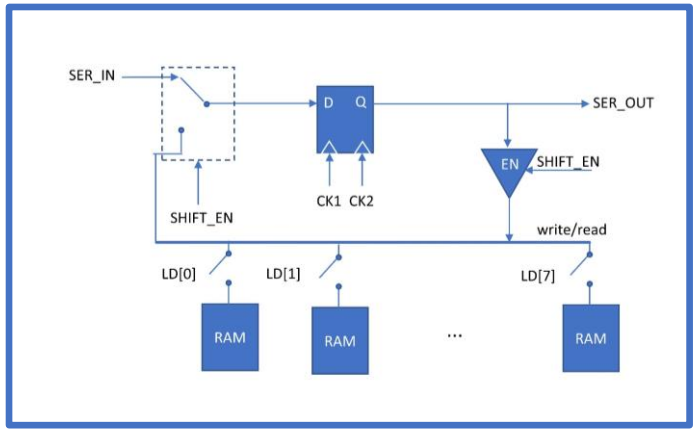
- Same sensor from RD50-MPW2
- Reuse of the analog blocs from RD50-MPW2:
  - Preamplifier
  - Discriminator
  - DACs for biasing (at the periphery)
- Monitoring scheme for preamplifier output (SFOUT) and discriminator (HB).
- Capability to mask noisy pixel (**new**)

Analog front-end electronics in pixel

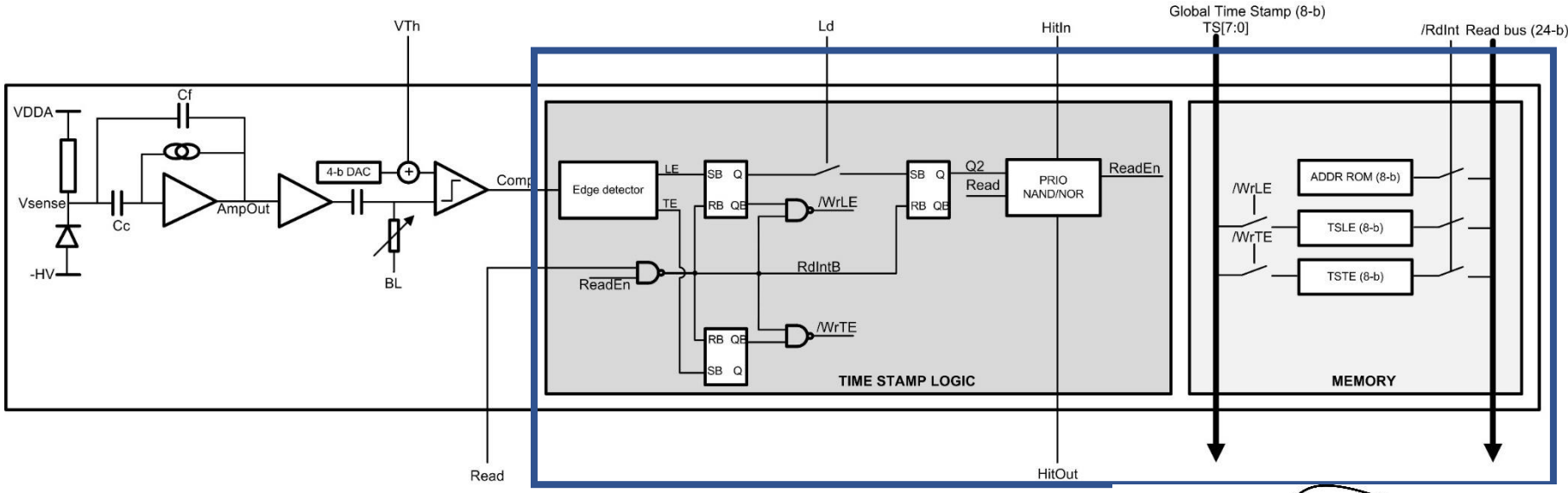




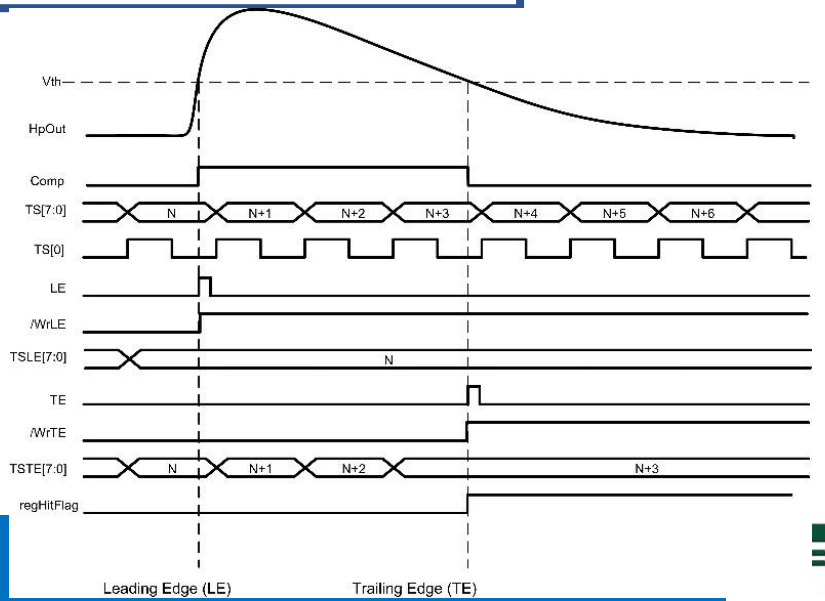
- On pixel 8 configuration bits (**new**):
  - Trimming DAC (4-b)
  - Masking (1-b)
  - Enable injection (1-b)
  - Enable discriminator monitoring (1-b)
  - Enable preamplifier monitoring (1-b)
- Serial programming



Digital electronics in pixel

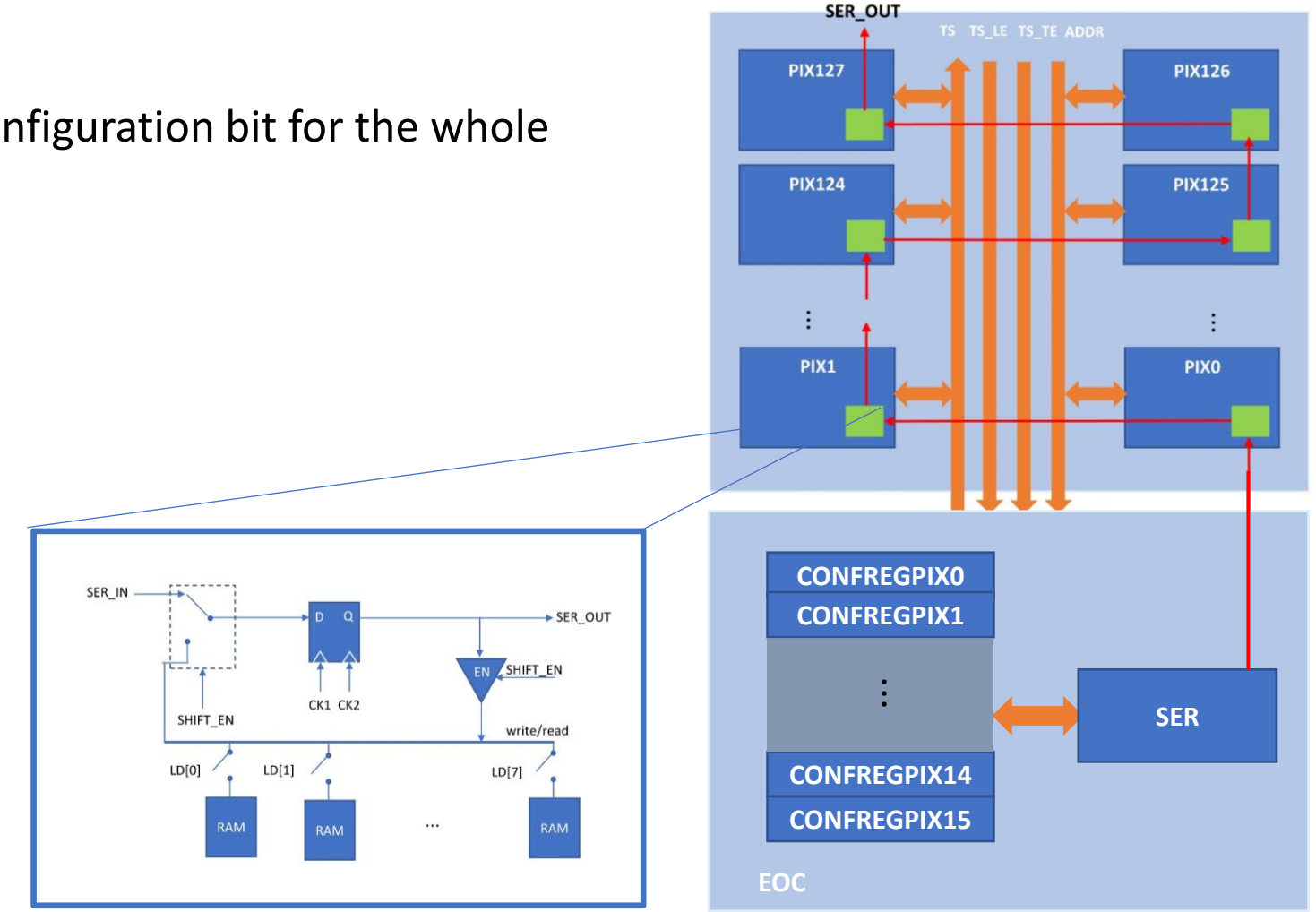


- Column-drain readout architecture
- For each hit:
  - Leading edge (LE): 8-bit DRAM memory
  - Trailing Edge (TE): 8-bit DRAM memory
  - Address: 8-bit ROM memory
- TOT = LE – TE (computed off-line)
- Hit flag + priority encoding simplified



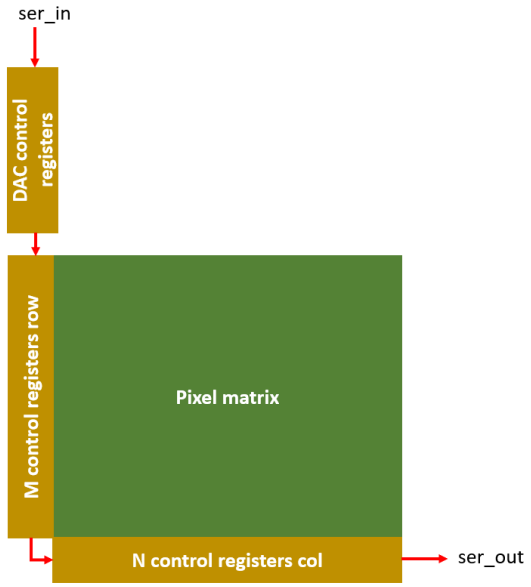
Pixel configuration

- 8-bit RAM in pixel
- Serial programming of 1 configuration bit for the whole double column.
- Serializer at EOC.

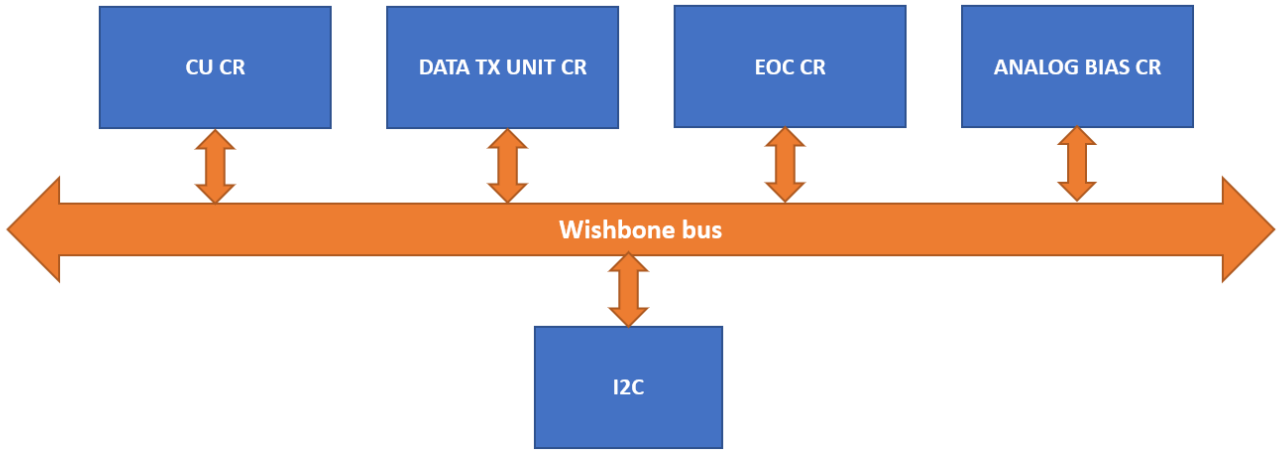


Slow control

- **RD50-MPW1/2:**
  - Very long shift register to configurate the chip
  - All configuration bits needed to be transmitted again when only changing 1 configuration bit

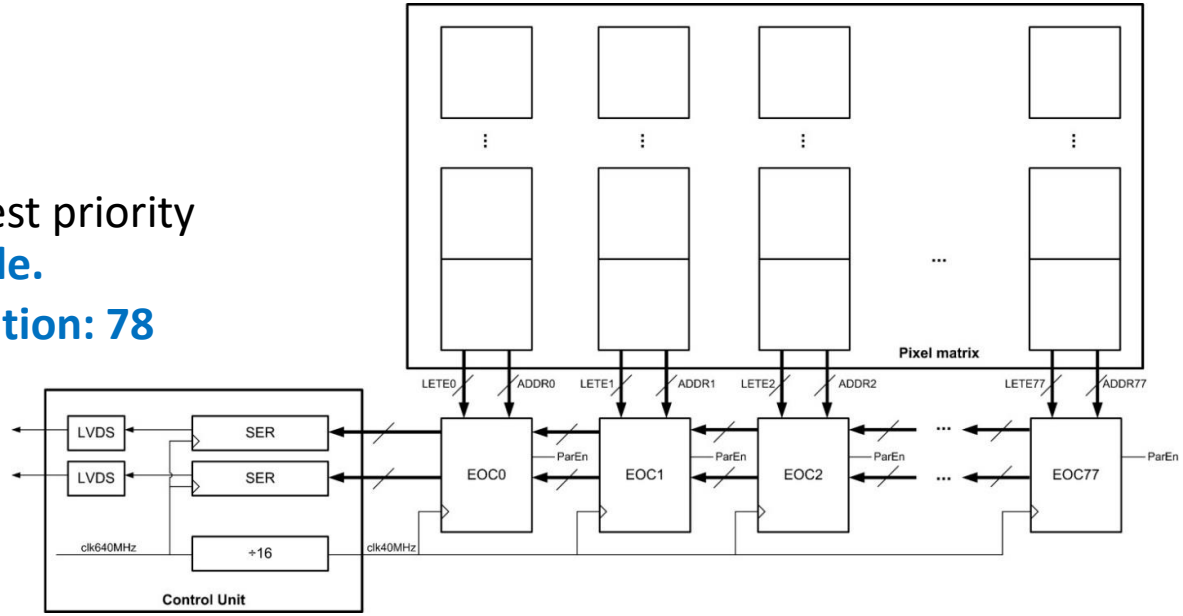


- **RD50-MPW3:**
  - 8-bit Control Registers (CR)
  - Individual access through wishbone bus
  - Byte addressable
  - I2C interface (IP from CERN)



RD50-MPW1 – Pixel matrix readout

- ToT info (LE+TE) and pixel address stored in the EOC at the periphery.
- EOCs form a shift register operating @ 40 MHz.
- Continuous readout :
  - 1) ADDR, TS_LE and TS_TE of the hit pixel with highest priority in a column stored in the EOC. **Duration: 1 clock cycle.**
  - 2) CU shifts the content of the EOCs at 40MHz. **Duration: 78 clock cycle.**
- 2 serial LVDS ports @ 640Mbps

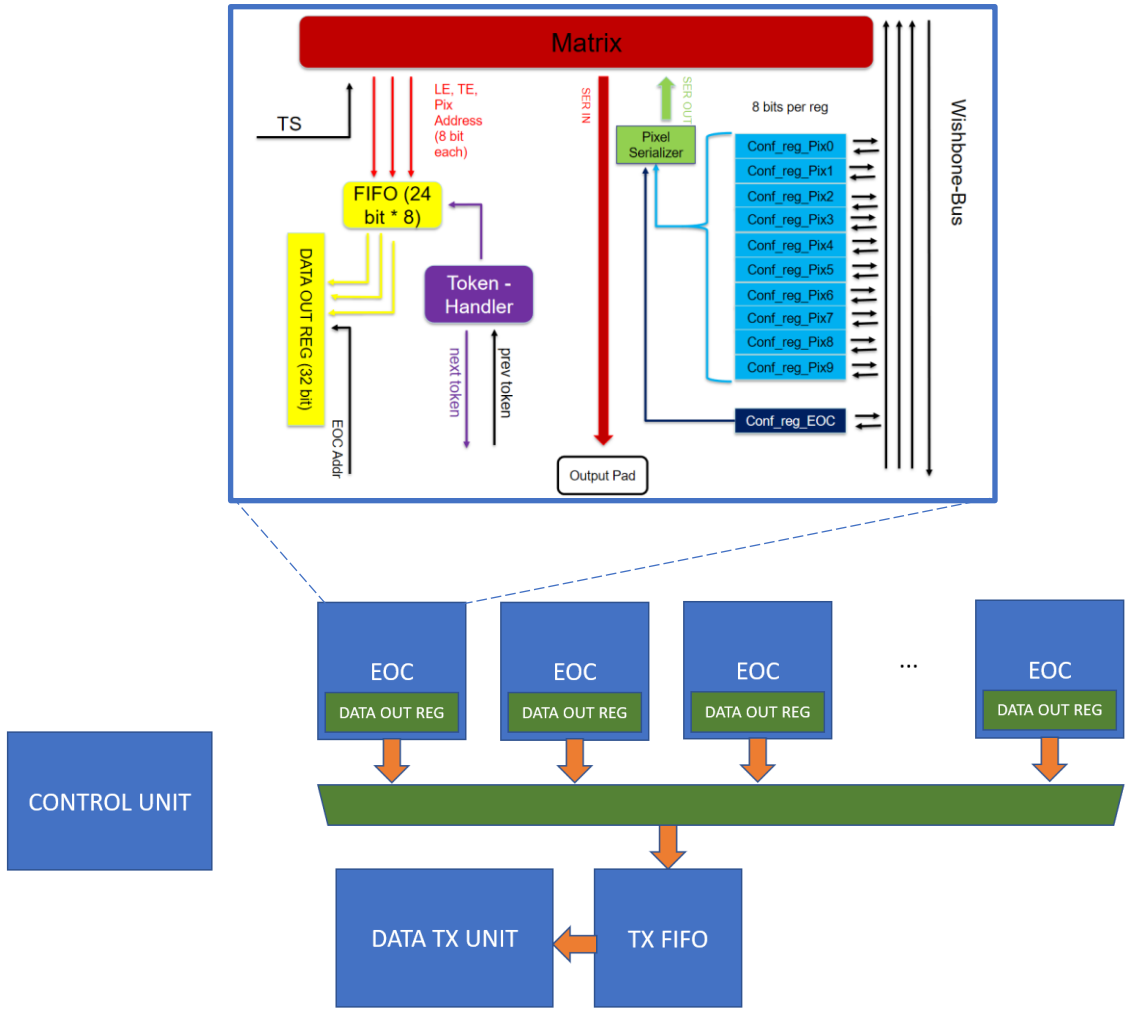


- **Limitations:**
  - Transmission of bare data (No synchronization frame, SOF and EOF)
  - Every column is given a time slot even not having data to transmit (no zero suppression)
  - Only one pixel per column is readout every 25ns * number of columns
  - A pixel can not detect a new hit until it is readout by the EOC

pixel may stay hundreds of clock cycles blocked to process a new hit

RD50-MPW3 – Pixel matrix readout

- New EOC architecture to minimize the dead time of the pixels:
  - FIFO to store LE, TE and ADDR from the pixels
  - FSM dedicated to the readout of the double column
  - Pixel readout handled by the control unit
- Hit in a pixel immediately readout if FIFO is not full
- CU reads sequentially the EOCs
- Token mechanism to determine the EOC to be read
- Read data temporally stored in a FIFO
- DATA TX UNIT:
  - Data rate: 640Mbps
  - LVDS port
  - Transmission protocol under development (SOF, EOF, 8b/10B, …)

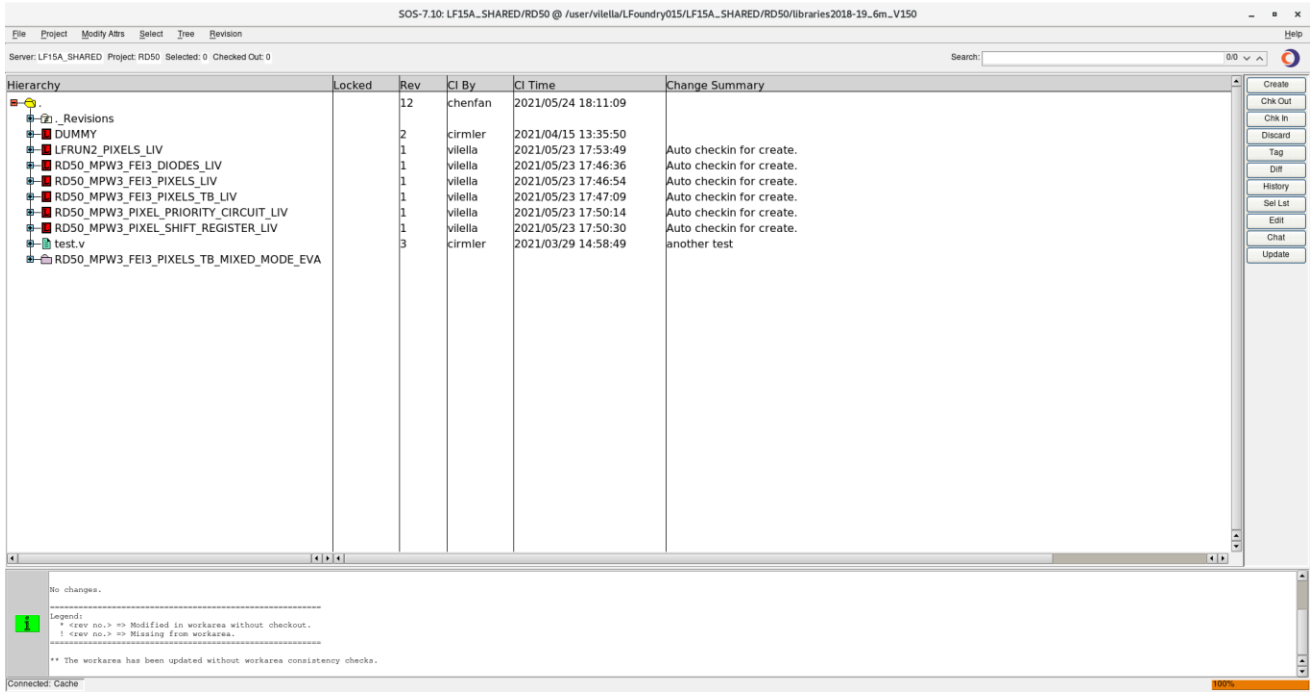


Status

- Functional model of the whole ASIC **available**
- Analog front-end electronics on pixel:
  - schematic: **ok**
  - Layout: **on-going**
- Digital electronics:
  - EOC: **RTL model available**
  - **Functional** model of the other blocks
- Verification environment: **on-going**
- Submission scheduled for October 2021

Design tools

- Cliosoft SOS 7.10 (repository for analogue design and physical implementations)
- CERN GitLab (repository for behavioural model and digital design)
- Cadence 2018-19 release (IC6.1.7)
- LFoundry15Ai PDK V1.5.0



Summary

- RD50-MPW3 incorporates all the lessons learned from RD50-MPW1/2
- Reuse of RD50-MPW2 analog electronics
- Improved digital readout electronics
- Design of RD50-MPW3 is on-going
- Possible inclusion of different test structures (not decided yet)
- Submission scheduled for October 2021