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Status of the design of RD50-MPW3 ASIC

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RD50-MPW3 is a new prototype HV-CMOS ASIC, developed by the CERN-RD50 CMOS Working Group, whose submission for fabrication is planned for Q4 2021. It is the most advanced prototype of the RD50-MPWx series. RD50-MPW1 includes a fully monolithic matrix of 40 x 78 pixels, with a very small 50 μm x 50 μm pixel area that integrates both analog and FE-I3 style digital readout electronics inside the collecting electrode. In this prototype, however, the diodes exhibit high leakage currents and the readout electronics show IR drops and crosstalk. To fix these issues, we took a staged approach. RD50-MPW2 minimizes the sensor leakage currents, in more than four orders of magnitude compared to its predecessor, with novel methodologies and includes simplified yet improved pixels. The pixel size is 60 μm x 60 μm to increase the spacing between the HV ring and the collecting deep n-well to achieve higher breakdown voltages of 120 V before irradiation. The pixels include analog front-end electronics only to simplify the design and are arranged in an 8 x 8 matrix.
RD50-MPW3 will incorporate all the lessons learnt so far and fix the IR drops and crosstalk. This ASIC will include a fully monolithic matrix of 64 x 64 pixels with a 60 μm x 60 μm pixel area and both analog and FE-I3 style digital readout electronics. To reduce the number of routing lines and minimize the crosstalk, the pixels will be arranged in a double column scheme and will be configured through serial circuitry. Other improvements will focus on increasing the readout speed of the peripheral electronics by means of more efficient End Of Column (EOC) blocks and an I2C link to read/write the control status registers. The data will be packed into frames, zero-suppressed and serialized at 640 Mbps. A transmission protocol will be implemented to facilitate data transmission and resynchronization. The design will follow a digital-on-top flow to guarantee the timing and power performance. Figure 1 shows a block diagram of RD50-MPW3.
In this talk, the authors will present the status of the design of RD50-MPW3.

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