A high speed serializer ASIC for ATLAS Liquid Argon calorimeter upgrade

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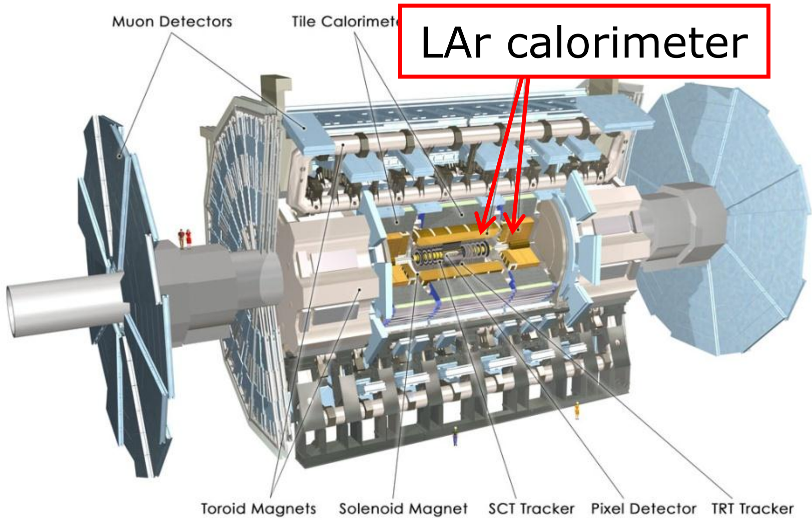
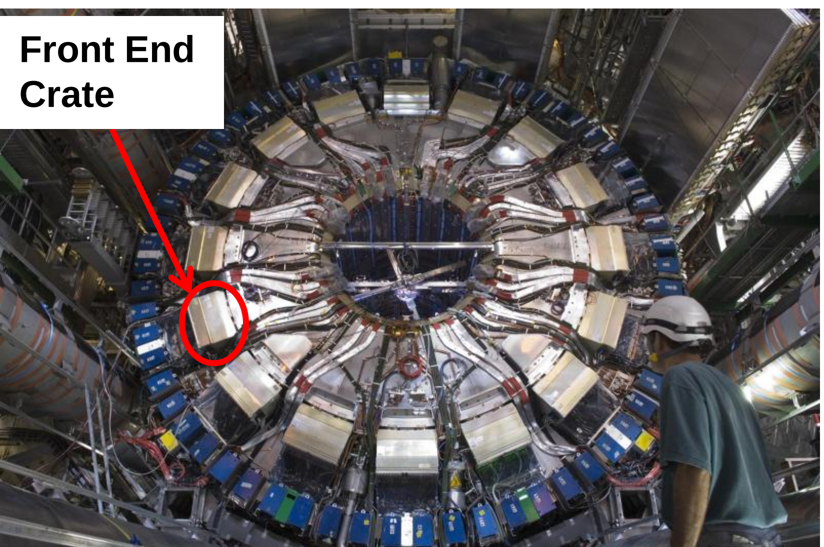
Outline

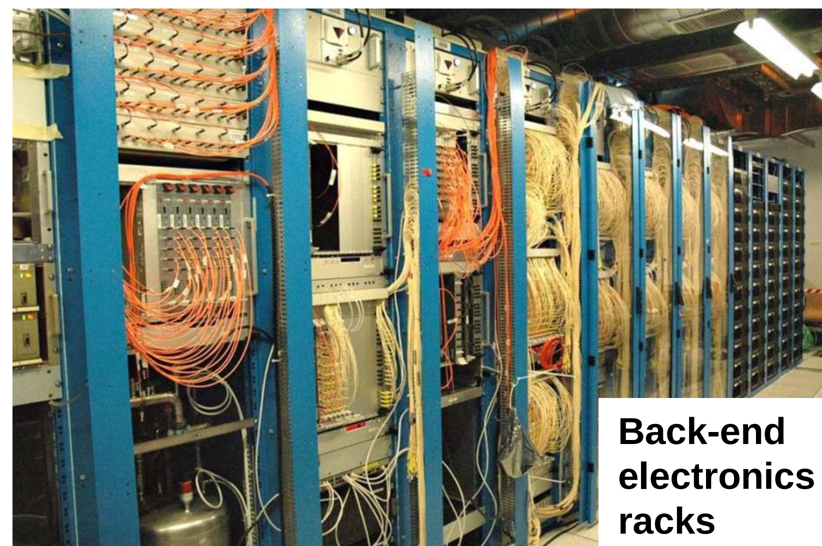
- ❑Introduction
- ❑The design and test of a single–channel serializer
  - – Design
  - – Lab test
  - – Radiation test
- ❑The design of a double-channel serializer
- ❑Conclusion

The ATLAS Liquid Argon calorimeter



- 182,486 detector channels
- Front-end electronics (FE) on the detector in radiation environment
- Back-end electronics (BE) in a shielded counting room
- Fiber optical links between FE and BE

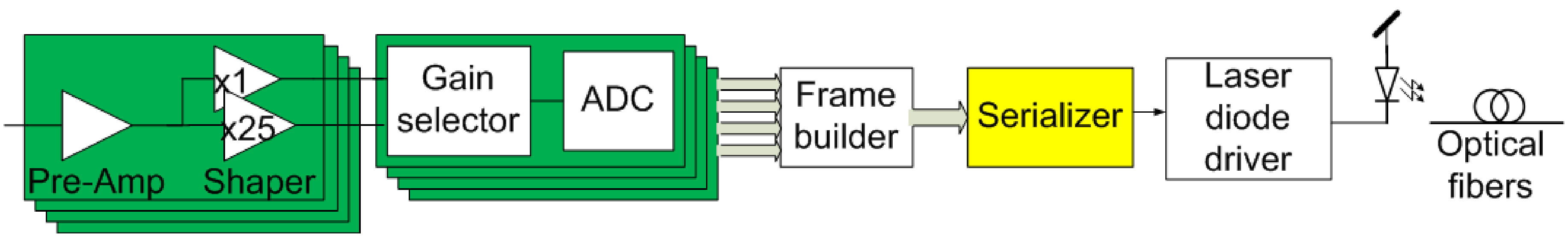




The LAr electronics upgrade

- Challenges raised by the LHC upgrade on LAr electronics
  - 10x more radiation
  - 20x more pile-up events
- LAr electronics upgrade baseline:
  - Remove analog Level-1 trigger sum from the front-end boards (FEBs)
  - Transfer all digitized data off the detector (about 100 Gb/s per FEB)
  - Implement a fully digital off-detector trigger with a higher trigger rate and a longer trigger latency
- Fiber optical links upgrade
  - High speed (8 – 10 Gb/s each link)
  - Multichannel
  - Radiation tolerant
  - High reliability

ID 187, Hucheng Chen, "Readout Electronics for the ATLAS LAr Calorimeter at HL-LHC", June 10, 16:00



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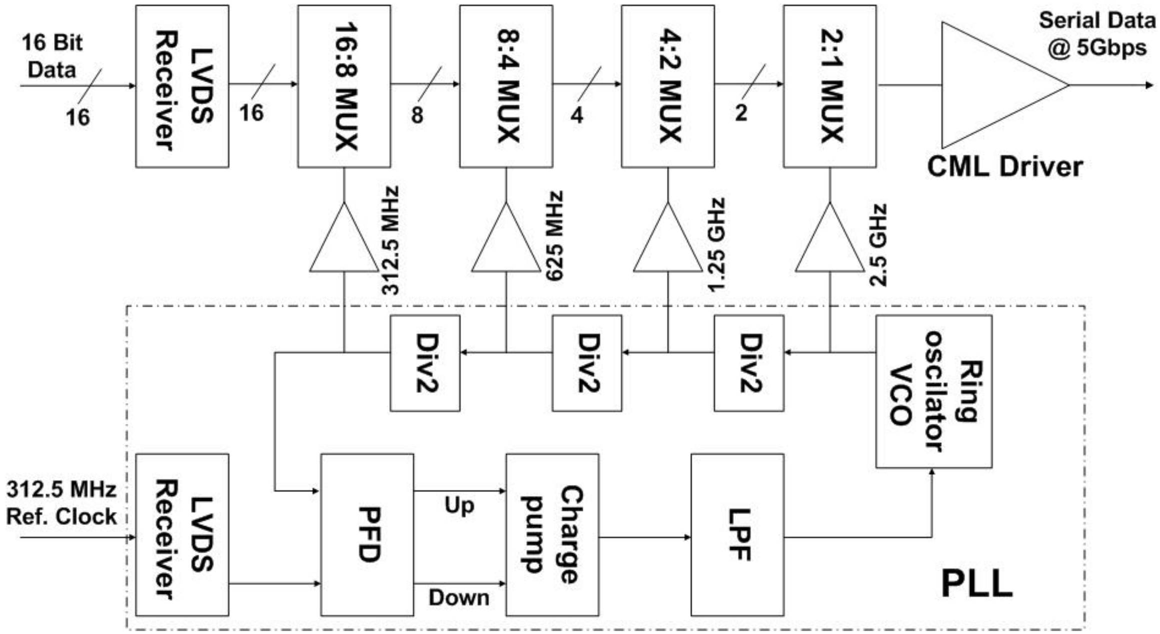
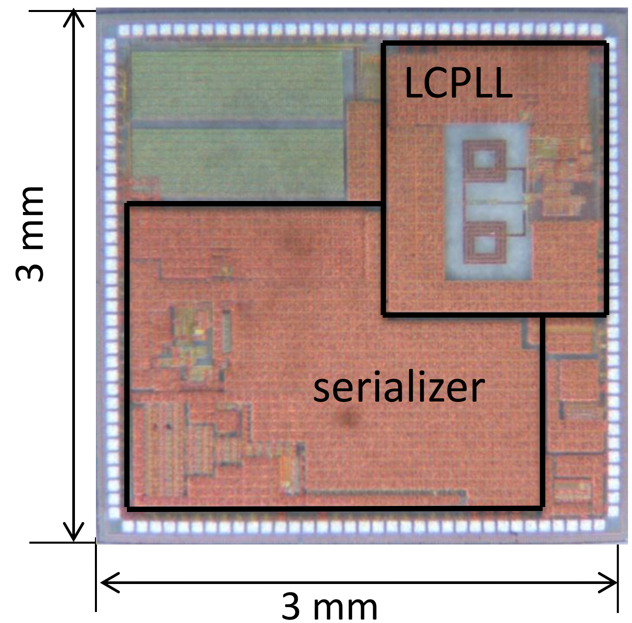
Single-channel serializer - Design



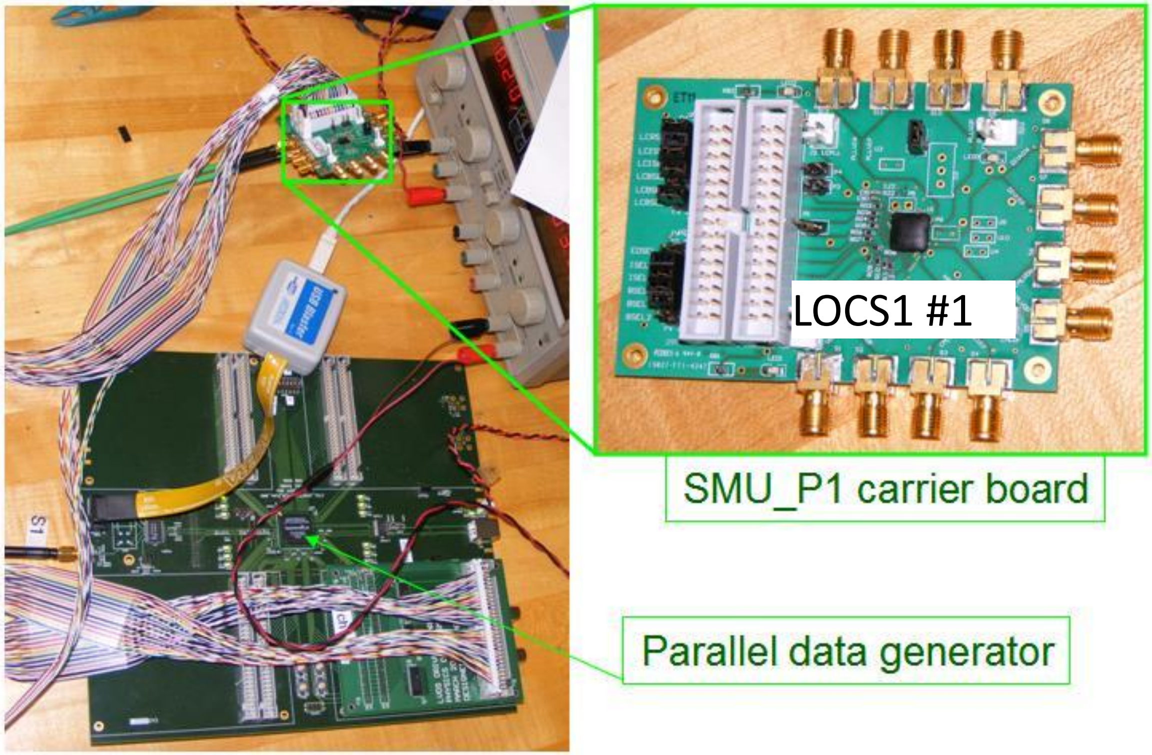
Design diagram



Die micrograph

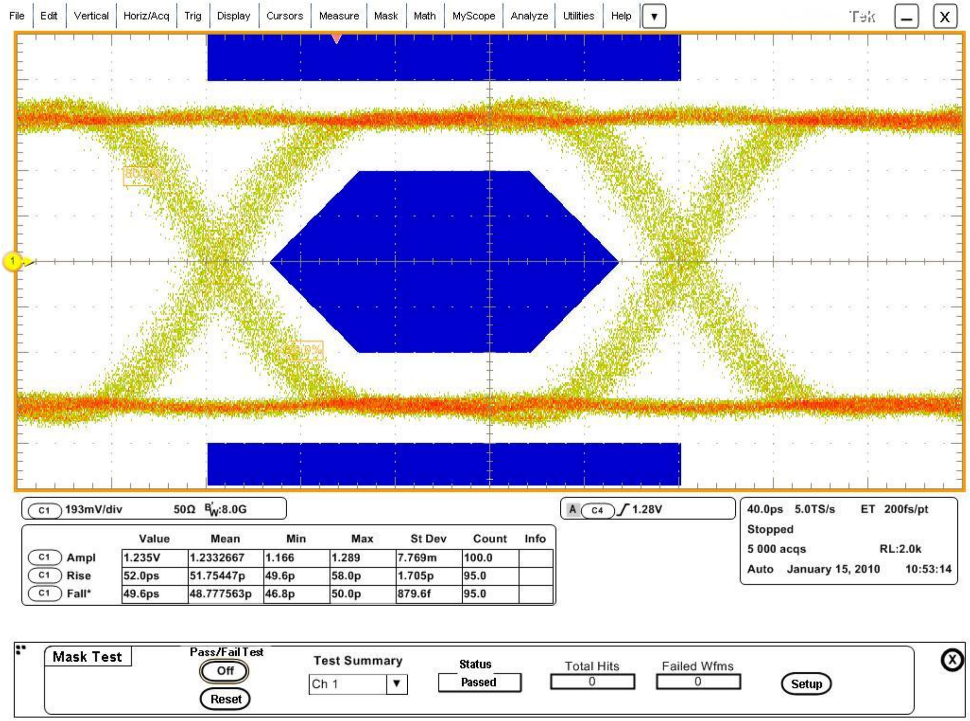
- A 16:1 CMOS multiplexer has a binary tree architecture
- A ring oscillator based PLL generates clocks of each stages
- A differential CML driver drives serial data at 5 Gb/s to coax cables

Single-channel serializer - Test setup



- An FPGA board provides a 312.5 MHz clock and 16 bit parallel data to a chip carrier board, both in LVDS
- 5 Gb/s PRBS serial data are monitored using an oscilloscope or BERT

Single-channel serializer - Lab test



Eye diagram at 5 Gb/s

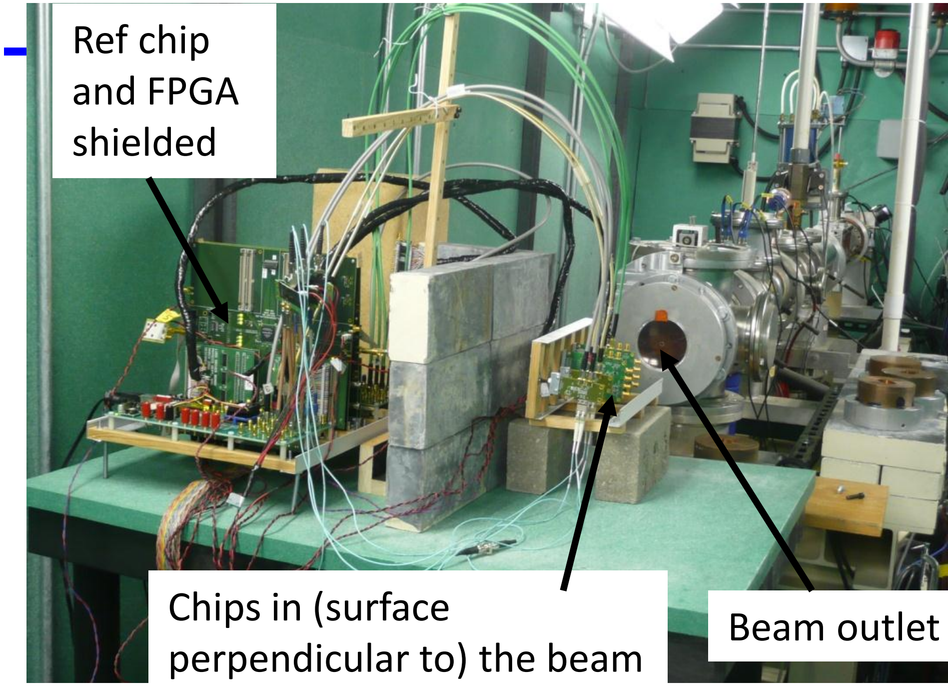
The mask is adapted from FC 4.25 Gb/s and scaled to 5 Gb/s

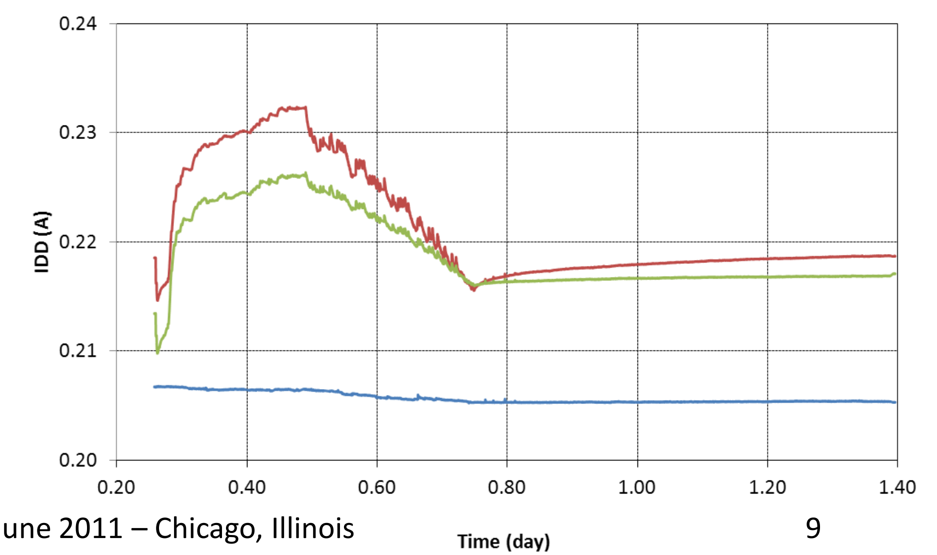
Output amplitude (peak-peak, V)	1.16
Rise time (20% - 80%, ps)	52.0
Fall time (20% - 80%, ps)	51.9
Total jitter @ BER 10^{-12} (peak-peak, ps)	61.6
Random jitter (RMS, ps)	2.6
Deterministic jitter (peak-peak, ps)	33.4
Power consumption (mW)	463
Minimum data rate (Gb/s)	4.0
Maximum data rate (Gb/s)	5.7

Single-ch serializer - Radiation test

Setup:
- 200 MeV proton beam at IUCF
- 2 chips in the beam and 1 chip shielded (ref)

Results:
- Total ionization dose effects
  - All chips continue to function throughout the test
  - The power supply currents (I_{DD}) change less than 6% during the irradiation.
- Single event effects
  - Single bit errors: 5 bit flips in total → BER < 10^{-17} after LHC upgrade
  - Synchronization errors: 28 in total → 3 errors in 10 year operation time





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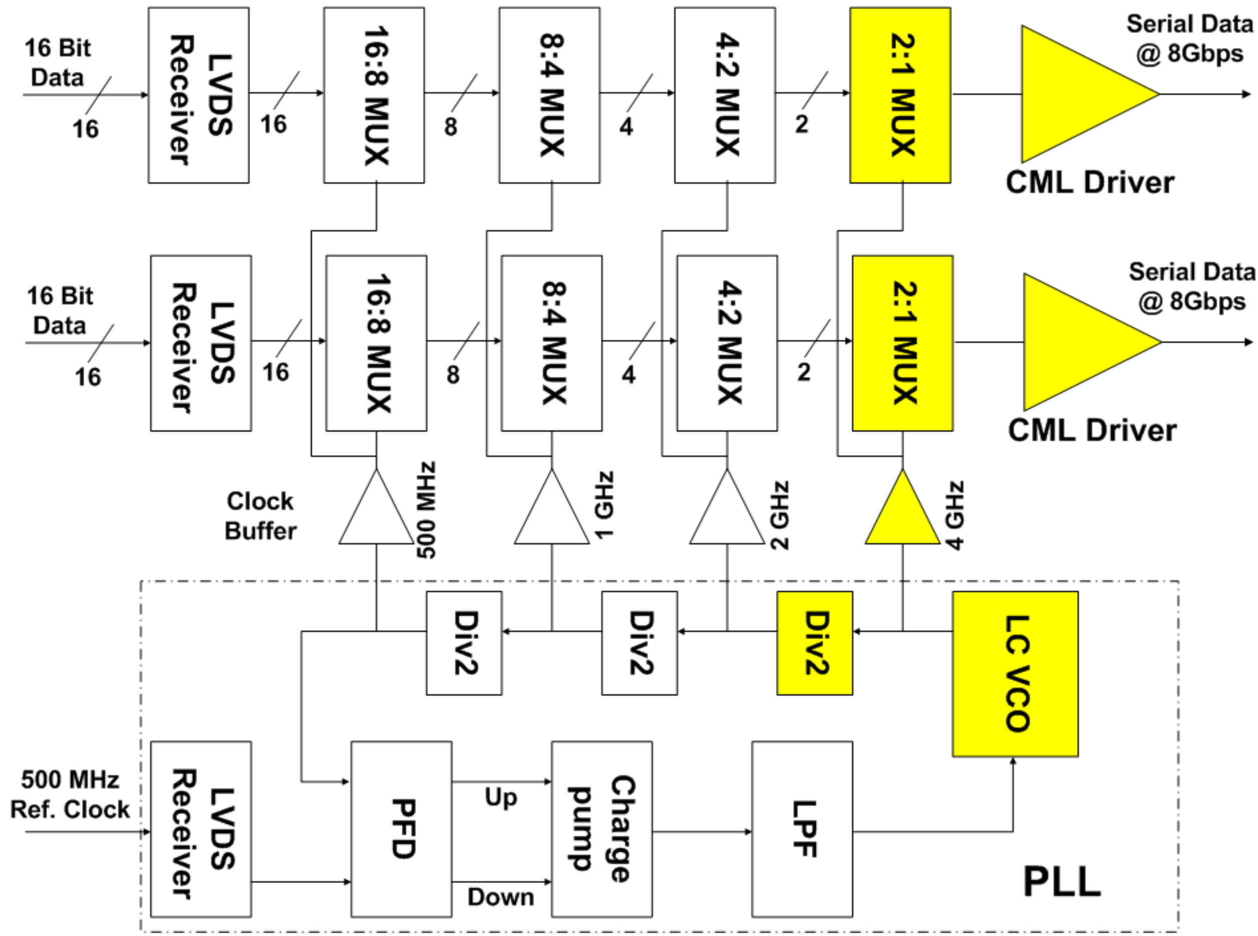
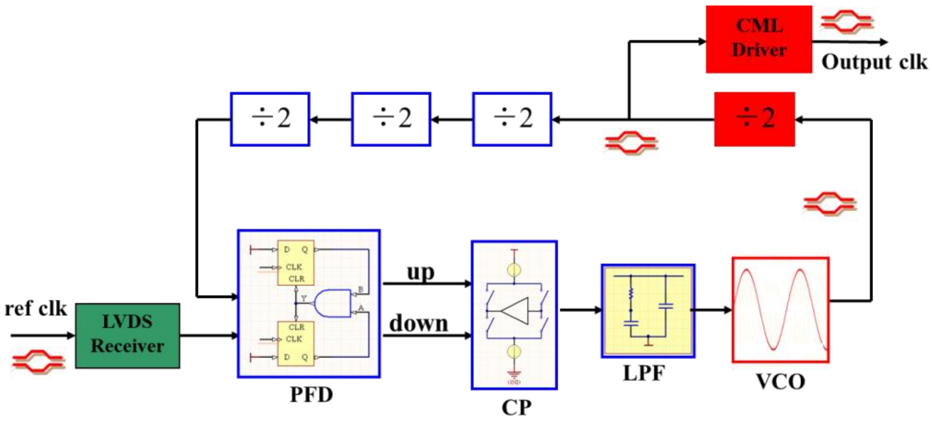
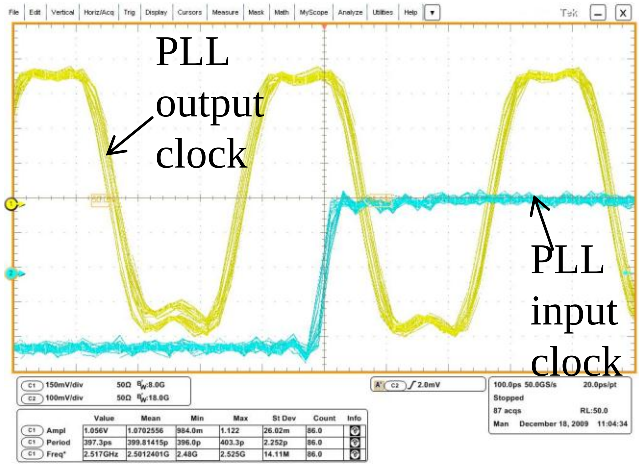
Double-channel serializer – Overview

- Two 16:1 serializer channels
- Data rate ~ 8 Gb/s each channel
- Basic architecture and low speed CMOS circuits are inherited from the single-channel version
- LC PLL has been implemented and tested
- The design of all the fast (CML, shapes in orange) parts have been done.



LCPLL

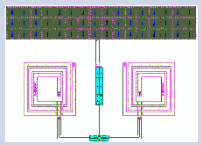
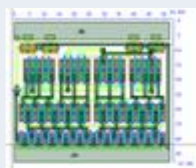
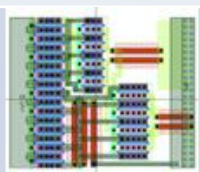
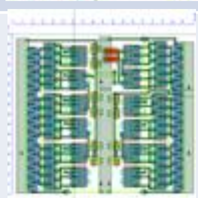
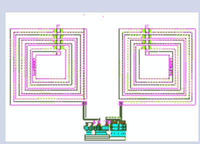




An LC phase locked looped (PLL) has been implemented in the same prototype as the single channel serializer ASIC and tested. The major test results:

- ❑ Power consumption: 111 mW at 4.9 GHz. Compare: ring oscillator based PLL, 173 mW at 2.5 GHz
- ❑ Tuning range: 4.7 to 5 GHz. Expectation: 3.8 to 5 GHz. A design error in the first stage of the divider chain has been identified. A new design has been done.
- ❑ Random jitter: 1.3 ps (RMS)
- ❑ Deterministic jitter: 7.5 ps (pk-pk)

2-ch ASIC design – fast parts

Parts	layout	Area (μm^2)	Power (mW)	Performance
VCO		500x900	4.5	Implemented and tested. Tuning range is 3.7 ~ 5.0 GHz
Divider (÷2)		50x50	5.3	Max operation freq. > 4.25 GHz in the worst corner and 85 °C
Clock buffer		40x50	8.0	Max operation freq. > 4.9 GHz in the worst corner and 85 °C
2:1 Multiplexer		90x90	13.3	Deterministic jitter < 5.6 ps) w/ 8 Gb/s PRBS7 signals in the worst corner and 85 °C
CML driver		700x700	70	Deterministic jitter < 12 ps with 8 Gb/s PRBS7 signals in the worst corner and 85 °C

ASIC design - next steps

- A LC-tank based phase locked loop (PLL) has been implemented and tested in the same single channel ASIC prototype. The upper operation frequency is 5.0 GHz. We need to fine tune the LC VCO to fit the frequency of other slow components.
- Then we will work on the CMOS circuits part and overall timing adjustment.
- So far all the design is based on the GC process (0.25 µm). A faster PC process (0.25 µm feature size with significant improvement on interconnection) will come out in mid 2011, and 180 nm process in the later part of 2011. New irradiation tests will be needed on the new processes. We will need to decide on whether we prototype the GC design or move to the new design.
- The ASIC submission time is planned in early 2012

Conclusion

- A single-channel 5 Gb/s 16:1 serializer ASIC in a commercial 0.25 μm SOS CMOS technology has been developed. Laboratory test indicates that we have achieved the design goals. Irradiation test indicates that the ASIC meets the application requirements.
- A double-channel serializer 16:1 serializer ASIC is under development. Post layout simulation of all fast parts indicates that 8 Gb/s each channel is achievable.