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A high speed serializer ASIC for ATLAS Liquid Argon calorimeter upgrade

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The current front-end electronics of the ATLAS Liquid Argon calorimeters need to be upgraded to sustain the higher radiation levels and data rates expected at the upgraded LHC machine (HL-LHC), which will have 5 times more luminosity than the LHC in its ultimate configuration. This upgrade calls for an optical link system of 100 Gbps per front-end board (FEB). A high speed, low power, radiation tolerant serializer is the critical component in this system. In this paper, we present the design and test results of a single channel 16:1 serializer and the design of a double-channel 16:1 serializer. Both designs are based on a commercial 0.25 μm silicon-on-sapphire CMOS technology.

The single channel serializer consists of a serializing unit, a PLL clock generator and a line driver implemented in current mode logic (CML). The serializing unit multiplexes 16 bit parallel LVDS data into 1-bit width serial CMOS data. The serializing unit is composed of a cascade of 2:1 multiplexing circuits based on static D-flip-flops. The total jitter is measured to be 62 ps at bit error rate (BER) of 10-12 at 5 Gbps. Random and deterministic jitters are measured to be 2.6 ps and 33.4 ps, respectively. The serializer can work from 4.0 to 5.7 Gbps with BER less than 10-12. The power consumption is measured to be 463 mW at 5 Gbps. A proton beam test proves that the serializer meets the radiation tolerant requirements of ATLAS.

A double-channel 16:1 serializer is currently under development. A low jitter LC tank PLL is shared by two serializing units to save the power consumption. The critical high speed components, including clock buffer, divider and the last stage of 2:1 multiplexing unit, are implemented with current mode logic. The post-layout simulation results of these components indicate that 8 Gbps per channel is achievable.

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