TIPP 2011 - 2nd International Conference on Technology and Instrumentation in Particle Physics



Contribution ID: 275

Type: Oral Presentation

System implications of the different powering distributions for the ATLAS Upgrade silicon tracker

Saturday 11 June 2011 14:00 (20 minutes)

The inner tracker of the present ATLAS detector has been designed and developed to function in the environment of the present Large Hadron Collider (LHC). At the next-generation tracking detector proposed for the High Luminosity LHC (HL-LHC), the so-called ATLAS Upgrade, the particle densities and radiation levels will be higher by as much as a factor of ten. The new detectors must be faster, more highly segmented, cover more area, be more resistant to radiation, and require much greater power delivery to the front-end systems. At the same time, they cannot introduce excess material which could undermine performance. For those reasons, the inner tracker of the ATLAS detector must be redesigned and rebuilt completely.

The design of the ATLAS Upgrade tracker has already been defined. It consists of several layers of silicon particle detectors. The most internal layers will be constituted by silicon pixel sensors, and the external layers will be constituted of silicon "short" (~2.5 cm) and "long" (~10 cm) strip sensors. In response to the needs of the strip region for the upgraded tracker, highly modular structures are being studied and developed, called "staves" for the central region (barrel) and "petals" for the forward regions (end-caps). These structures integrate large numbers of sensors and readout electronics (integrated in circuit units called "hybrids"), with precision light weight mechanical elements and cooling structures, and will conform the strips region of the ATLAS upgraded tracker.

The powering scheme used to power the stave and petal modules must address a dramatic decrease in cables and services materials, due to the material budget and the minimal space available for additional services in the upgraded tracker. Two different powering distributions have been proposed for the stave and petal hybrids, hosting the readout and control electronics, and are currently under development by several groups of the ATLAS Upgrade collaboration. One of the options is based on DC-DC conversion, in which one ASIC performs a step-down high voltage conversion of a factor of 4-6 for each hybrid of a stave/petal module, delivering lower voltage, higher currents to the front-end electronics. An additional second-step voltage conversion is also considered in the readout chips. The other proposed scheme is based on serial powering, in which all the hybrids of each stave/petal module are powered in series. The (constant) current of the serial power chain is determined by the current required for each single hybrid, and the voltage is equal to the total voltage required by a single hybrid multiplied by the number of hybrids in the serial chain.

This work consists of a comparison between both powering schemes from the point of view of a stave/petal system. Numerous variables have been taken into account for this study, such as total power dissipation and power efficiency, system reliability and protection, cooling needs, noise performances, impact on the material budget of the tracker, and services needs and re-usability. The study points out the work performed so far concerning the system issues previously mentioned, as well as the advantages, drawbacks, and potential issues of each powering option.

Authors: Dr HABER, Carl (Lawrence Berkeley National Laboratory (LBNL)); Dr DIEZ-CORNELL, Sergio (Lawrence Berkeley National Laboratory (LBNL))

Presenter: Dr DIEZ-CORNELL, Sergio (Lawrence Berkeley National Laboratory (LBNL))

Session Classification: Semiconductor Detectors

Track Classification: Semiconductor Detectors