Semiconductor Detectors Track Overview

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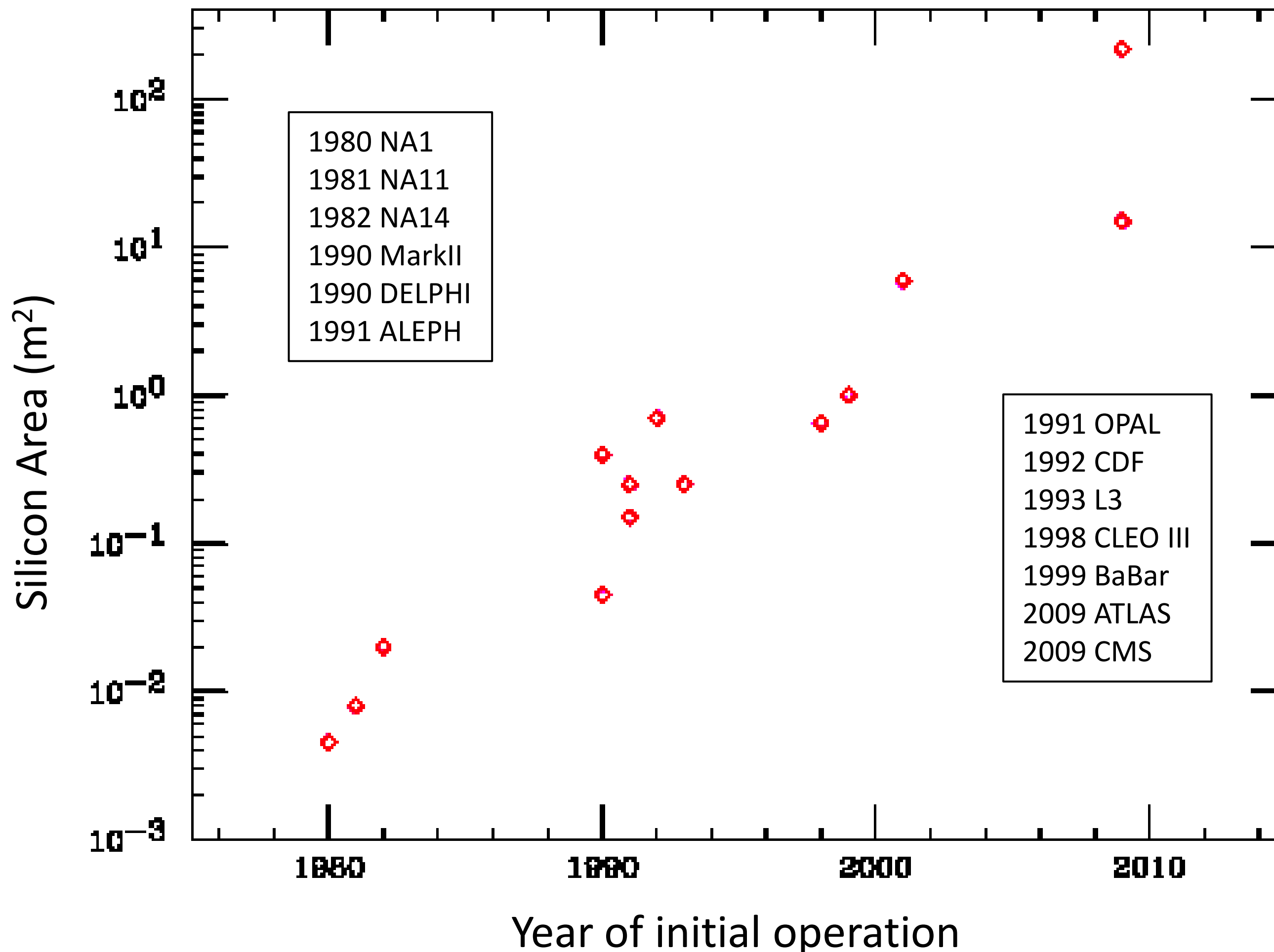
Outline

- History: Why semiconductor detectors?
  - (Concentrating on silicon)
  - Energy Resolution
  - Position Resolution (leverage of IC technology)
- Transition to the present
  - Further leverage of IC technology
    - ASICs
    - Bump Bonding, Micromachining
- Preview of this “track” in TIPP 2011

Transistors/integrated circuit

Exponential improvements of silicon ICs WILL end someday… but when?

Silicon Detectors in HEP (representative selection, appox dates)



Silicon detectors also continue to be improved in surprising ways – size is only one.

Stolen from someone (can't remember who)

Why Semiconductor Detectors? Energy Resolution

- Any energy deposition with E>band gap can create a detectable e-h pair → large number of charge carriers
- Long charge carrier lifetime in (achievable) crystals
- Large number of charge carriers → small statistical fluctuation of the number → good energy resolution

Material	Average energy to create 1 mobile charge carrier (pair)
NaI (gold standard)	>50 eV (per scin. γ – doesn't include detection QE)
Si	3.62 eV (band gap = 1.12 eV)
Ge	2.98 eV (band gap = 0.74 eV)
CdTe	4.43 eV (band gap = 1.47 eV)
Ar	26 eV
Xe	22 eV

(aside) Getting a Signal From Mobile Charges in a Semiconductor Detector

- Many mobile charge carriers are produced by energy deposition in the crystal.
- There must be a region in which an E field exists so that motion of the mobile charge will induce a signal that can be amplified (or charge collected/stored).
- Usually, this is accomplished by creating a volume that is depleted of mobile charge (depletion region) and can therefor support an E field.
  - With a diode junction
  - With an electrode capacitively coupled to the silicon
- Charge can also be collected from region of zero field (if it diffuses to the region of non-zero field)
  - Most CCDs and MAPS have very small depletion regions and collect electrons by diffusion in a thin epitaxial layer (electrons are trapped in the layer by a field at the p/p+ boundary with the substrate)
- E field can also depend on dc current
  - Radiation damaged silicon traps mobile charges produced thermally in the bulk; trapped leakage current produces space charge regions that are large near both sides of the sensor ("double junction" described by a number of authors)
  - Novel MAPS proposed by De Geronimo, et al. (NIM A 568 (2006) 167): applied voltage drives large dc current (composed of holes only) between p implants. Resulting E field helps collect mobile electrons created by particle being detected.

First Development – Nuclear Physics (γ-ray spectroscopy)

- 1959: Gold surface barrier (Si) diode: J.M. McKenzie and D.A. Bromley, Bull. Am. Phys. Soc. 4 (1959) 422.
- 1960's: Development of lithium "drifted" thick detectors: J.H. Elliott, NIM 12 (1961) 60.
  - Start with p-bulk, use lithium to create an n-p junction on one surface, reverse bias the junction at ~150C (in an oven) – lithium diffuses into the bulk making it nearly intrinsic allowing depletion of thick device without breakdown.
  - Detector must always be kept cold (liquid N2) to keep the lithium from drifting out.

Why Semiconductor Detectors? Position Resolution

- High stopping power of silicon → almost all free charge is created within a few microns of the path of a charged particle.
- Silicon IC technology (planar processing) is key
  - Photolithography to create micron-scale features
  - Doping by diffusion and ion implantation
  - SiO_2 passivation
  - J. Kemmer, NIM 169 (1980) 449 and NIM 226 (1984) 89

First use in HEP – Charm Experiments

- 1981 – 1985:
  - CERN NA11 (First planar devices): Home built & with Enertec/Schlumberger… later Eurisys Mesures, now Canberra Eurisys.
  - CERN NA14: Development with Centronic starting in 1981; in 1983 Wilburn & Lucas formed Micron & development continued.
  - Fermilab E653: Established R&D relationship with Hamamatsu in 1981 and contracted with Micron in 1983 (Hamamatsu SSDs with 12.5μ pitch used in 1987).

Breakthrough

- Fermilab E691 (Tagged Photon Experiment):
  - Used NA14-type sensors from Micron.
  - Coupled to working spectrometer, and a high flux tagged photon beam with good duty factor made possible by 800 GeV Tevatron
  - Inclusive trigger (almost min bias) & high rate DAQ
  - First use of massively parallel computer "farm"

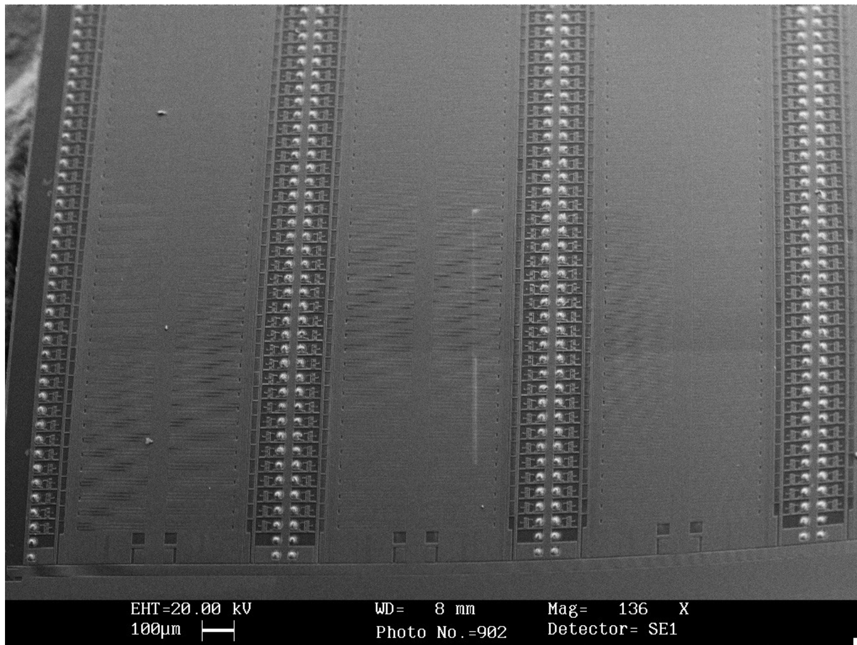
- Yielded definitive measurements of charm particle lifetimes and established silicon detectors as an essential component of the detector builder's "kit."

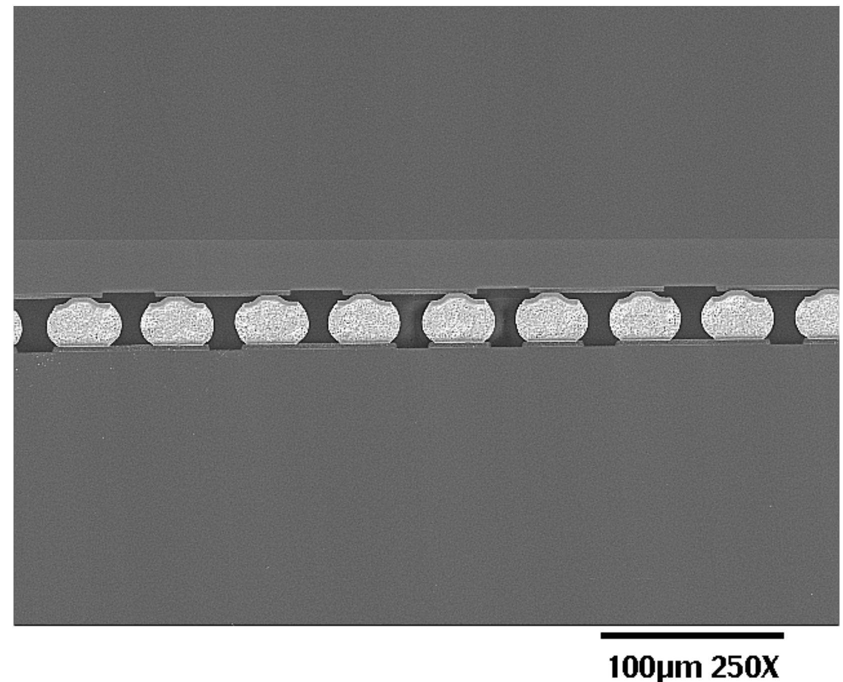
Further use of IC Technology Required by Collider Experiments

- Key enabling technology = ASIC (custom chip)
  - fan out to bulky FE electronics no longer required
- First custom readout chip: MarkII Microplex (1984)
  - LBL design, Stanford fab: 5μ NMOS (single metal, single poly)
- LEP experiments
  - MPI-Munich CAMEX64 (ALEPH), Fraunhofer (Duisburg) fab: 3.5μ CMOS
  - Rutherford Lab (OPAL & DELPHI), Plessy fab: 5μ, then 3μ CMOS
    - Correlated double sampling (reduced noise)
- CDF
  - LBL designed SVX
    - First IC designed for high rate (pedestal subtraction & zero suppressed read out)
    - First HEP ASIC prototyped & produced through MOSIS
- MANY MORE

Further Development Enabled by Use of IC Technology

- Enabling technology for hybrid pixel detectors = bump bonding
  - Now installed in ATLAS, CMS, & ALICE





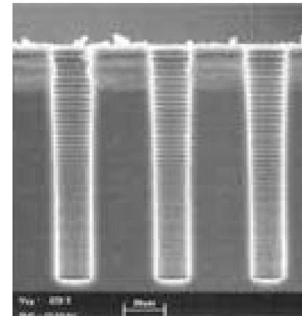
When will it end? Not soon…

- The next high impact enabling technology may be come from the same IC technologies that are enabling a revolution in micromachining (MEMS)
  - Thinning, deep trench etching, through hole vias…
    - 3D sensors
    - 3D ASICs
    - Reduced mass, higher performance, lower cost???

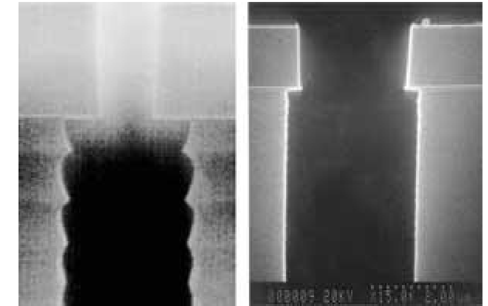
TSV Hole Fabrication Techniques

TSV = Through Silicon Via

- Etching
  - Deep Reactive Ion Etch (DRIE) is used to etch holes in silicon.
    - The most widely used method for forming holes in silicon
    - The process tends to form scalloped holes but can be tuned to give smooth walls.
    - Small diameter holes (1 um) and very high aspect ratio (100:1) holes are possible.
  - Plasma oxide etch is used to form small diameter holes in SOI processes. This process used by MIT LL. [2]
    - Since the hole is in an insulating material, it does not require passivation before filling with conducting material.
  - Wet etching
    - KOH silicon etch give 54.7^{0} wall angle
- Laser Drilling –
  - Used to form larger holes (> 10 um)
  - Can be used to drill thru bond pads and underlining silicon with 7:1 AR
  - Toshiba and Samsung have used laser holes for CMOS imagers and stacked memory devices starting in 2006.

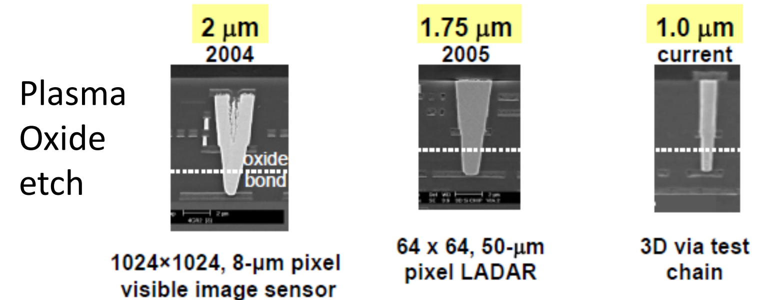


SEM of 3 Bosch process vias [1]

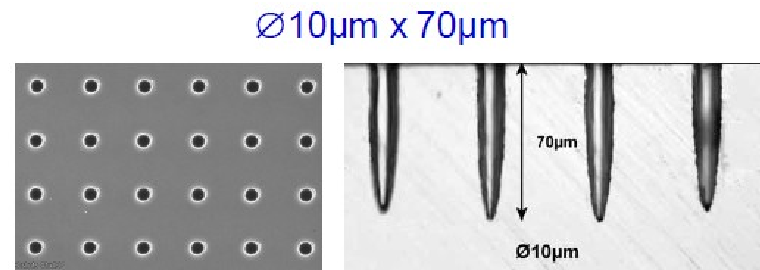


SEM close up of walls with/without scallops in Bosch process [1]

Plasma Oxide etch



∅10µm x 70µm



Laser drilled holes by XSIL [3]

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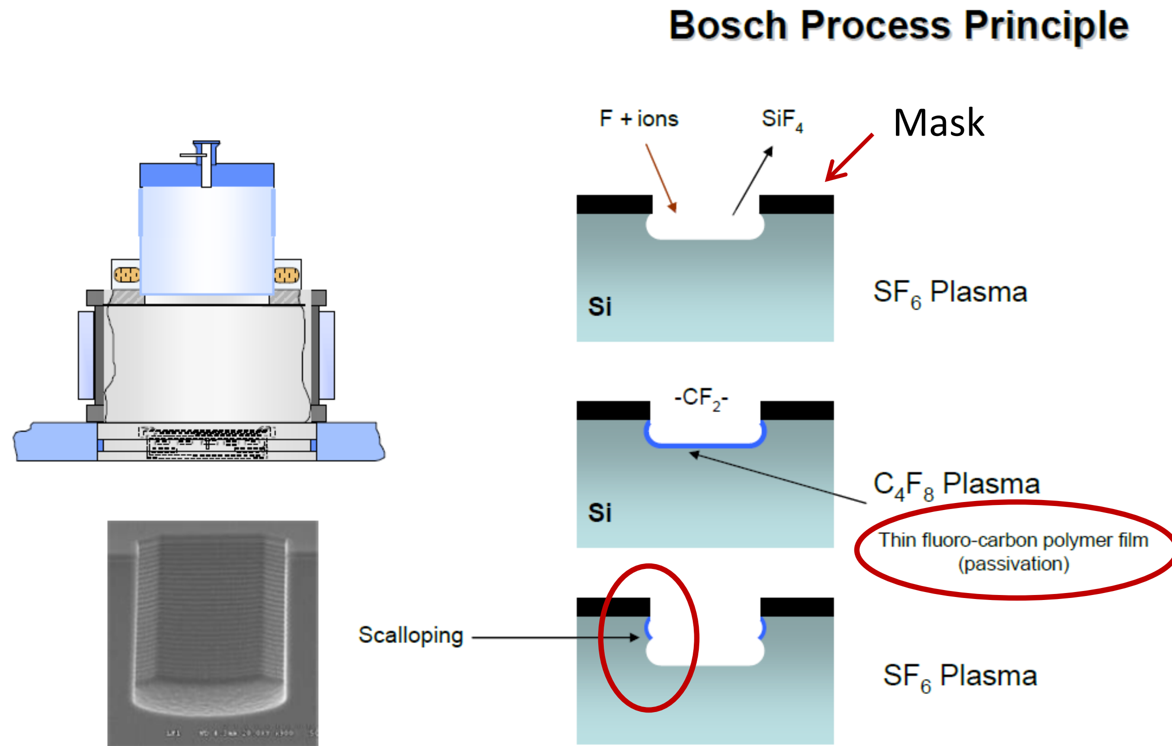
DRIE for Through Silicon Vias [4]

- Holes are formed by rapidly alternating etches with SF_6 and passivation with C_4F_8
- Any size hole is possible (0.1 -800 um)
- Etch rate is sensitive to hole depth and AR (aspect ratio).



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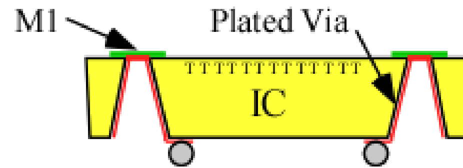
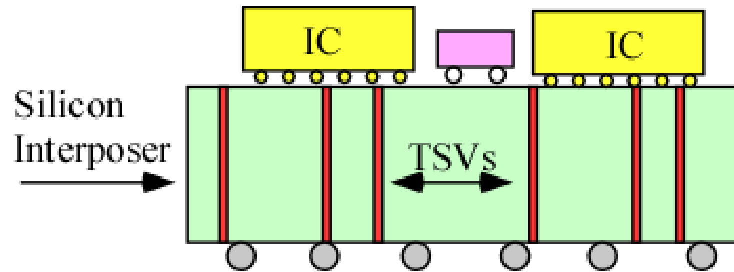
3D Integration Platforms with TSVs

- 3D wafer level packaging
  - Backside contact allows stacking of chips
  - Low cost
  - Small package
- 3D Silicon Interposers (2.5D)
  - Built on blank silicon wafers
  - Provides pitch bridge between IC and substrate
  - Can integrate passives
- 3D Integrated circuits
  - Opens door to multilevel high density vertical integration
  - Shortest interconnect paths
  - Thermal management issues

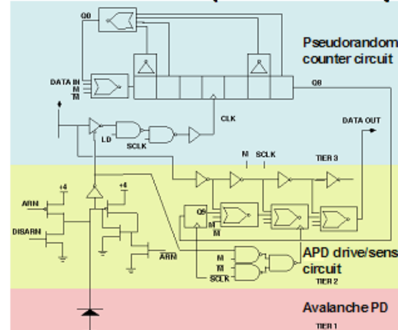


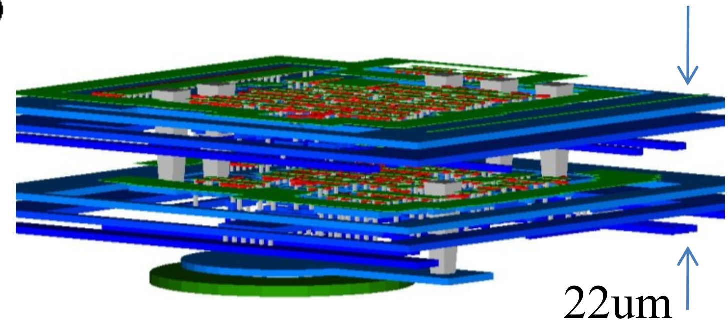
3D Wafer level package



3D Silicon interposer

VISA APD Pixel Circuit (~250 transistors/pixel)





MIT LL 3D integrated APD Pixel Circuit [8]

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3D Sensors in HEP

- First developed by Parker & Kenny
- Current development in the context of RD50 (http://rd50.web.cern.ch/rd50/)
  - Barcelona, Bari, BNL, Bucharest, CERN, Dortmund, Erfurt, Fermilab, Florence, Freiburg, Glasgow, Hamburg, Helsinki HIP, Ioffe, ITE, ITME, Karlsruhe, KINR, Lappeenranta, Liverpool, Ljubljana, Louvain, Minsk, Montreal, Moscow ITEP, Munich, New Mexico, Nikhef, NIMP Bucharest-Magu, Oslo, Padova, Perugia, Pisa, Prague Academy, Prague Charles, Prague CTU, PSI, Purdue, Rochester, Santa Cruz, Santander, SINTEF, Syracuse, Tel Aviv, Trento, Valencia, Vilnius

3D ICs in HEP

- 3D Consortium (http://3dic.fnal.gov)
  - CPPM, IPHC, LAL, LPNHE, IRFU, CMP, Bergamo, Pavia, Perugia, Sherbrooke, INFN (Bologna, Pisa, Rome) Bonn, AGH, Fermilab
- Multi-Project Wafer service now offered by MOSIS, CMP, and CMC (US, Europe, Canada)

Semiconductor Detector Track Preview (1)

- Reports on the performance of current generation detectors (and lessons learned)
  - Large (enormous) scale LHC systems
  - Long term experience from CDF & D0
    - Clear exposition of double junction resulting from radiation damage

Semiconductor Detector Track Preview (2)

- Developments driven by need for mass minimization & position resolution
  - First HEP use of DEPFETs (BELLE-II)
    - Also first use of novel thinned silicon structures integrating sensor and support structure

Semiconductor Detector Track Preview (3)

- R&D to meet SLHC radiation tolerance requirements
  - Talks from all LHC experiments
  - 3D silicon
  - Diamonds

Conclusion

- Semiconductor detectors first used more than 50 years ago.
- Became ubiquitous in HEP more than 30 years ago.
- But new developments continue to extend their reach… and promise to continue to do so for years.
- Welcome to the TIPP 2011 Semiconductor Detector Track!