SLID-ICV Vertical Integration Technology for the ATLAS Pixel Upgrades

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Benefits of vertical integration technology for HEP

Multi-tier ASIC

→ Functionalities splitting

→ Reduction in pixel size

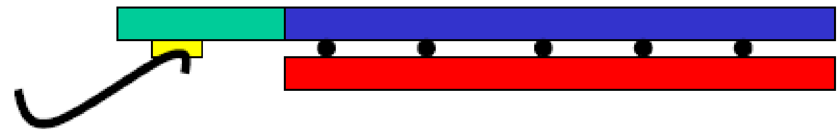
Thin sensor and ASIC → Material budget reduction

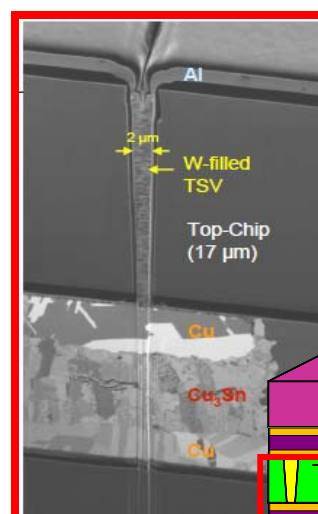
4-side buttable ASIC

↓

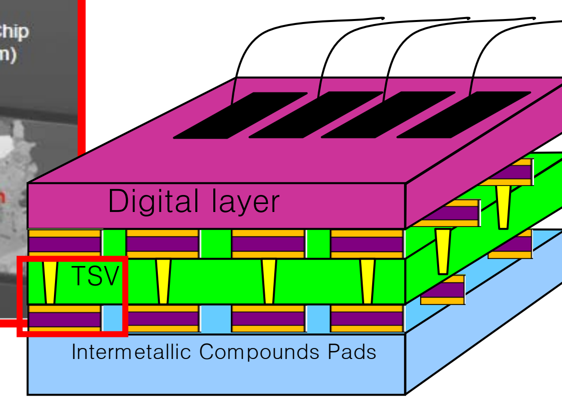
Larger fraction of active area

Standard hybrid pixel module with bump-bonding



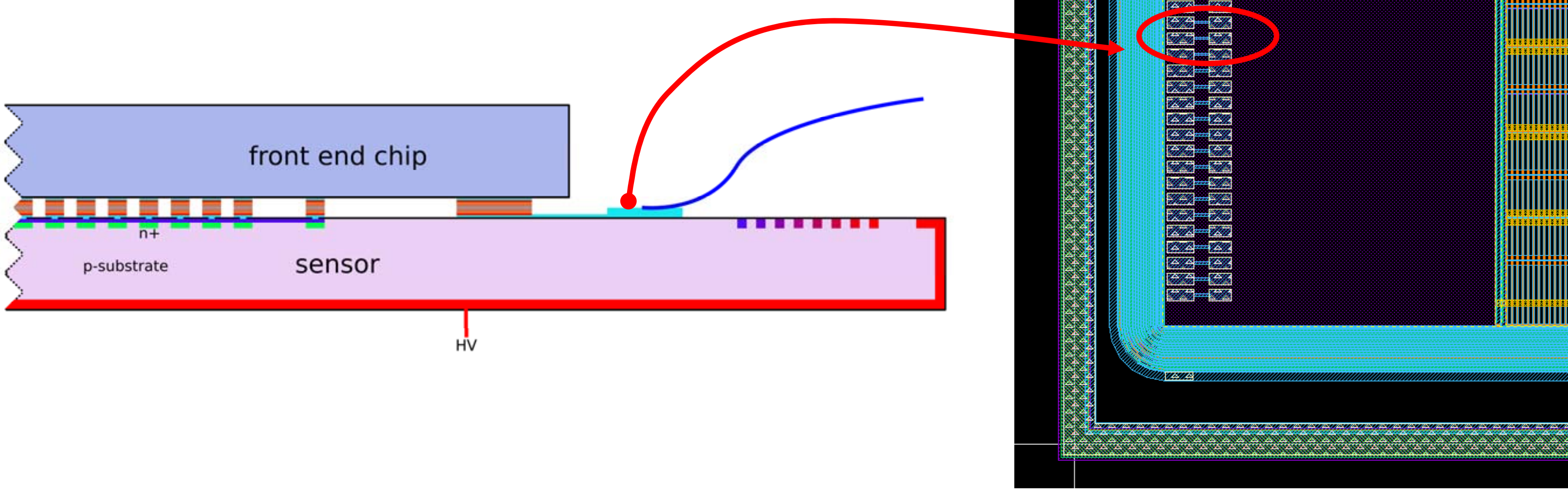


Fraunhofer EMFT



MPP 3D R&D Program: demonstrator module

- Step I:
  - ASIC thinned to 200 µm
  - n-in-p pixel sensors of 75 µm active thickness
  - thin sensors / ASIC interconnection using SLID
  - No TSV, integrated fan-out on sensor for service connection
- Step II:
  - TSV etched in the read-out chip on the front-side on every wire bonding pad to route signal and services to the ASIC backside
  - ASIC thinned to 50 µm
  - thin sensors /ASIC interconnection using SLID



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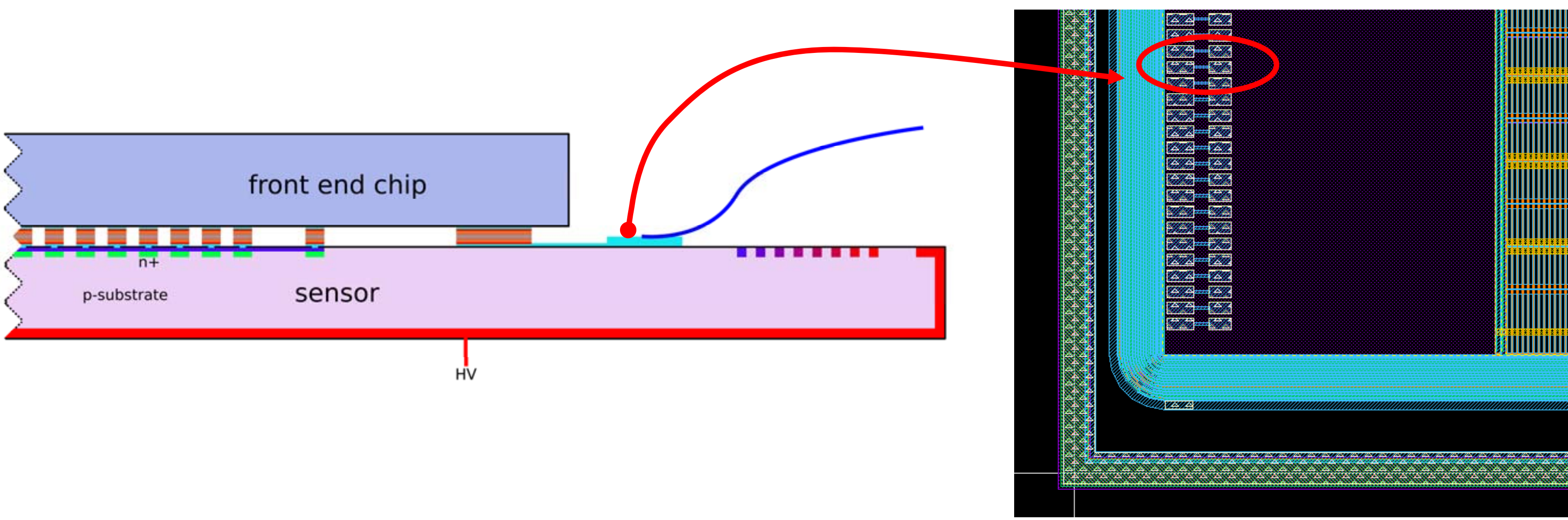

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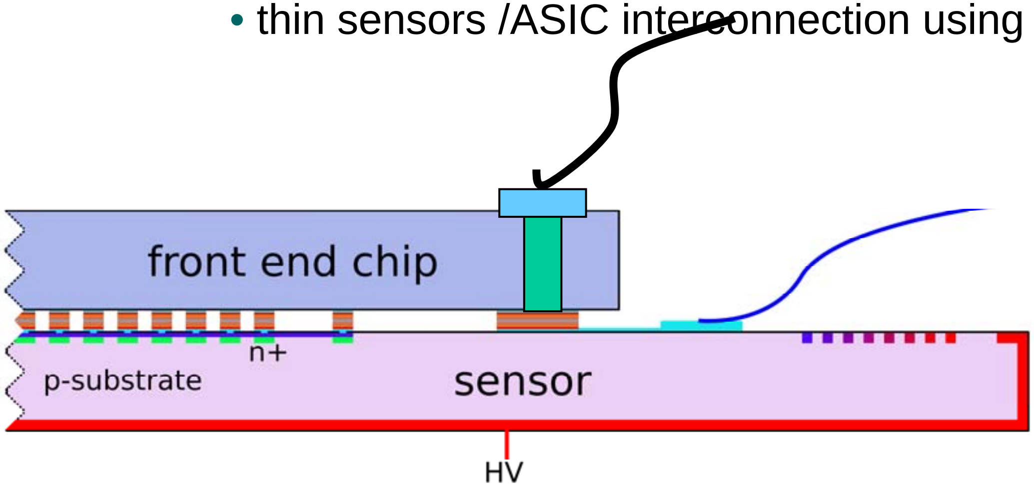
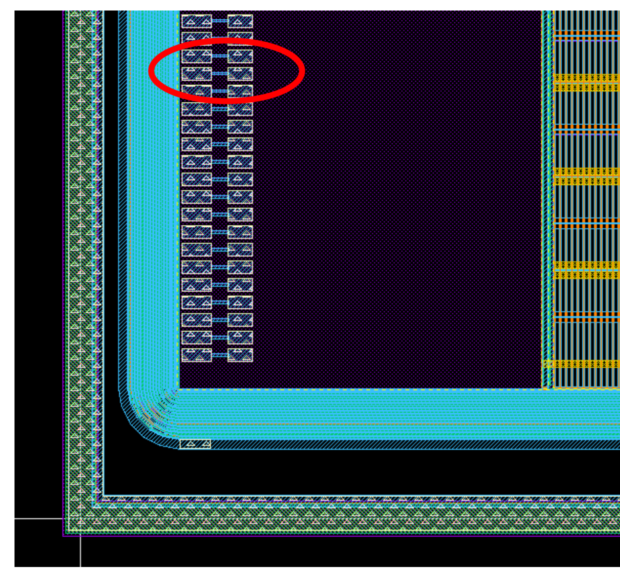


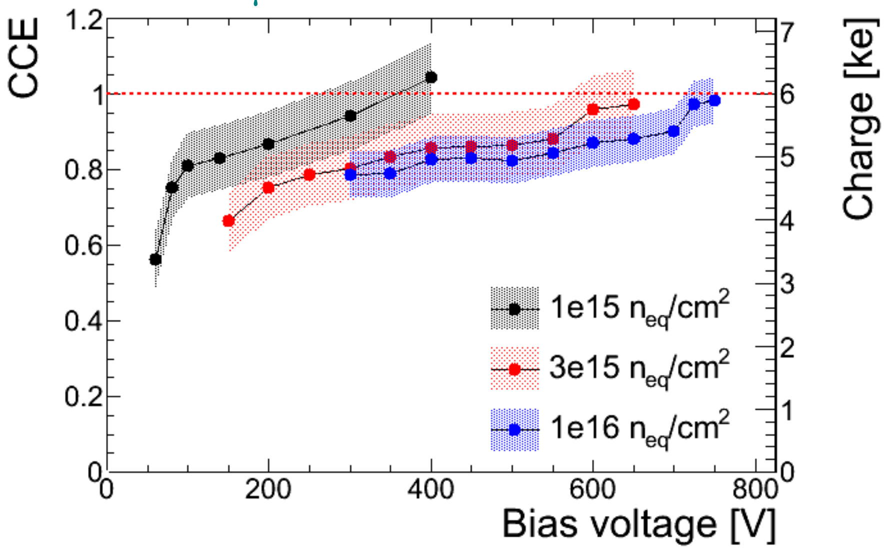


Thin pixels for the ATLAS pixel Upgrade

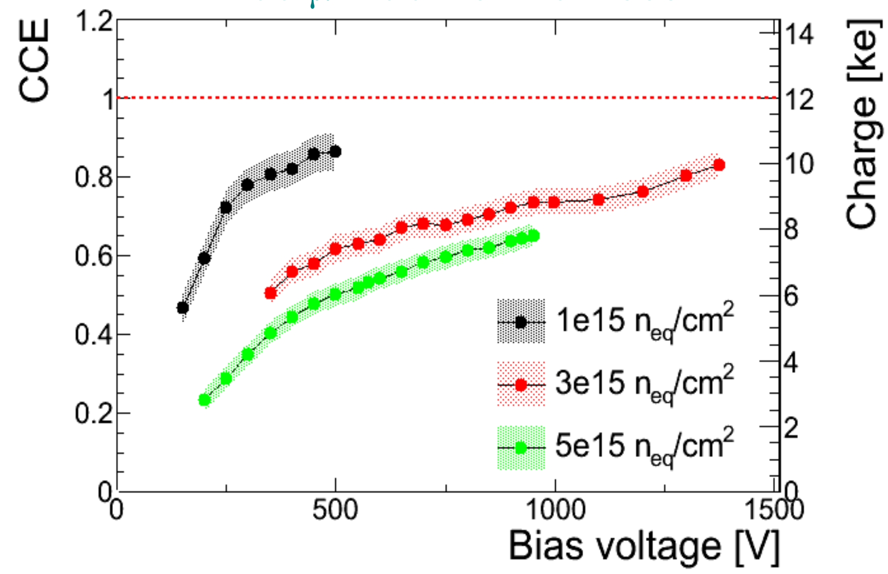
- ATLAS pixel system for the Phase 2 Upgrade: In the inner layers radiation doses of 1-2x10^{16} n_{eq}/cm^2 are foreseen
- Higher electric fields in thinner devices at equal V_{bias} : at HL-LHC fluences higher CCE is expected (larger drift velocity, charge multiplication)
- Minimize material and multiple scattering

Charge collection efficiency measured with thin p-type strip sensors produced by MPP-HLL – Alibava read-out system

75 μm active thickness

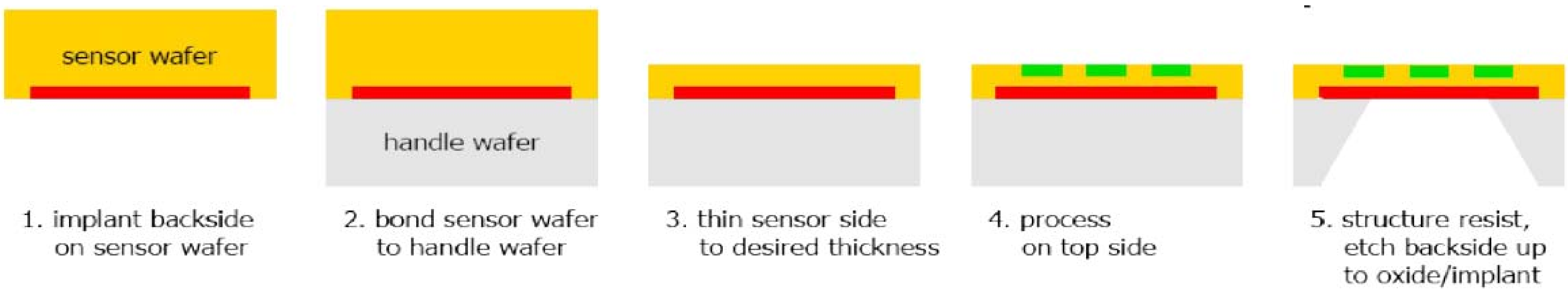


150 μm active thickness

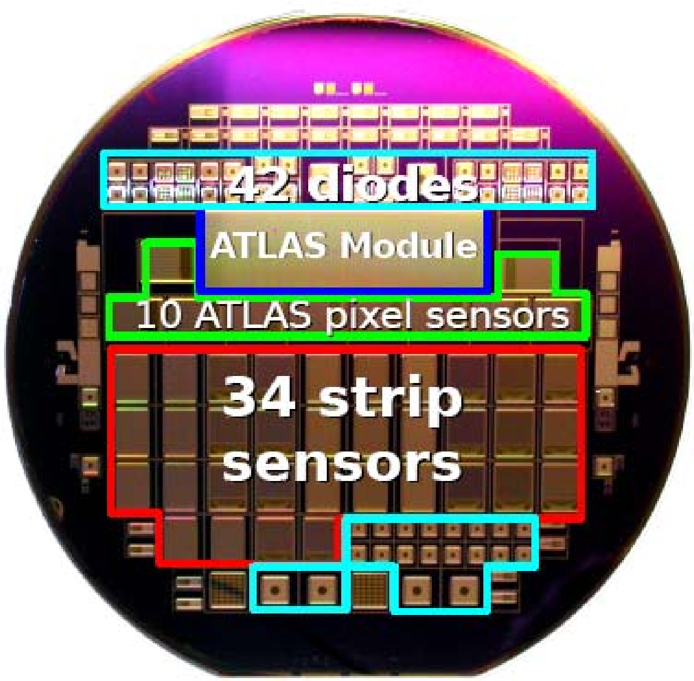


A. Macchiolo et al. http://dx.doi.org/10.1016/j.nima.2010.11.163

Sensor thinning technology at MPP-HLL



- The process has been completed including step #4. The handle wafer has been used as a support during the ASIC interconnection phase. Backside etching demonstrated in other productions



- Production characteristics:
  - 8 n-in-p 6" wafers with ATLAS FE-I3 compatible sensors
  - Different active thicknesses: 75µm and 150µm
  - Pre-irradiation characterization:
    - Excellent device yield (79/80)
    - Low currents (~10 nA /cm^2)
    - Good breakdown behaviour (V_{bd} >>V_{fd})

L. Andricek et al., doi:10.1016/j.nima.2010.04.087

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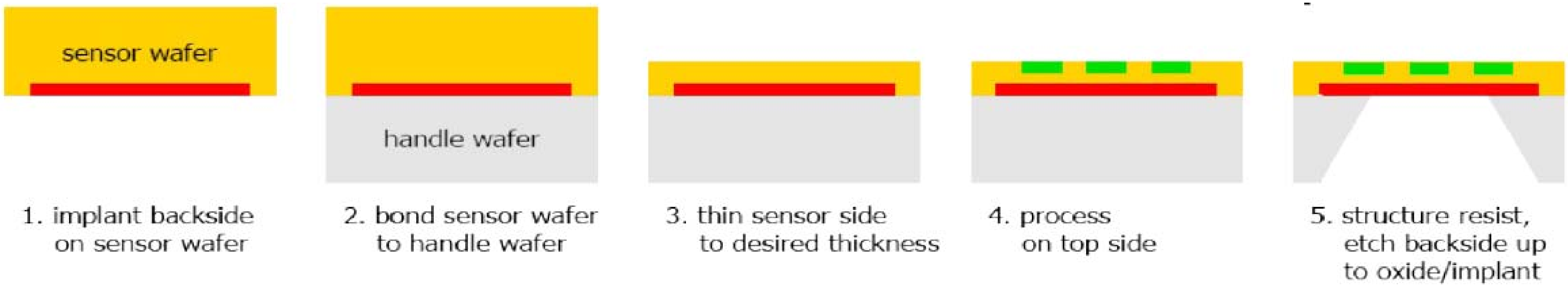

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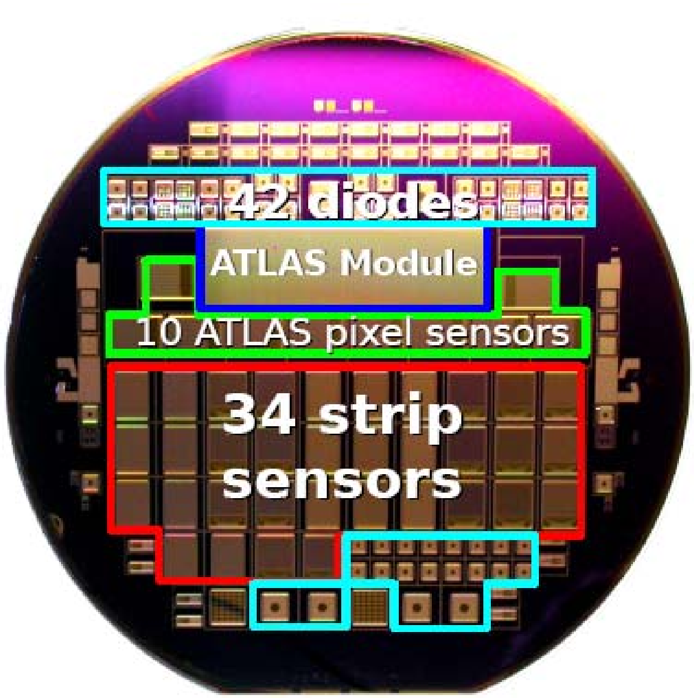
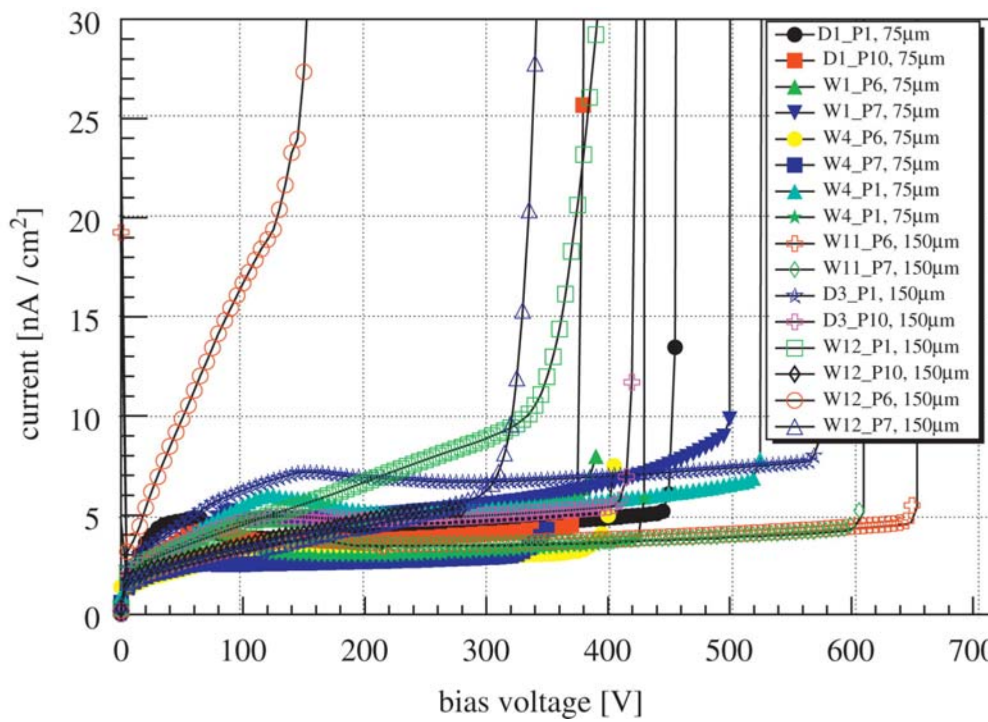
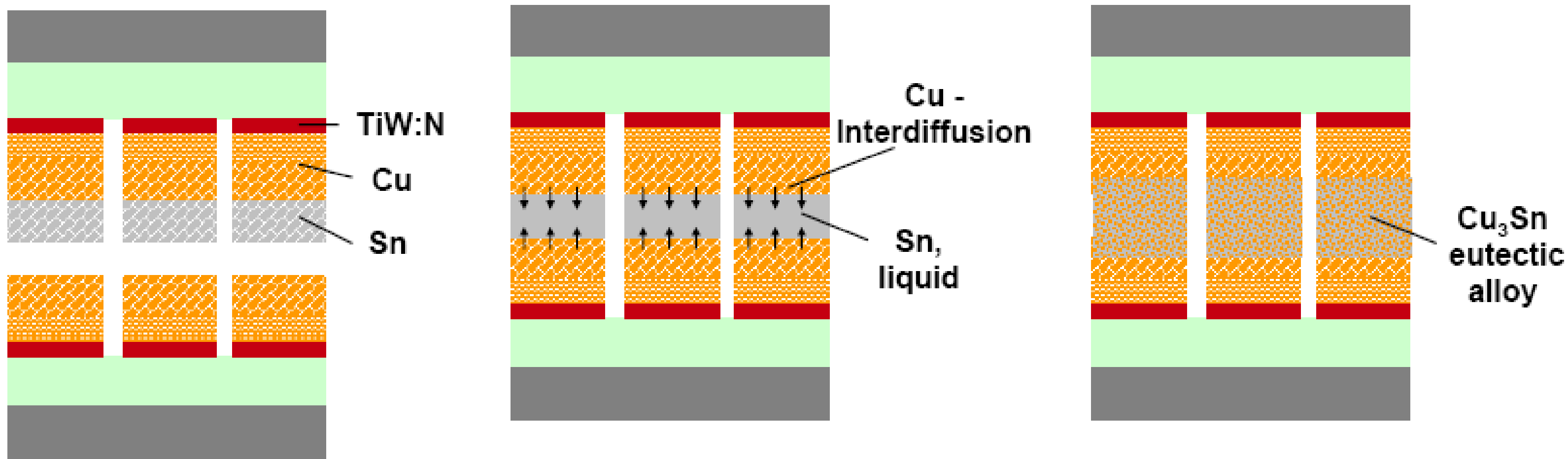




EMFT SLID Process

Metallization SLID (Solid Liquid Interdiffusion)



Through Mask Electroplating

Contact under Pressure and Heat
~ 5 bar, 260 – 300 °C (Sn-melt)

Formation of Eutectic Alloy;
T_{melt} > 600 °C

- Alternative to bump bonding (less process steps "lower cost" (EMFT)).
- Small pitch possible (~ 20 µm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

- However: no rework possible.

Fraunhofer EMFT

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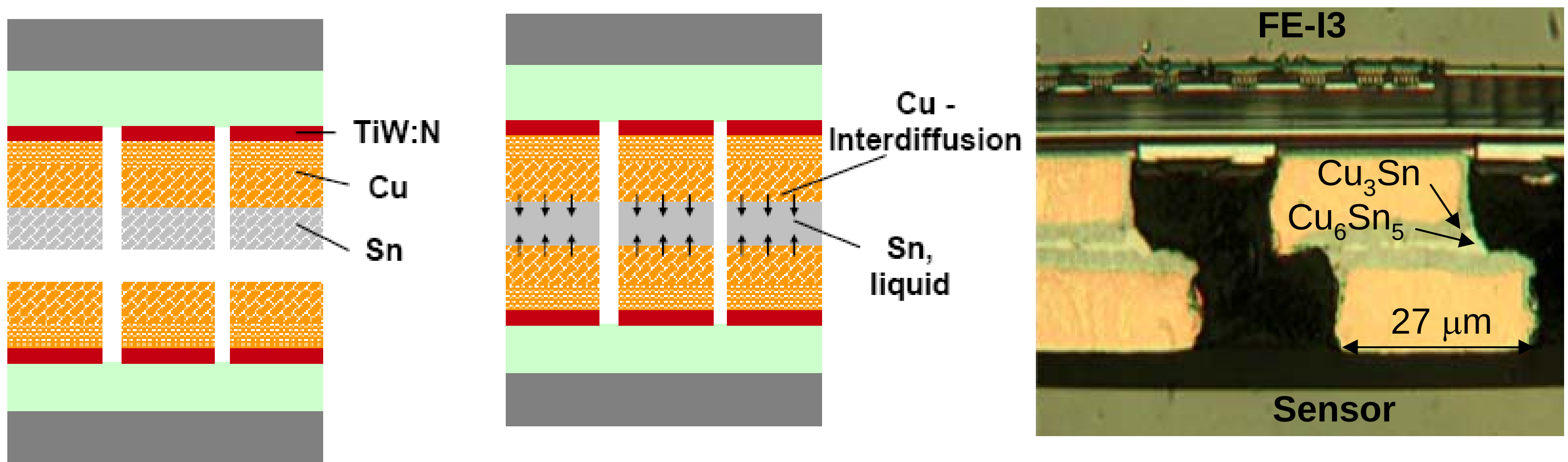

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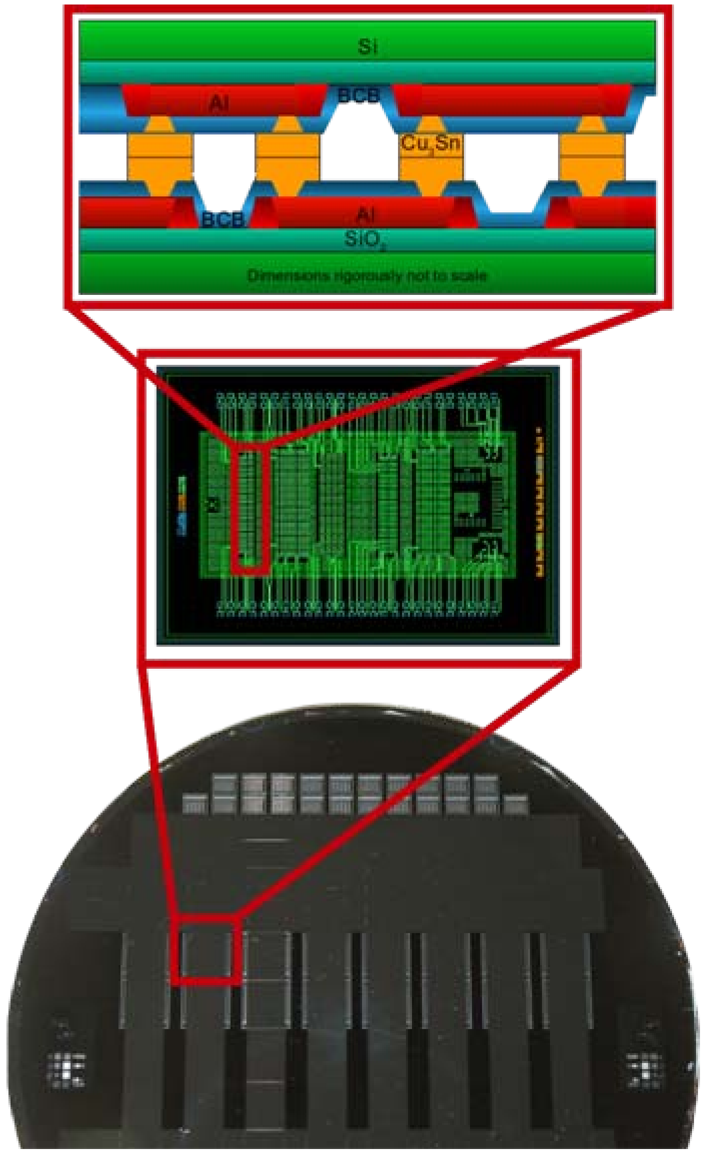
Daisy chains: wafer-to-wafer SLID



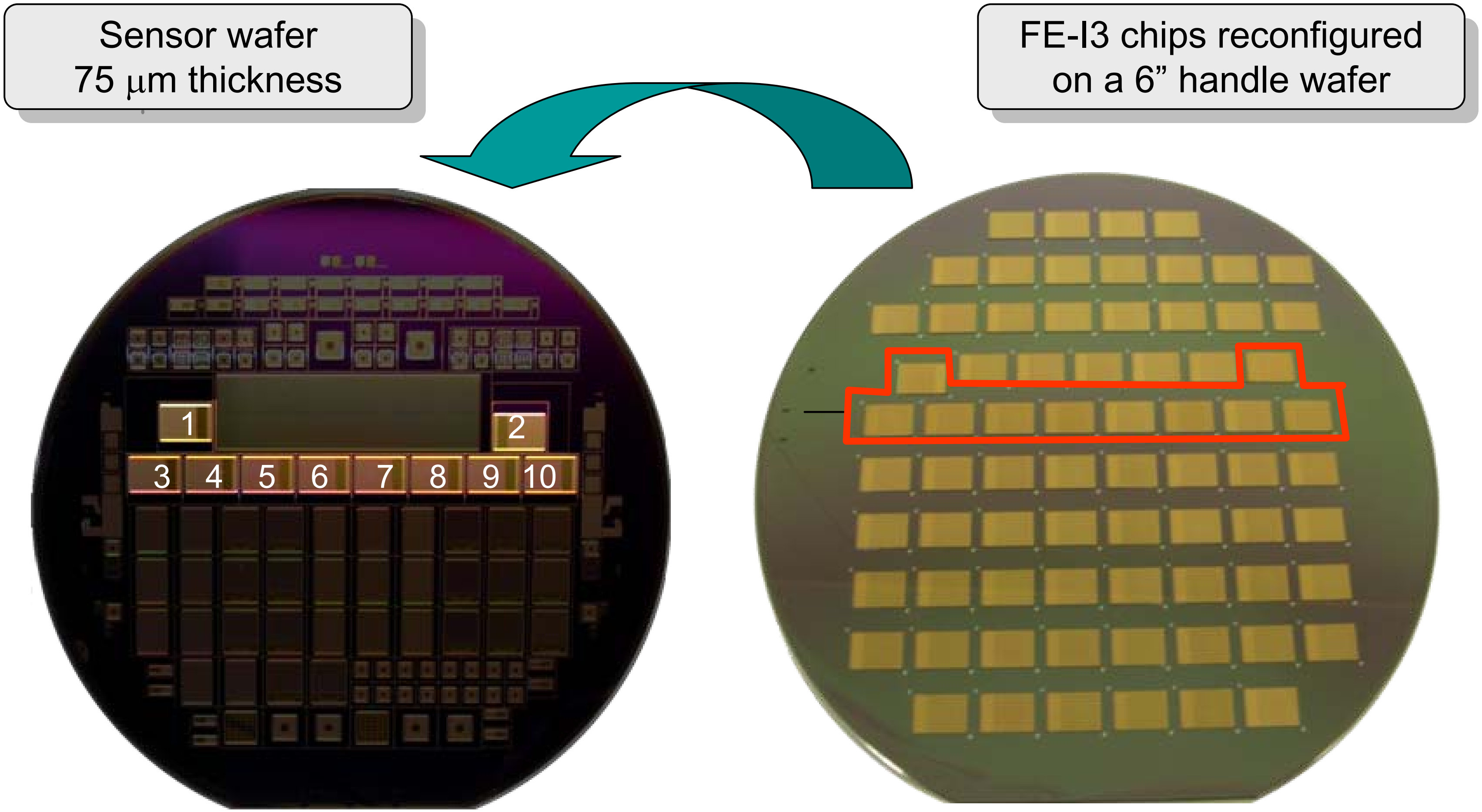
- Aim: determine the feasibility of the SLID inter-connection within the parameters we need for the ATLAS pixels.

- SLID efficiencies measured with daisy chains structures (wafer to wafer connections).

Pad width [μm²]	Pitch [μm]	Aplanarity	SLID Inefficiency
30x30	60	0	$<1.2\times10^{-4}$
80x80	115	0	$<8.9\times10^{-4}$
80x80	100	0	$<7.8\times10^{-4}$
27x60	50,400	0	$(5\pm1)\ \times10^{-4}$
30x30	60	100 nm	$(10\pm4)\times10^{-4}$
30x30	60	1 μm	$(4\pm3)\ \times10^{-4}$

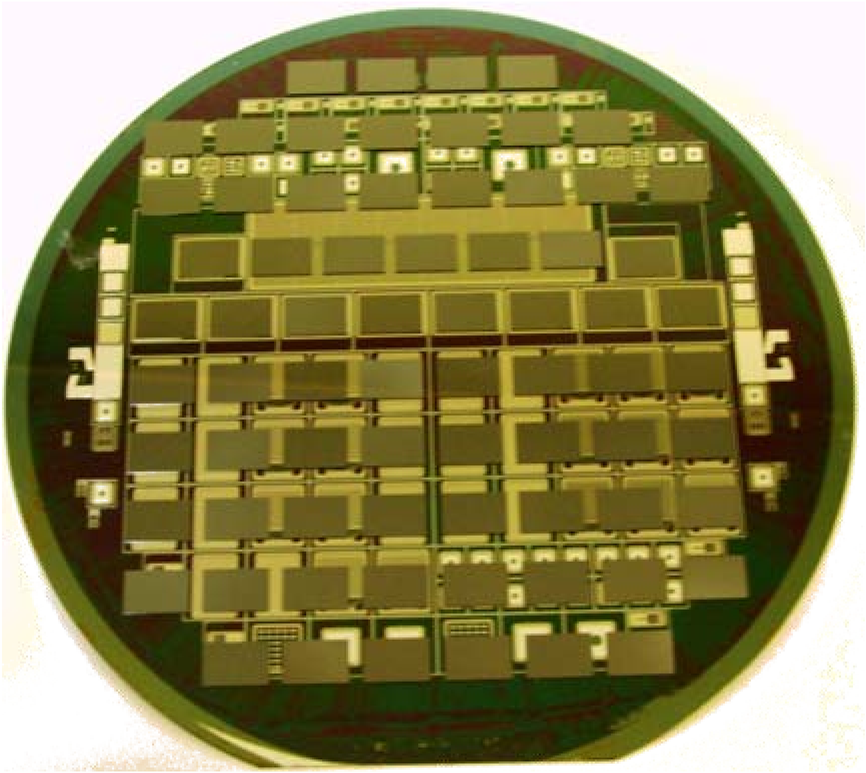
A. Macchiolo et al. “Application of a new interconnection technology for the ATLAS pixel upgrade at SLHC“
http://cdsweb.cern.ch/record/1234896/files/p216.pdf

Chip to wafer SLID interconnection (with handle wafer)



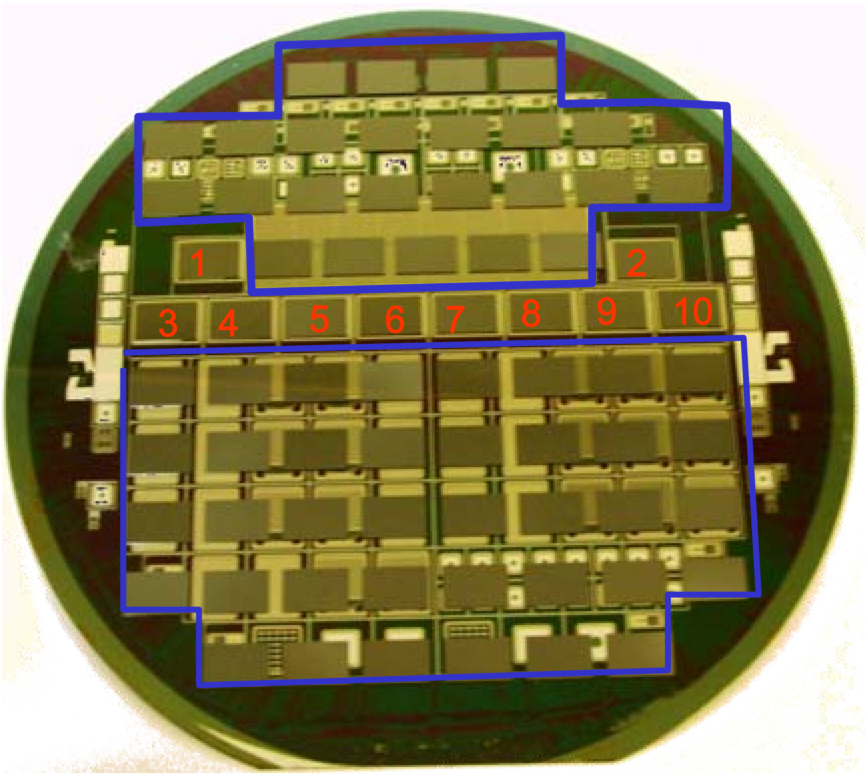
The chips on the handle wafer suffer from strong misalignment with respect to the nominal positions.

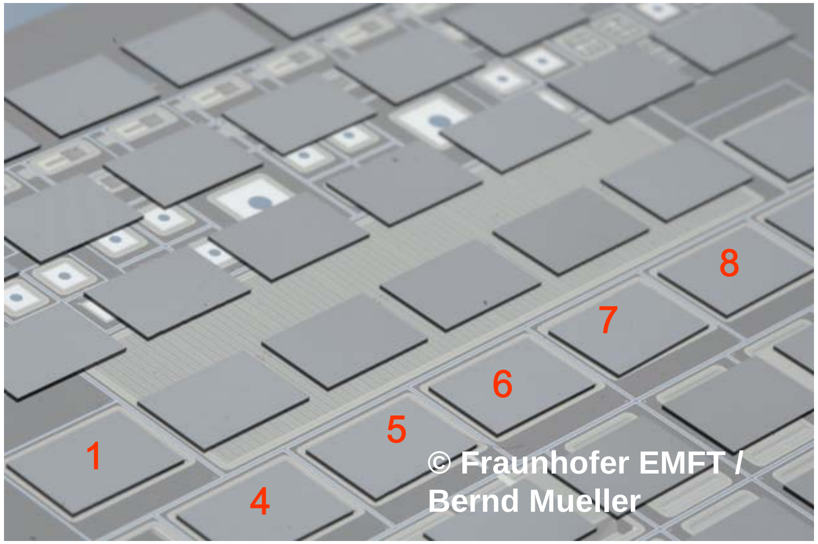
Chip to wafer SLID interconnection (with handle wafer)



After SLID interconnection and handle wafer removal

Chip to wafer SLID interconnection (with handle wafer)





FE-I3 chips (mostly not electrically functioning) used to improve the pressure homogeneity on the wafer during the SLID interconnection

Measured misalignment

1 ★

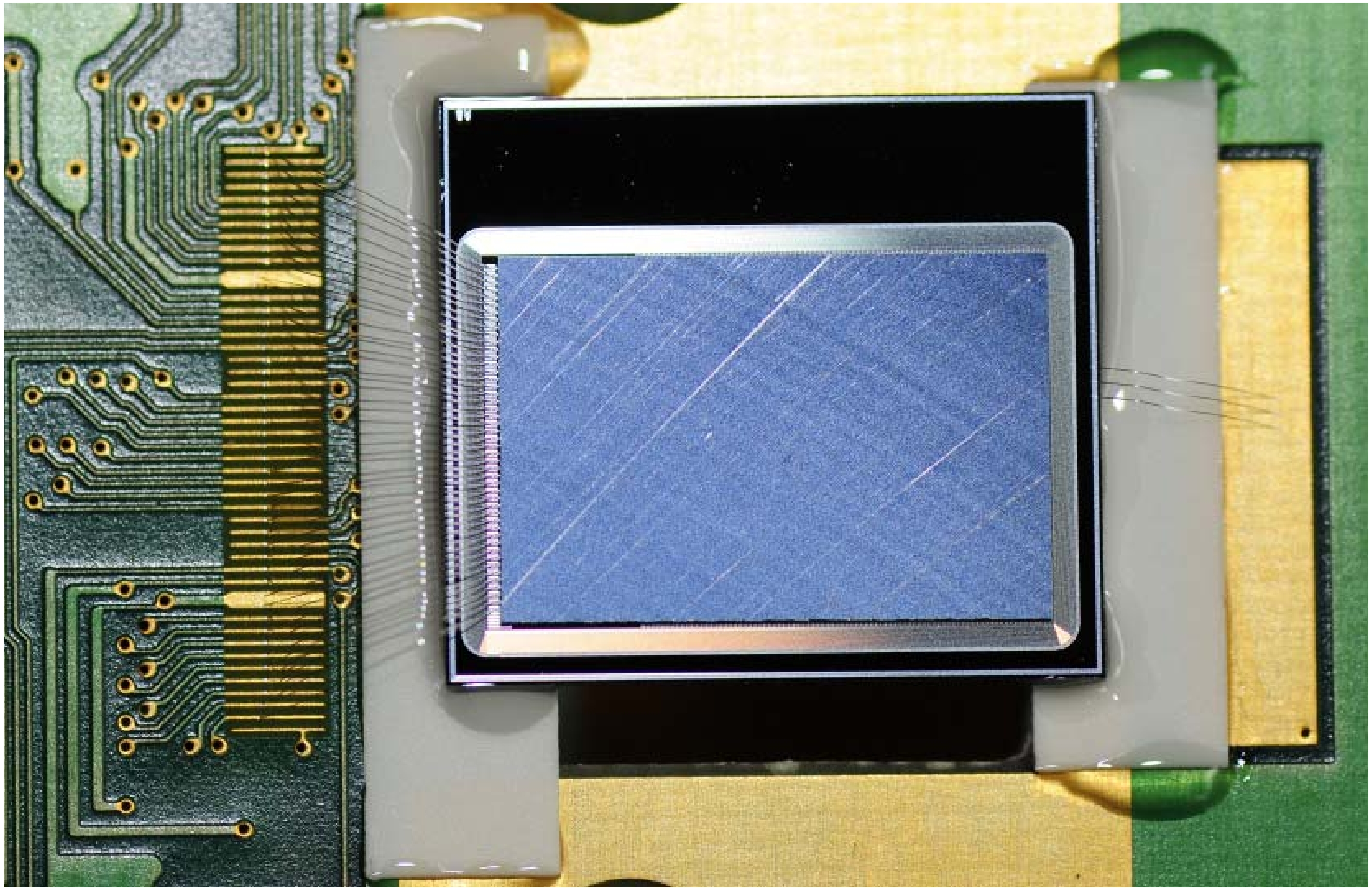
Residual misalignment in ★ after correction for a global offset of the FE-I3 chips

Chip	3	4	5	6	7	8	9	10	Pad size	Distance
Δx [μm]	-23	44	-34	-8	-16	-17	-17	-16	27	23
Δy[μm]	-34	73	-58	-19	-18	-25	-21	-25	60	29
Tilt [º]	-0.38	0.72	-0.61	-0.21	-0.21	-0.23	-0.24	-0.26		

- 5 modules with a misalignment and tilt that do not induce shorts or open, included the area in the corners
- Very good alignment for the SLID pads in the central region of the FE-I3 matrix

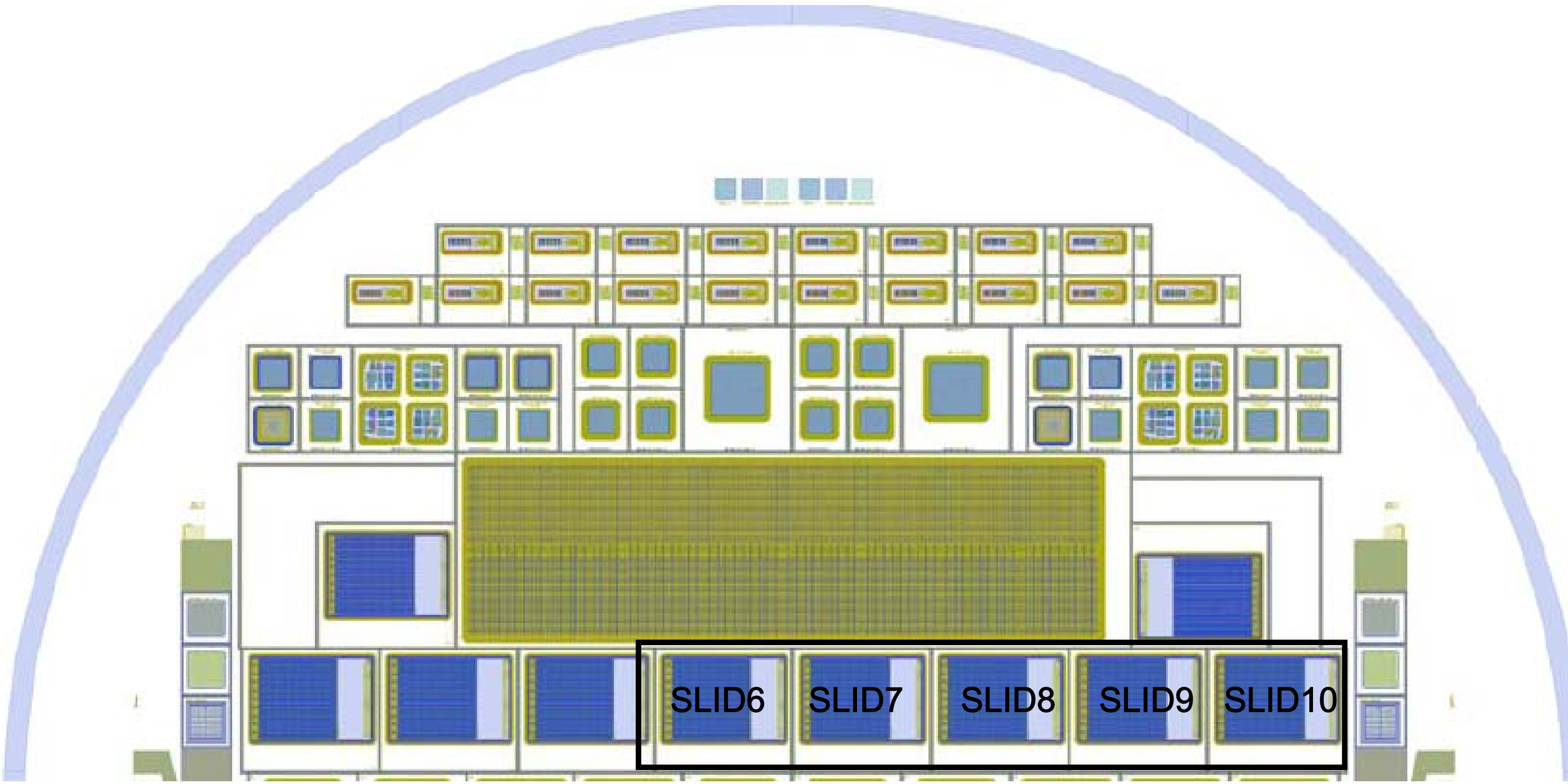
SLID Module measurements

- SLID modules glued and wire-bonded to a modified version of the ATLAS pixel detector board (Bonn University)
- Measurements performed with the ATLAS USBPix read-out system



Overview of the 5 SLID modules tested

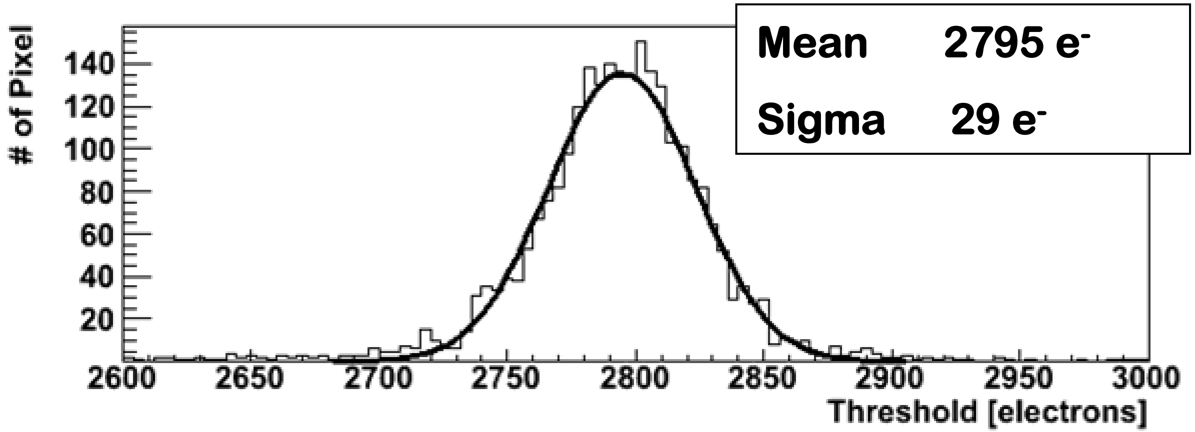
- The five sensors and the chips are all functional
- Chips can be tuned with a small threshold dispersion (except SLID7)
- Leakage current at 50 V ~ 25 nA (above Vdepl=40V)
- ^{90}Sr source scan performed for all the modules



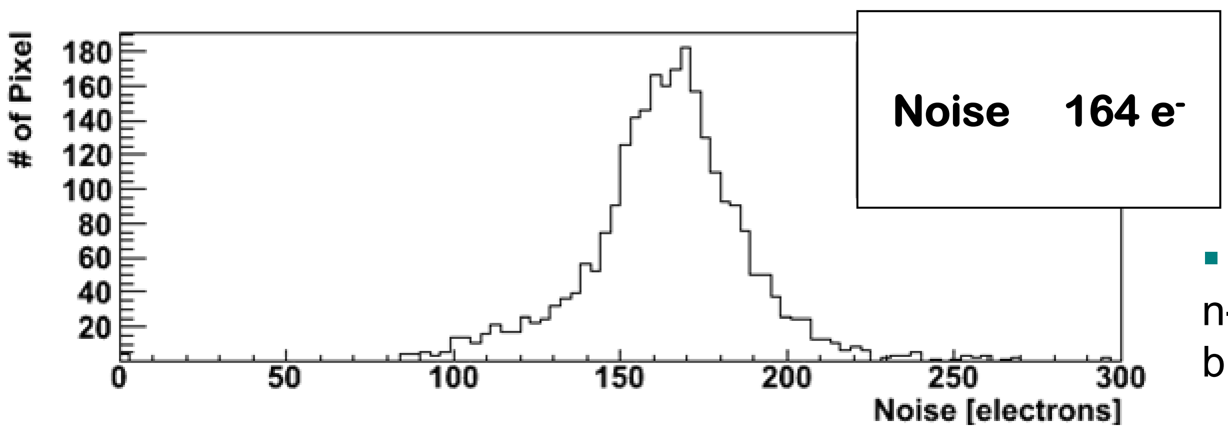
Modules tested

Tuning of Module SLID10

Threshold tuned to 2800 e-

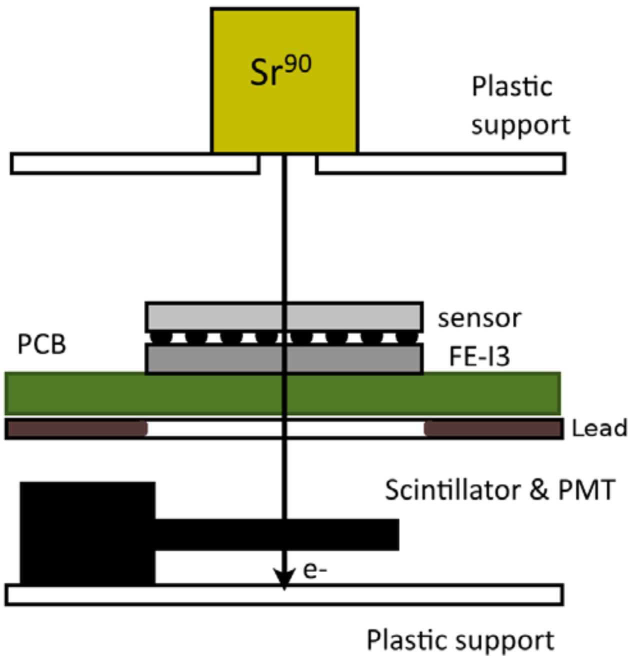


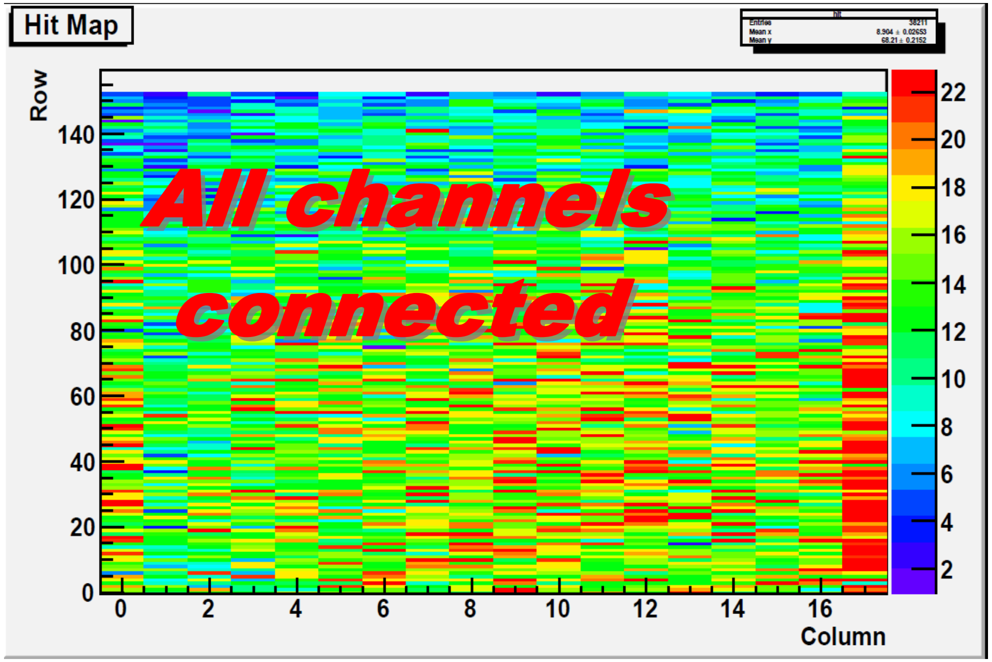
- Modules can be tuned with a small threshold dispersion in the range 2500-3500 e-

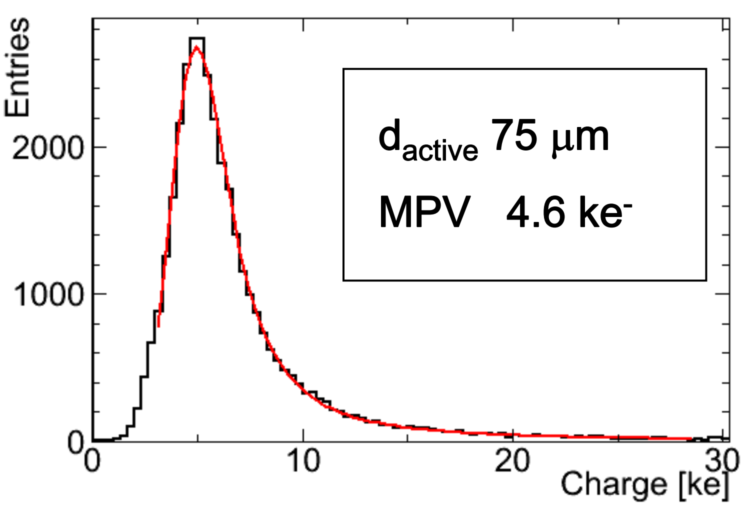


- Noise value comparable to n-in-p SCMs connected by bump-bonding (~170-190 e^-)

SLID Module 10: ^{90}Sr Source Scan



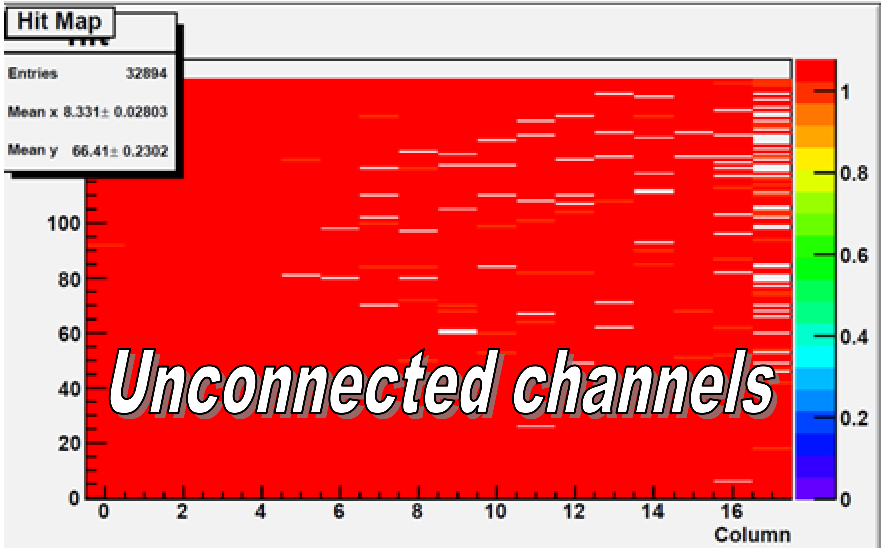


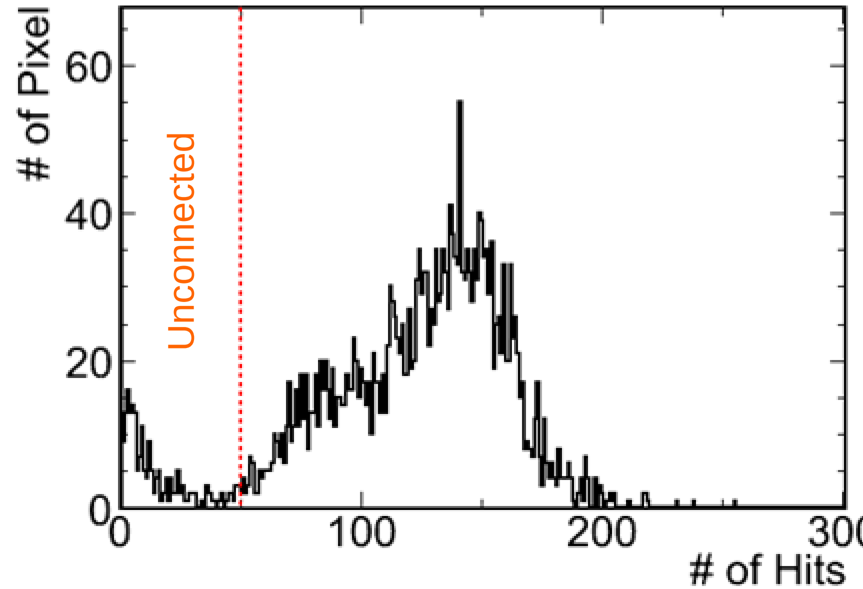


- All channels connected and functional

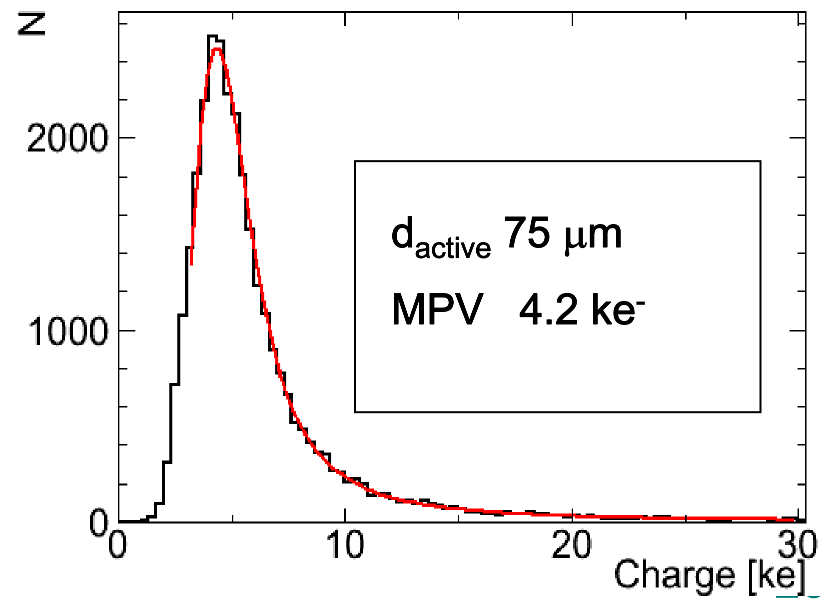
- Collected Charge with ^{90}Sr: compatible with the signal from bump-bonded n-in-p module, 300 um thick, after scaling for the active thickness

SLID Module 9: Charge Collection

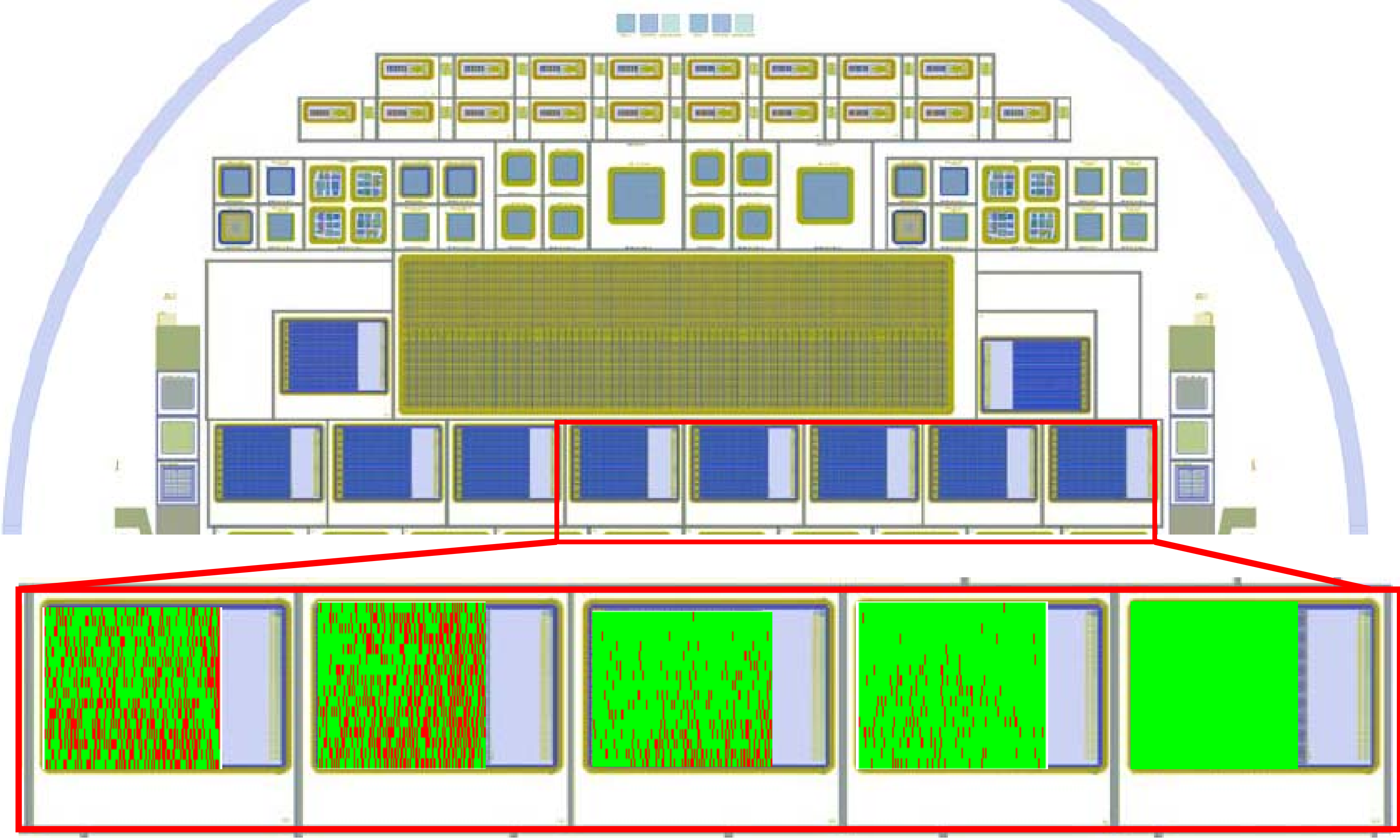




- Number of unconnected channels ~ 6%
- The module is fully functional except for the fraction of disconnected channel
- Similar results for SLID8-SLID7-SLID6 with an increasing number of unconnected channels.



Overview of the SLID interconnection efficiency



Connected channel

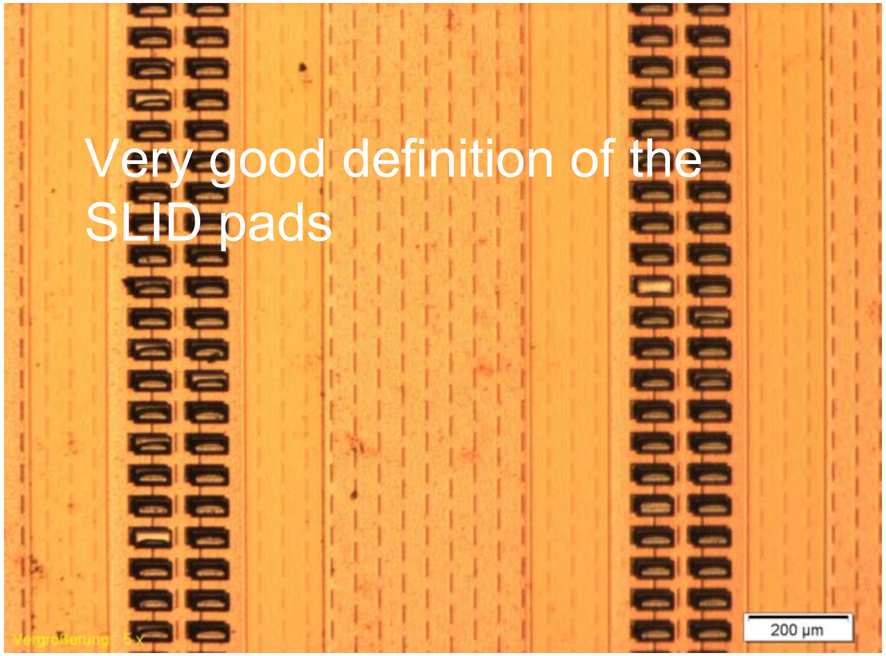
Not connected channel

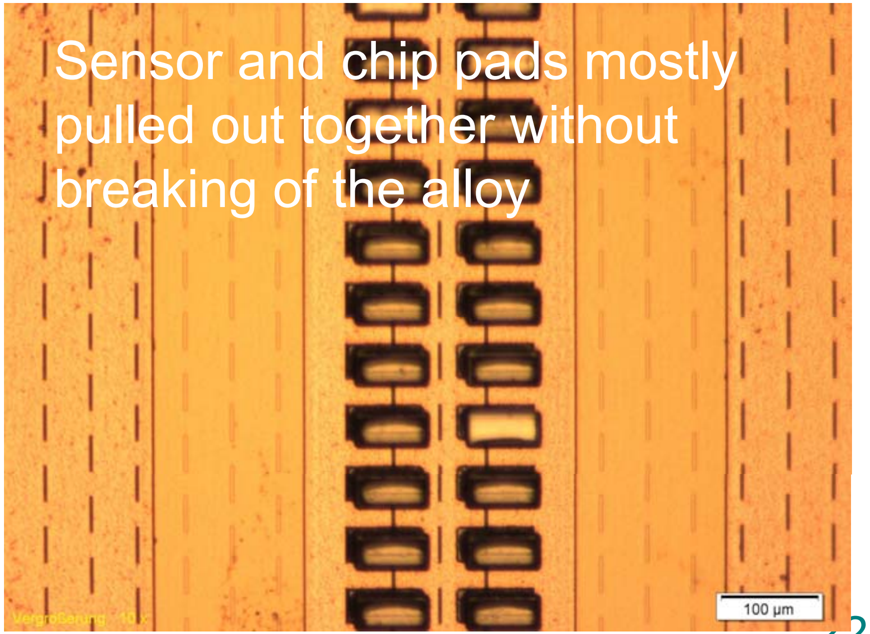
Observations about the disconnected channels

Chip	Discon. Pixel	%
6	731	30
7	713	29
8	274	11
9	134	6
10	0	

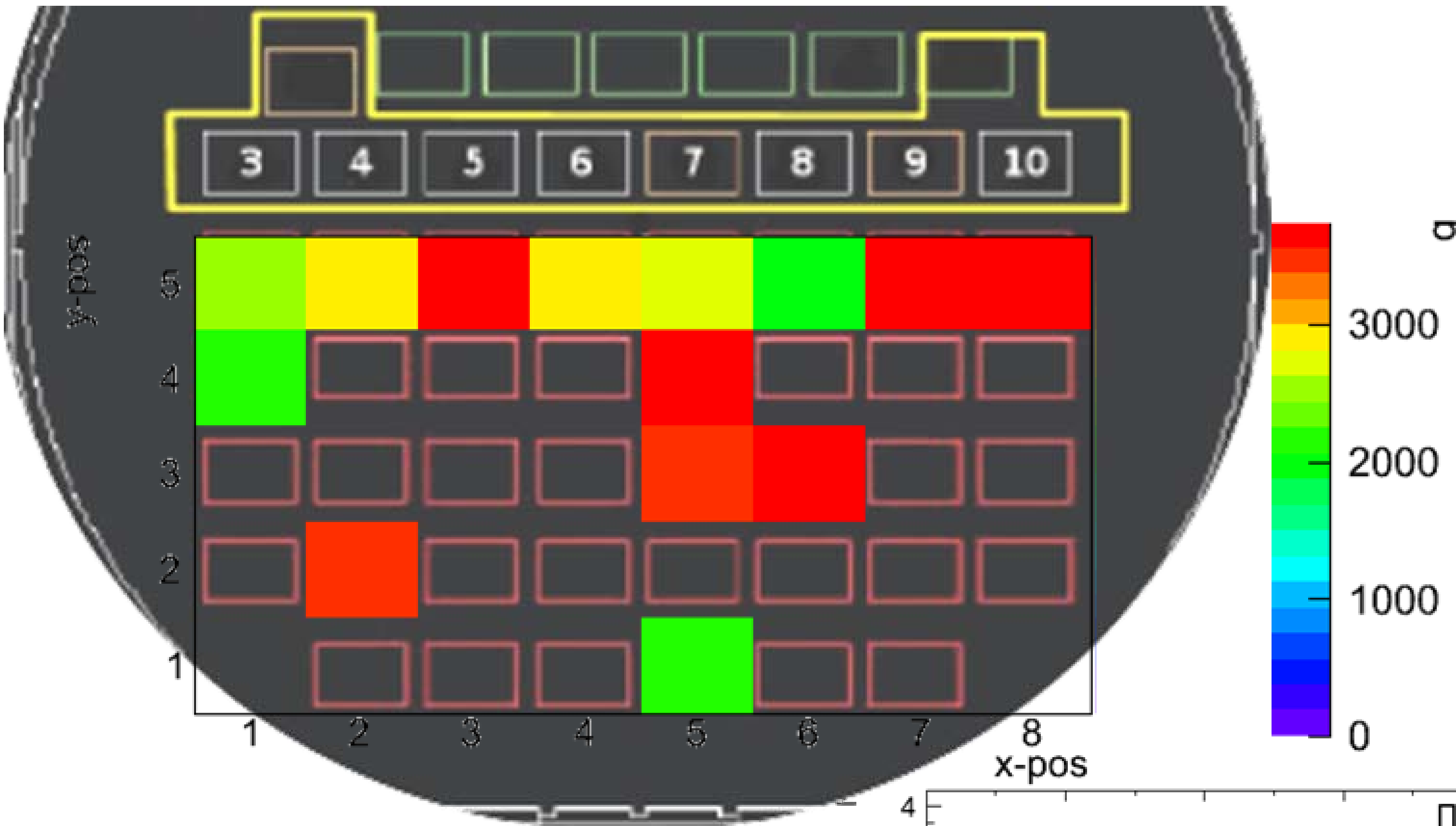
- Number of disconnected channel growing towards the center of the wafer
- Pattern of disconnected channels shows that the chip misalignment cannot be the only cause.

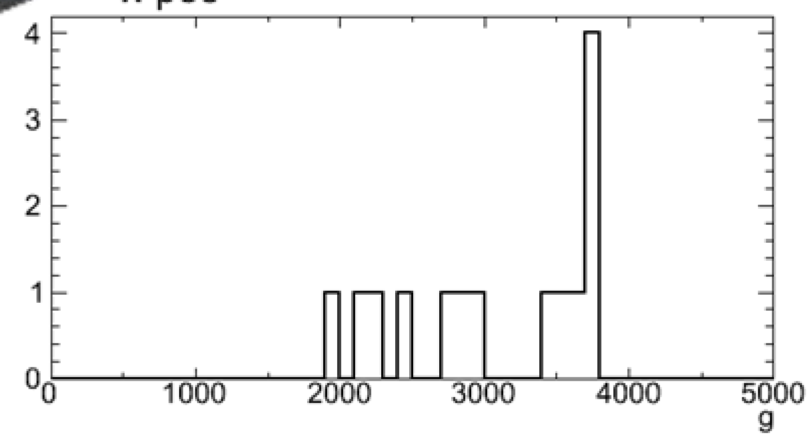
Pull test with "mechanical" FE-I3 chips placed below the hot pixels





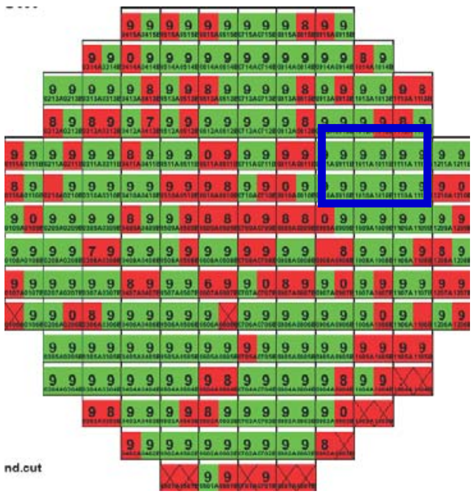
Connection strength – Pull out tests





- Pull out test performed with “mechanical” chips placed below the hot chips
- Connection strength of the order of 0.01N→ similar to bump-bonding and other pixel interconnection technology

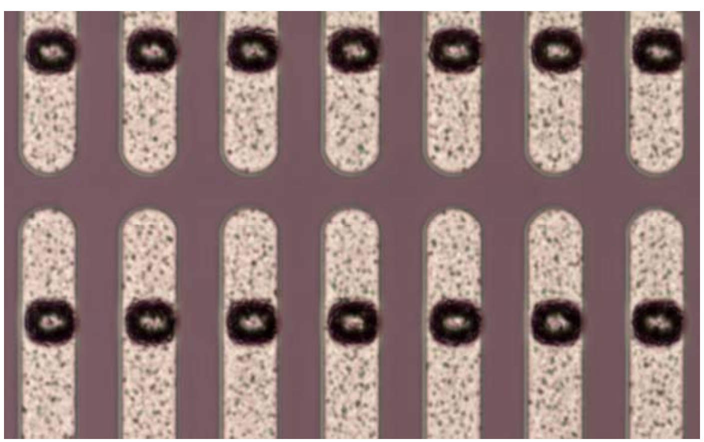
Possible causes of the SLID inefficiency

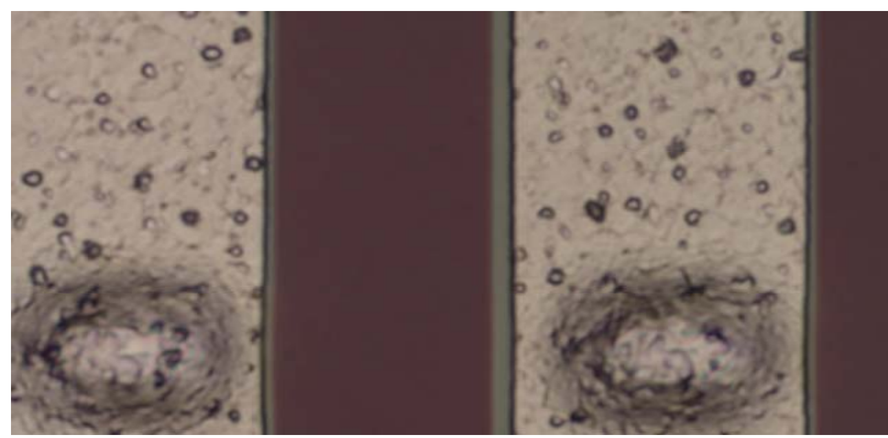


- The FE-I3 chip wafer has been thinned down to 200 um at EMFT before electroplating
- Differences in the chip heights (1-2 μm) could induce lack of homogeneity in the applied pressure.

- The hot chips were chosen from neighboring positions to minimize the height spread

- Not perfect openings in the BCB sensor passivation observed in some regions of the pixel sensors before SLID electroplating





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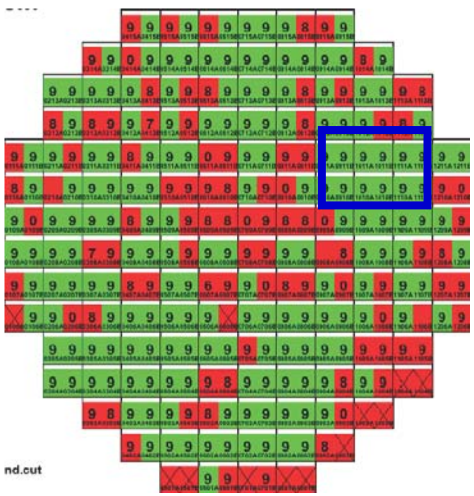

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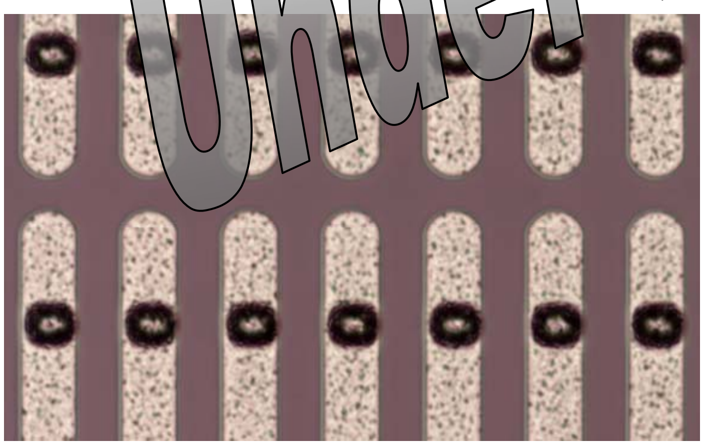
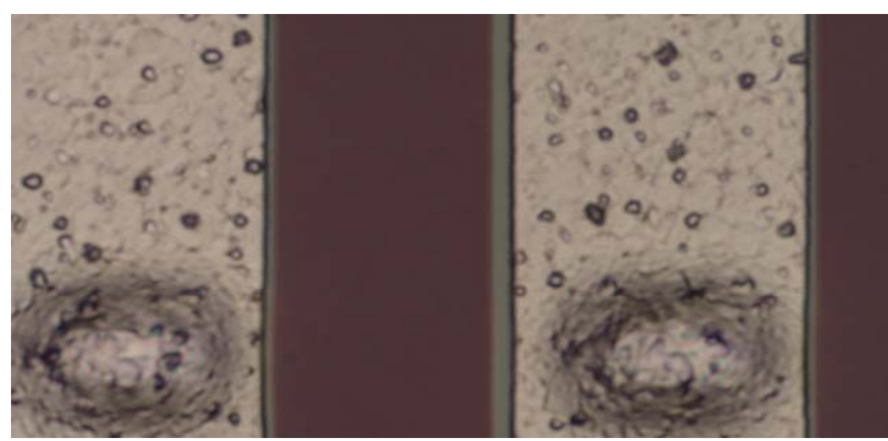
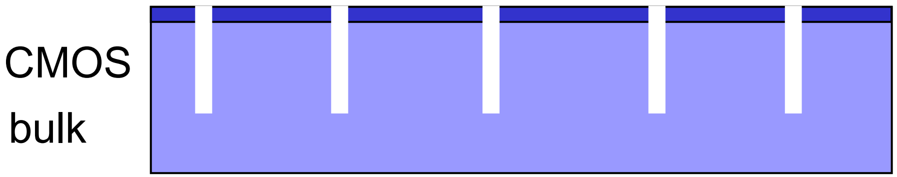
Under investigation

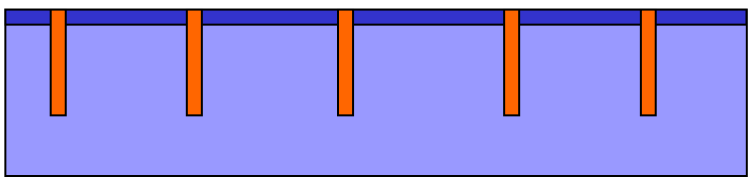




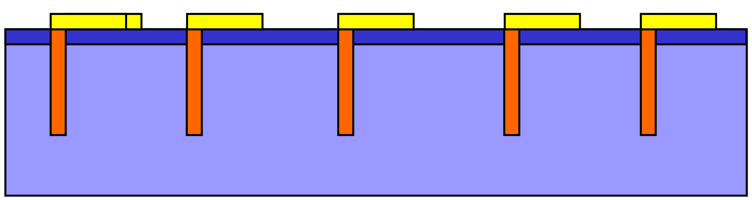
Trough Silicon Vias processing



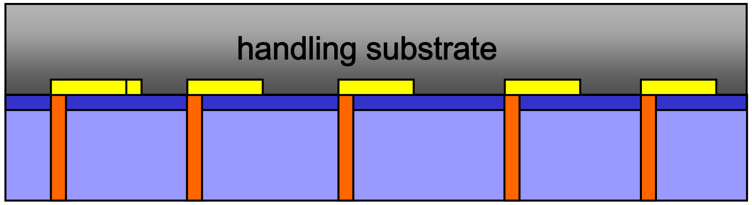
Etching (Bosch process) on FE-I3 8” wafers. 60 µm deep TSVs with lateral dimensions of 3 x 10 μm^2



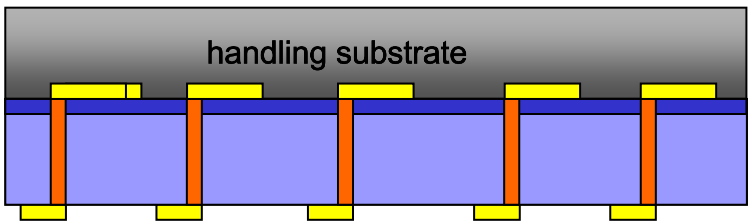
Insulation, filling with tungsten



Electroplating, metallization on the ASIC front side

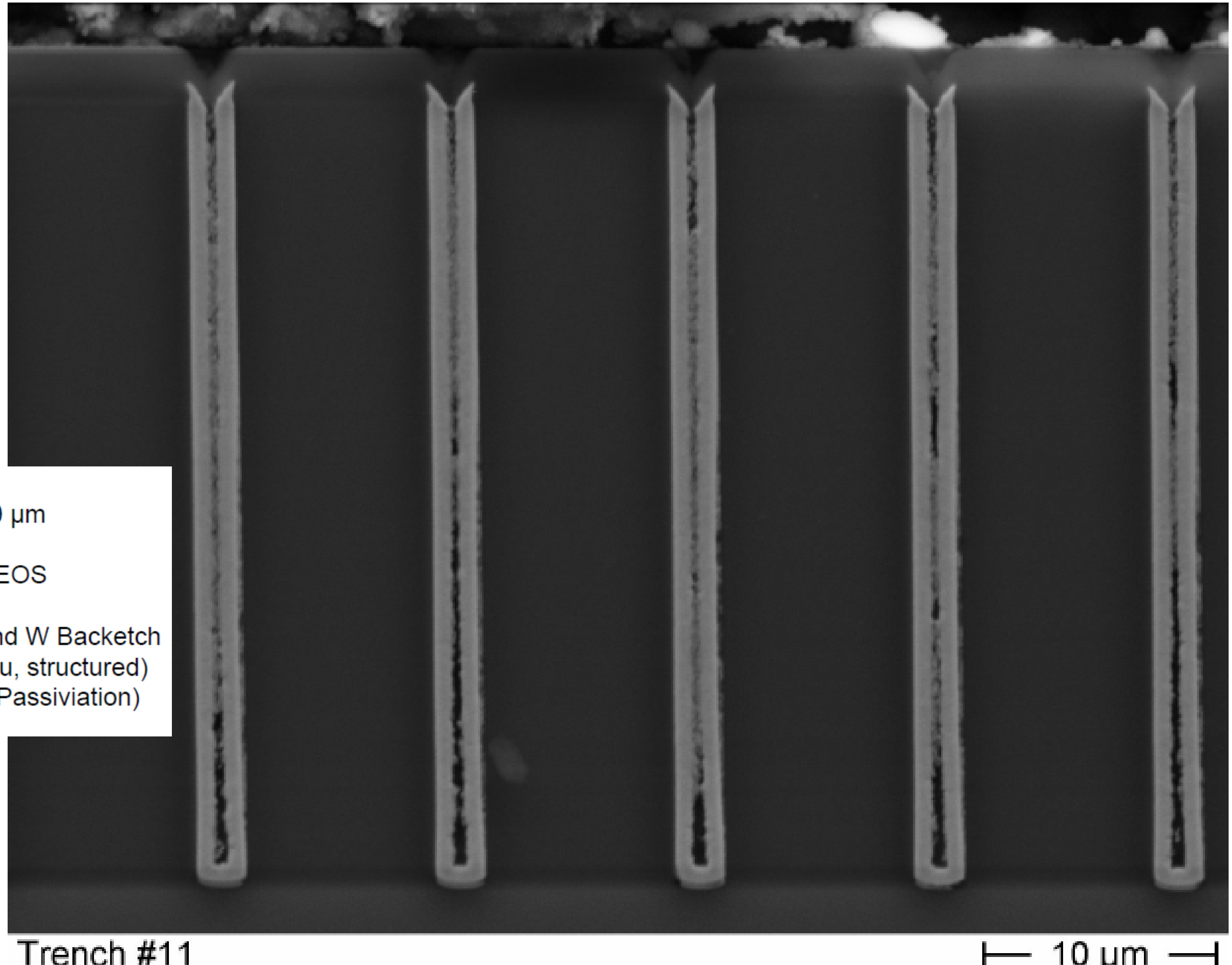


Back thinning to expose the TSV, backside isolation



Electroplating, metallization on the ASIC back side

Trough Silicon Vias processing



ICV-Dimensions:
3 µm x 10 µm x 50 µm

300 nm SACVD TEOS
20 nm TiN CVD
900 nm W CVD und W Backetch
800 nm M1 (AlSiCu, structured)
850 nm PN/POX (Passiviation)

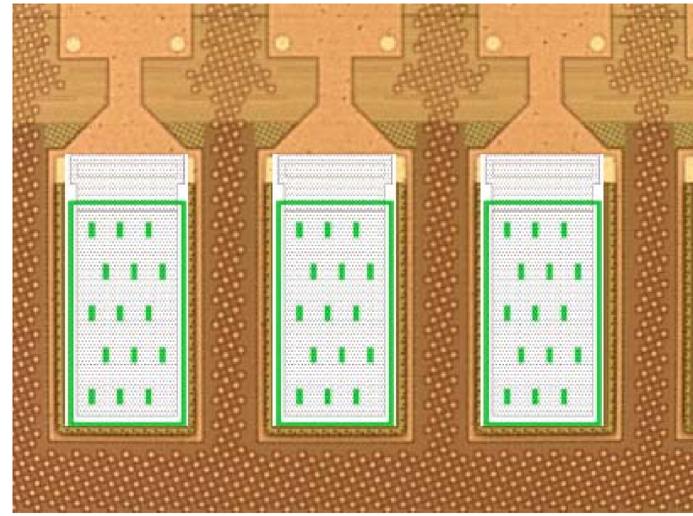
Courtesy of R. Wieland, EMFT

TSV in the FE-I3 chips

Fraunhofer EMFT TSV

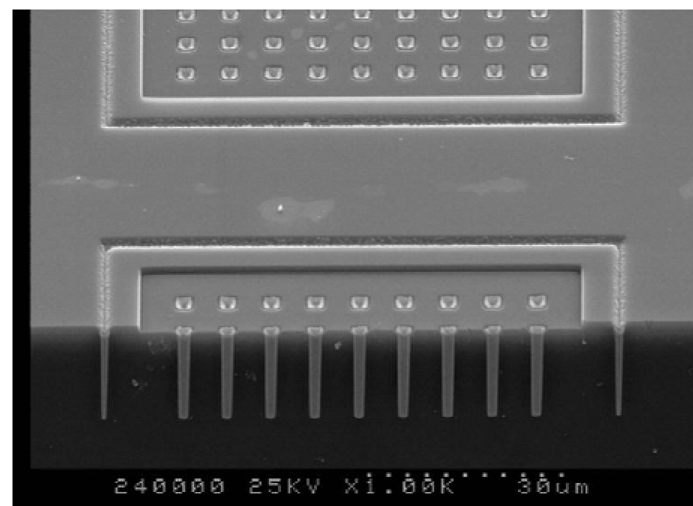
➢ First etching trials on dummy wafer ✓

- Performed in the un-thinned FE-I3 chips of one designated test-wafer
- Etched to a depth of ~ 69 μm
- Optimize the trench width to obtain the same depth as in the TSV



➢ Process plan of the hot FE-I3 wafer

- Local planarisation of the fan-out pads by depositing and etching of SACVD-Oxide ✓
- Perform via etching and filling in the hot FE-I3 wafer



- Connect the readout chip with SLID to the hot sensor wafers

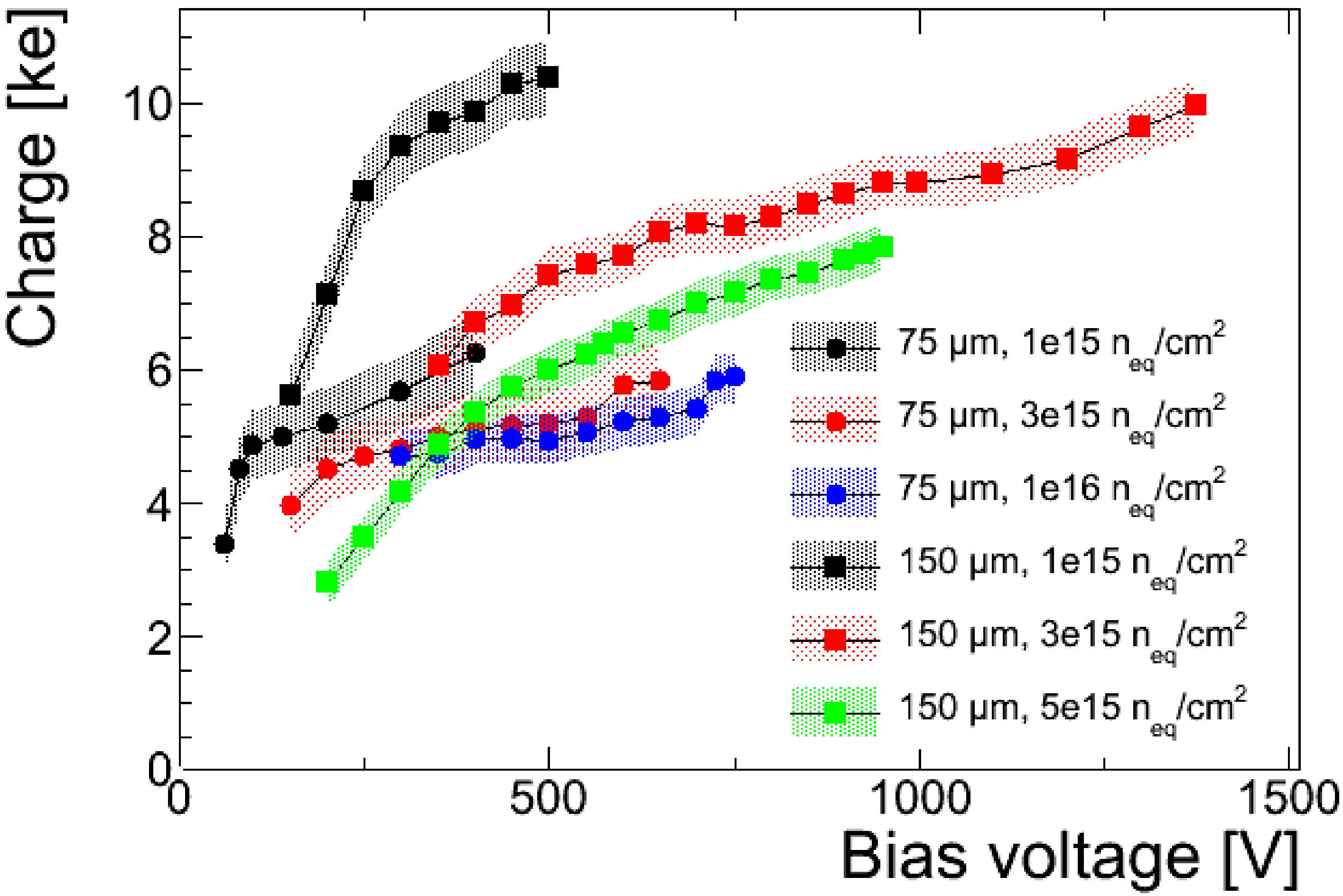
Summary and Outlook

- FE-I3 modules functional after SLID Interconnection, with extremely good performance (low noise, threshold dispersion, charge collection)
- Problems with chip alignment on the handle wafer
- Systematic loss of SLID connection efficiency for a fraction the modules close to the wafer center→ reasons under investigation, probably not related to the interconnection technology

Plans

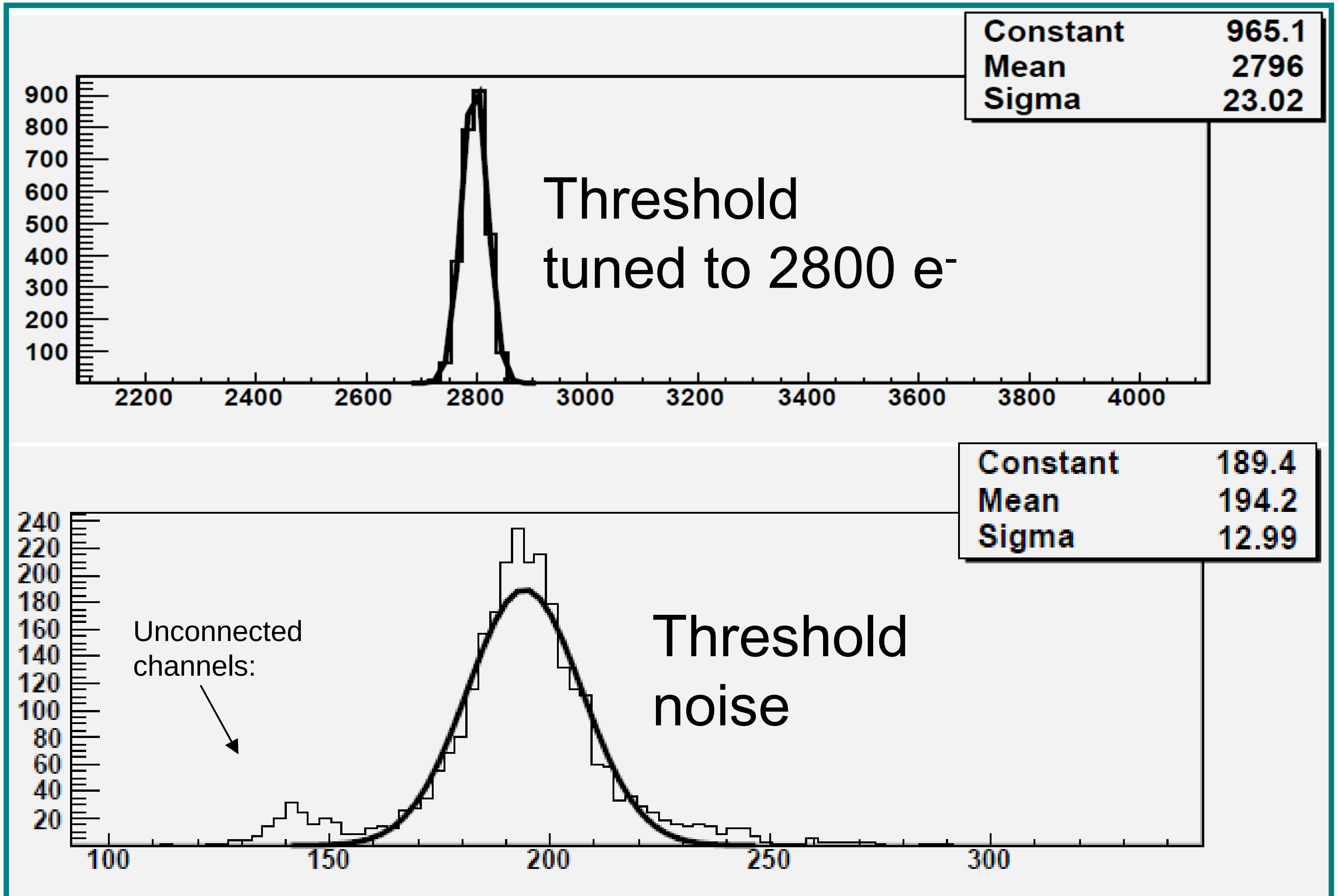
- Irradiate some of the SLID modules to study the radiation hardness of the technique
- Optimize pick and place of the chips on handle wafer with new machines
- Full SLID assembly of sensors and FE-I3 chips with TSV

Back-up Slides

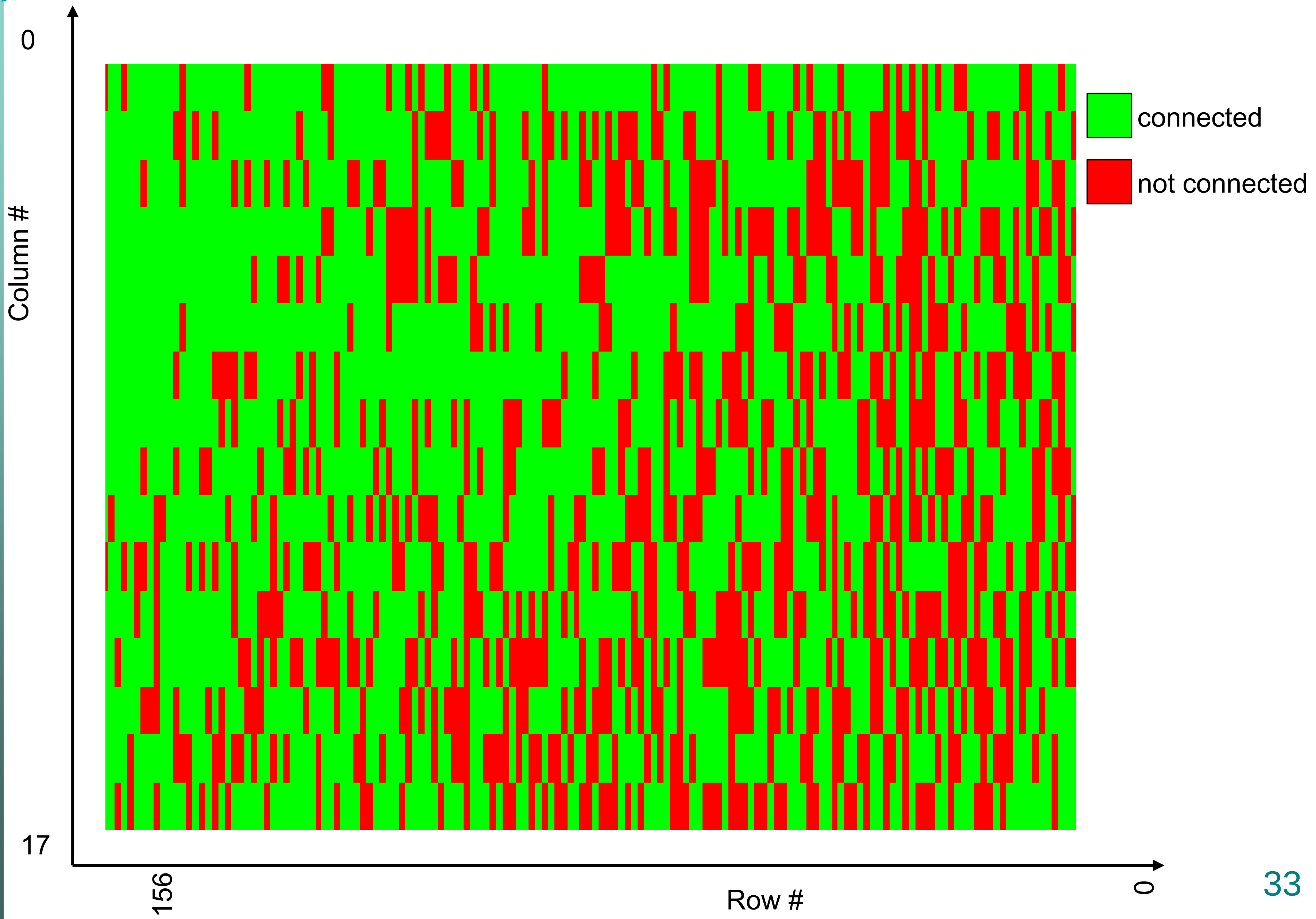

Charge [ke]
10
8
6
4
2
0
0
500
1000
1500
Bias voltage [V]
75 µm, 1e15 n_eq/cm^2
75 µm, 3e15 n_eq/cm^2
75 µm, 1e16 n_eq/cm^2
150 µm, 1e15 n_eq/cm^2
150 µm, 3e15 n_eq/cm^2
150 µm, 5e15 n_eq/cm^2

SLID Module 9: chip tuning

- Pixel with lower noise are an indication of unconnected channels

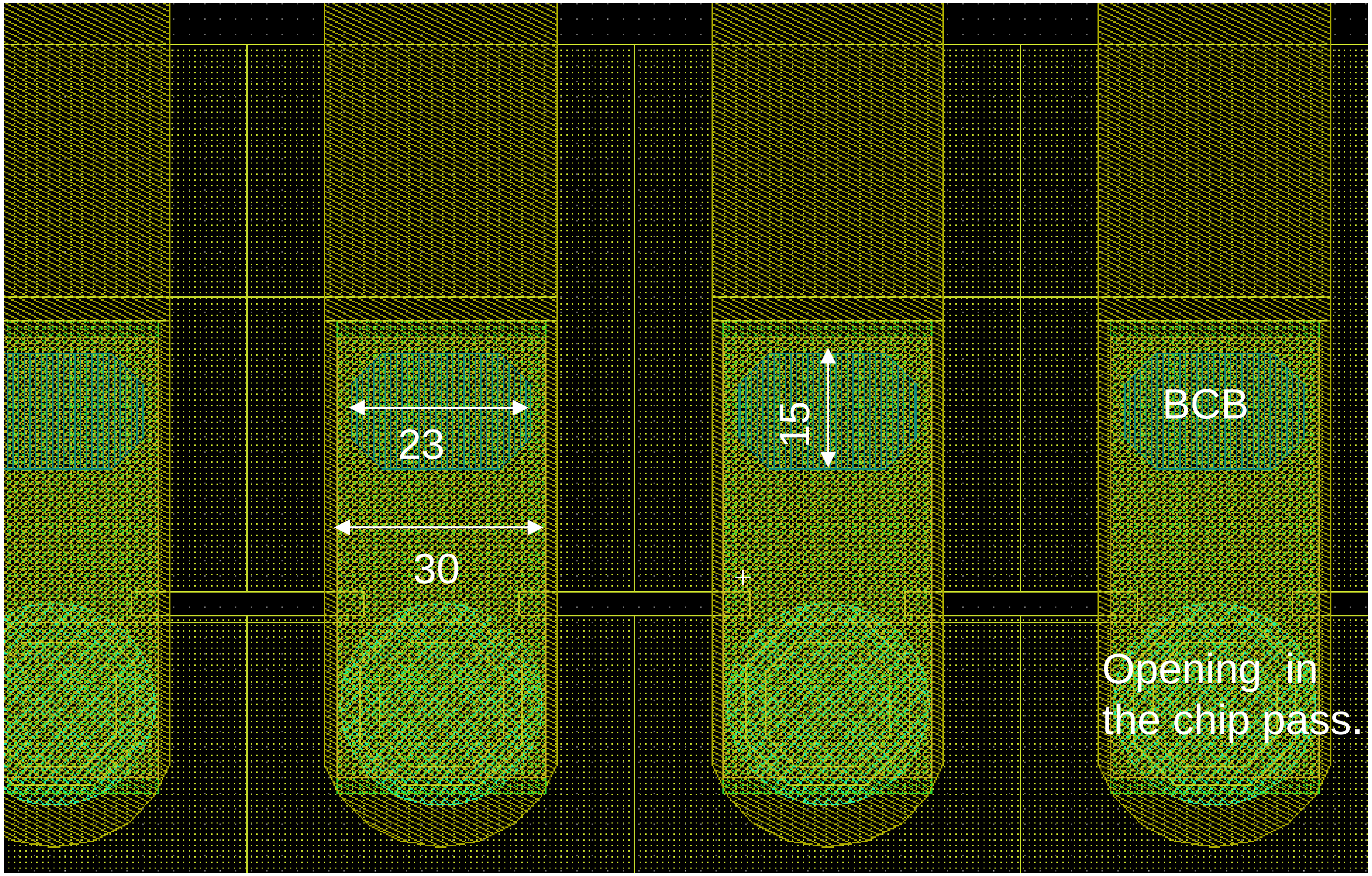


Connection map of SLID 7 module



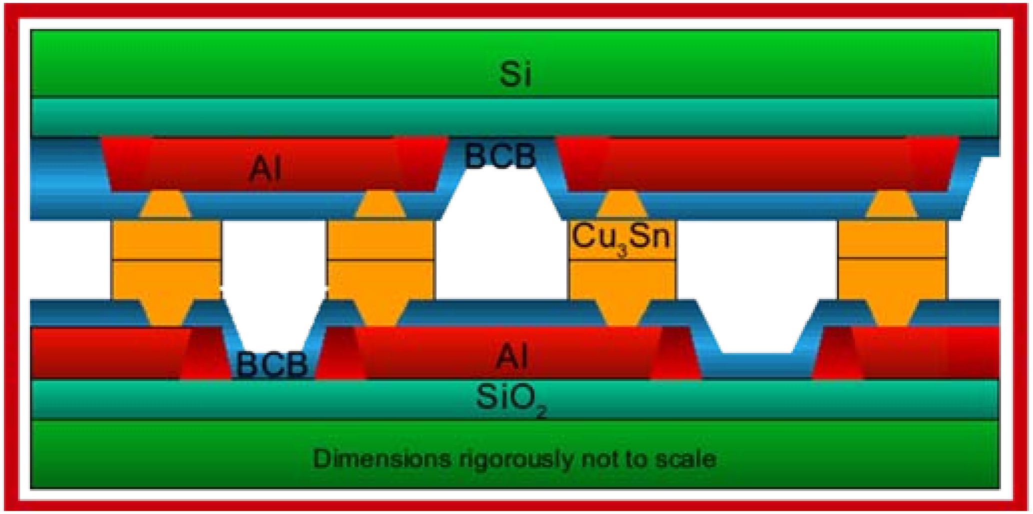
Possible causes of SLID inefficiency – BCB openings

- BCB passivation not completely open?



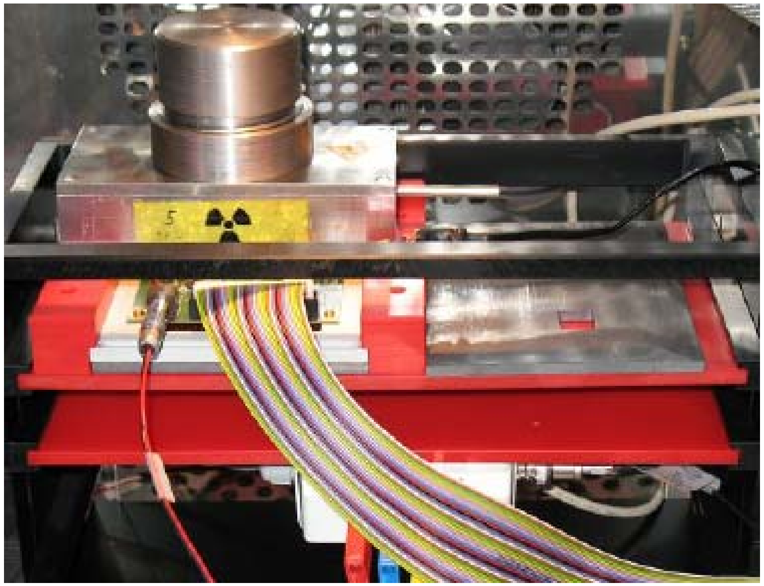
New daisy chain production for SLID testing

- FE-I4 geometry, daisy chains with 26800 pads each
- Arranged in the most regular pattern possible
- Test of the placement on the handle wafer with new flip-chipping machine at EMFT
- SLID efficiency with measurements of the electrical continuity



- EMFT can do the copper electroplating in house, tin will be available in October (subcontracted to IZM Berlin in the past).

CCE Measurements (I)

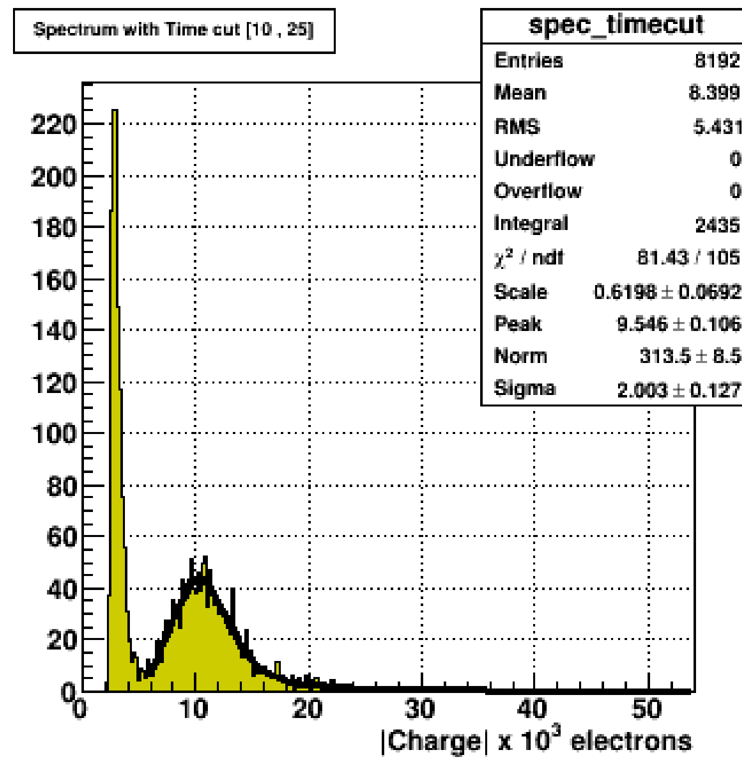


➢CCE measurements on irradiated n-in-p strips, from the same production,are on-going with the ALIBAVA system.

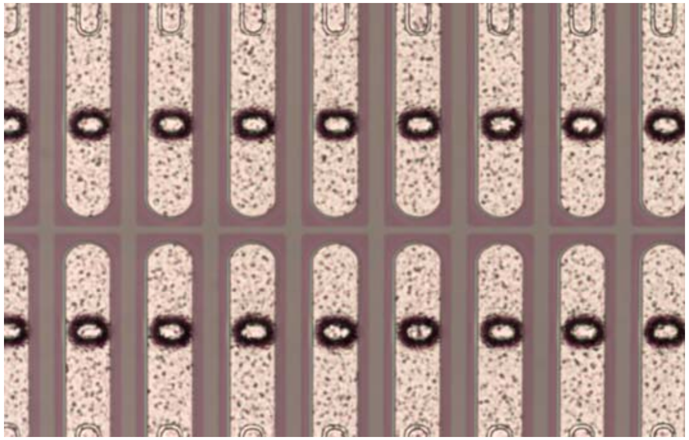
➢ The strip sensors used in these measurements have the same structure as the pixels (punch-through biasing, DC coupling) with the exception of the length (~ 7 mm)

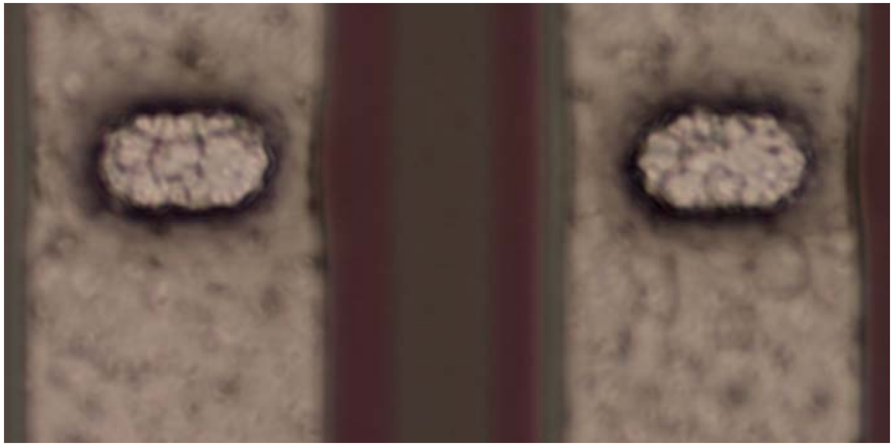
➢ CCE measurements on pixels are only possible after SLID interconnection of sensor and FE-I3 (in preparation, see next slides).

150 μm thick, Φ=3E15 n_{eq} /cm^2, V_{bias}=650 V



Possible causes of SLID inefficiency – BCB openings





- Region of a FE-I3 sensor (before SLID electroplating) with “strange” looking BCB openings