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## SLID-ICV Vertical Integration Technology for the ATLAS Pixel Upgrades

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A new pixel module concept is presented, where thin sensors and a novel vertical integration technique are combined. This R&D activity is carried out in view of the future ATLAS pixel detector upgrades.

A first set of n-in-p pixel sensors with active thicknesses of 75 and 150 microns has been produced from standard thickness wafers using a thinning process developed at the Max-Planck-Institut Semiconductor Laboratory. The pre-irradiation characterization of these sensors shows a very good device yield and high break down voltages.

After proton irradiations up to a fluence of  $1E16$  n eq./cm<sup>\*\*2</sup>, Charge Collection Efficiency (CCE) measurements have been performed, yielding a higher CCE than expected from the present radiation damage models [1].

The interconnection of thin n-in-p pixels to the FE-I3 ATLAS electronics has been completed, exploiting the Solid Liquid Interdiffusion technique (SLID) developed by the Fraunhofer institute EMFT-Munich, as a possible alternative to the standard bump-bonding. One of the main advantages of this interconnection technique with respect to bump-bonding is that it can be applied to a second layer of chips on top of the first one, without destroying the pre-existing bonds, paving the way to a full exploitation of vertical integration technologies.

The SLID interconnection is characterized by a very thin eutectic Cu-Sn alloy, achieved through the deposition of 5 microns of Cu on both sides, and 3 microns of Sn on one side only. The feasibility of its application in the parameter range needed for the ATLAS pixel detector has been investigated with a test-structure production used to explore both the “wafer-to-wafer” and the “chip-to-wafer” interconnection.

We will present the preliminary results of the characterization of the first FE-I3 pixel modules interconnected through SLID, performed with the ATLAS pixel read-out system USBPix.

In addition, the status of the Inter Chip Vias (ICV) etched into the FE-I3 chip wafers will be reported. ICVs will be used to route the signals vertically through the read-out chips, to newly created pads on their backside. In the EMFT-Munich approach the chip wafer is thinned to about 50 microns and support wafers are used during the thinning and interconnection phases.

If successful this will serve as a proof of principle for future four-side buttable pixel assemblies, without the cantilever presently needed in the chip for the wire bonding.

[1] A. Macchiolo et al., “Performance of thin pixel sensors irradiated up to a fluence of  $1E16$  n eq./cm<sup>\*\*2</sup> and development of a new interconnection technology for the upgrade of the ATLAS pixel system”, NIM A, in press, doi:10.1016/j.nima.2010.11.163

**Author:** Dr MACCHIOLO, Anna (Max-Planck-Institut fuer Physik)

**Co-authors:** MOSER, Hans-Guenther (Max-Planck-Institut Semiconductor Laboratory); ANDRICEK, Ladislav (Max-Planck-Institut Semiconductor Laboratory); BEIMFORDE, Michael (Max-Planck-Institut für Physik); WEIGELL, Philipp (Max-Planck-Institut für Physik); RICHTER, Rainer H. (Max-Planck-Institut Semiconductor Laboratory); NISIUS, Richard (Max-Planck-Institut für Physik)

**Presenter:** Dr MACCHIOLO, Anna (Max-Planck-Institut fuer Physik)

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