Belle2Link: a Global data Readout and transmission for Belle II Experiment

Liu Zhen-An, Sun Dehui, Zhao Jingzhou, Xu Hao

Trigger Lab

IHEP, Beijing

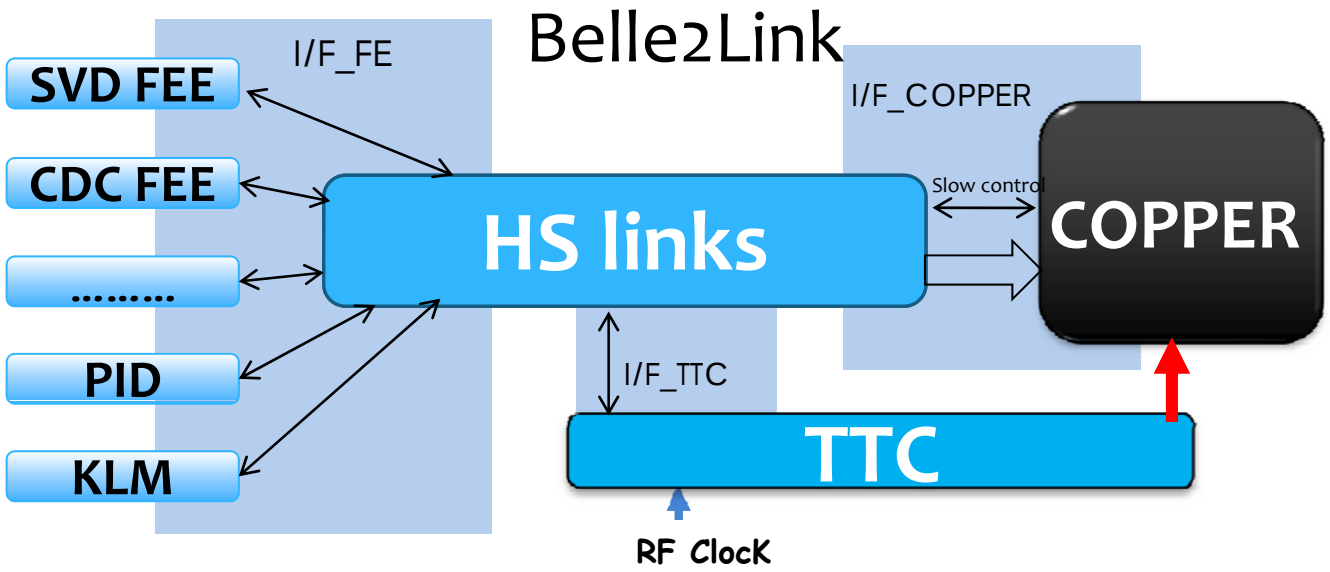
Outline

* Overview
* Hardware Description
* Firmware Description
  * Implementation of slow control
* Model system
  * Joint Test with CDC model
  * Data analysis
* Summary

Overview for Belle2Link

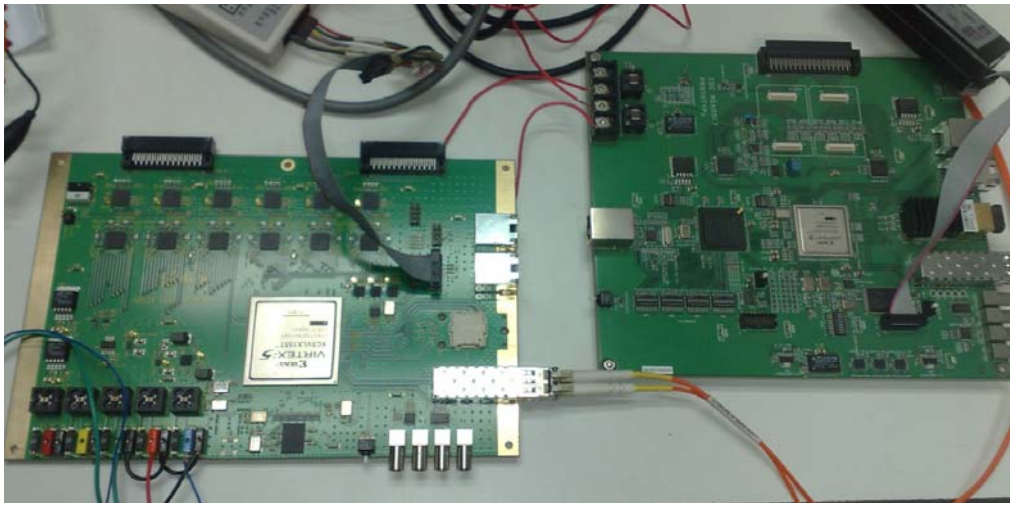
Belle2Link is a name for global fast data readout and transmission between Detector Front-End Electronics(FEE) and Back-End DAQ system of Belle II experiment. It features, with system simplicity and reliability, as:

1. unification in hardware design(for each detector sub-system)
2. unification in firmware design(for each detector sub-system)
3. provides electrical isolation
4. provides high speed transmission rate
5. work at different input data rate(with different detector sub-system)
6. home brew transmission protocol
7. Slow control on the same link



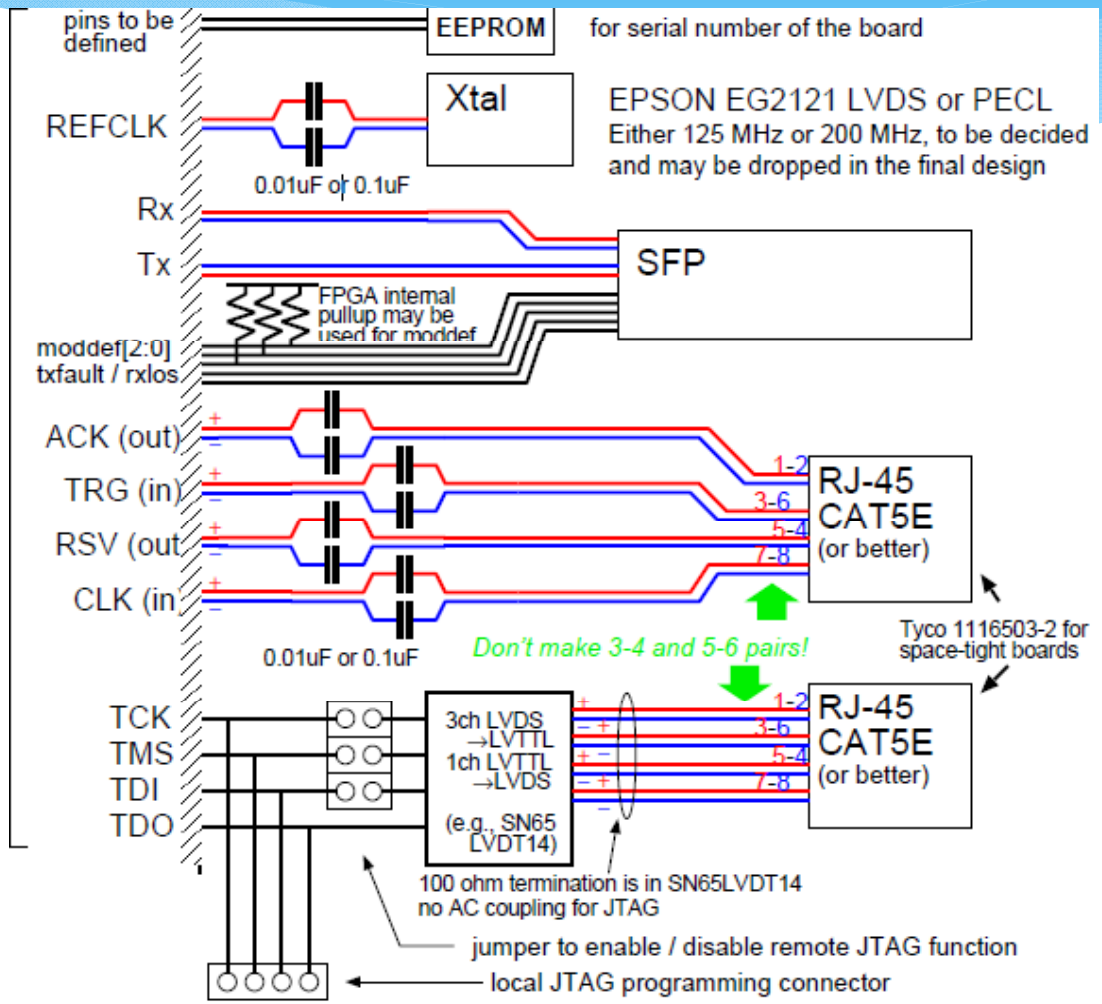
Hardware Description

* Front-End Electronics
  * The hardware will be designed by each detector system following Belle2Link requirement for FPGA and high speed transceivers
  * The readout and data transmission will be part of belle2link
  * Integration of FEE and Belle2link at IHEP for CDC as a Model



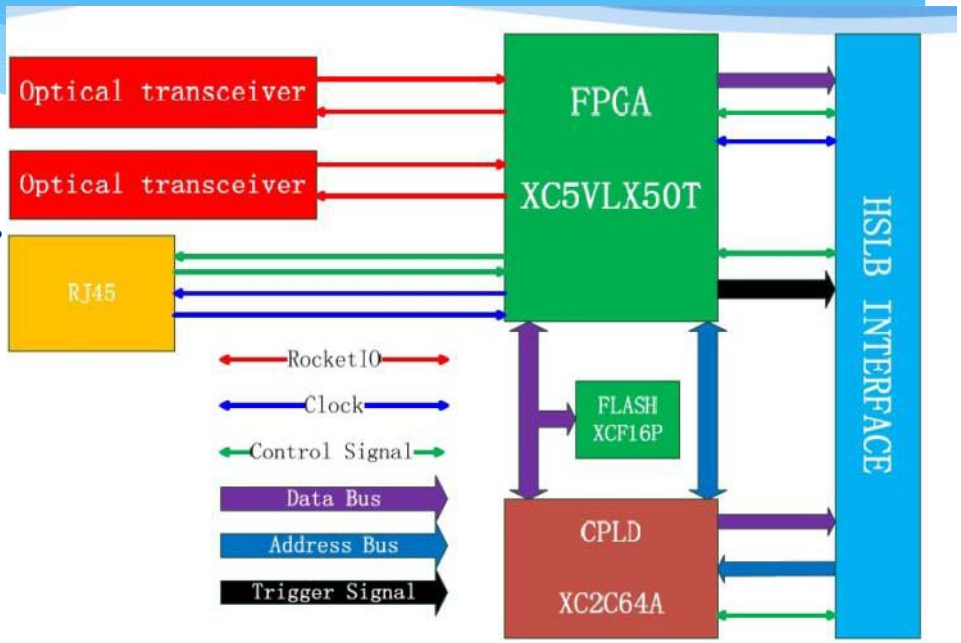
Belle2Link/timing interface at FEE

* Unification in Belle2Link/timing interface Design
* A serial port with SFP transceiver for Belle2Link
* RJ45X2 for JTAG and Timing
* On-board crystal for backup



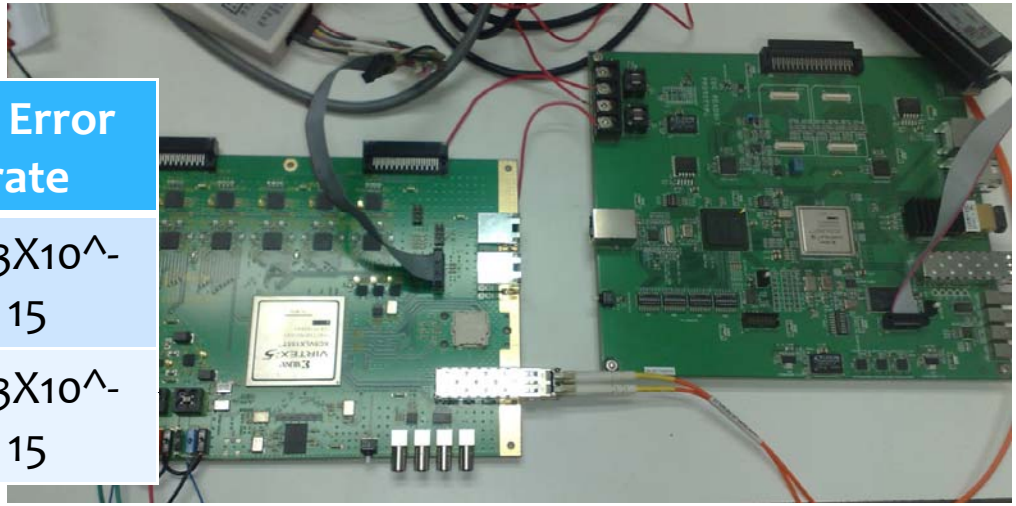
Interfacing card to COPPER

- Belle II DAQ is based on COPPER
- HSLB: High speed Link Board put on existing COPPER board
- Designed lane rate : 3.125Gb/s/ch.
- Data Preprocessing ability
- Online configuration.
- Version 2.0 is satisfactory.
- Belle2link Model system based on this version
- Joint test with detector model based on this
- Mini-production under going for all subsystem



the HSLB

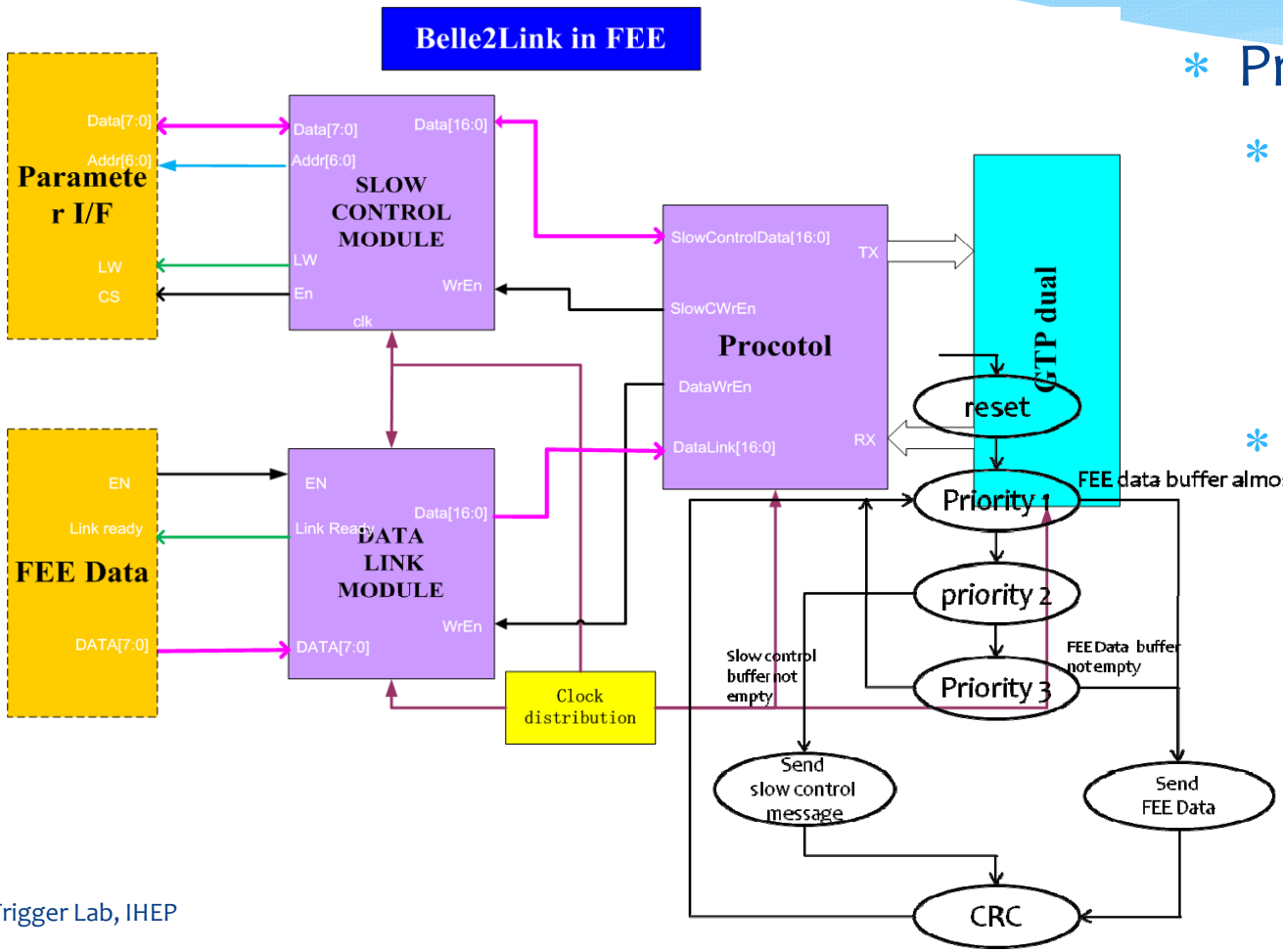
- HS Link
  - Line rate: 3.125Gbps.
- Data transfer to COPPER
- Configuration
  - online: CPU->CPLD->FPGA
  - reloadable Flash



Direction	Error	Time	Bit Error rate
HSLB->CDC	0	72 hours	<1.3X10^-15
CDC->HSLB	0	72hours	<1.3X10^-15

Firmware Description

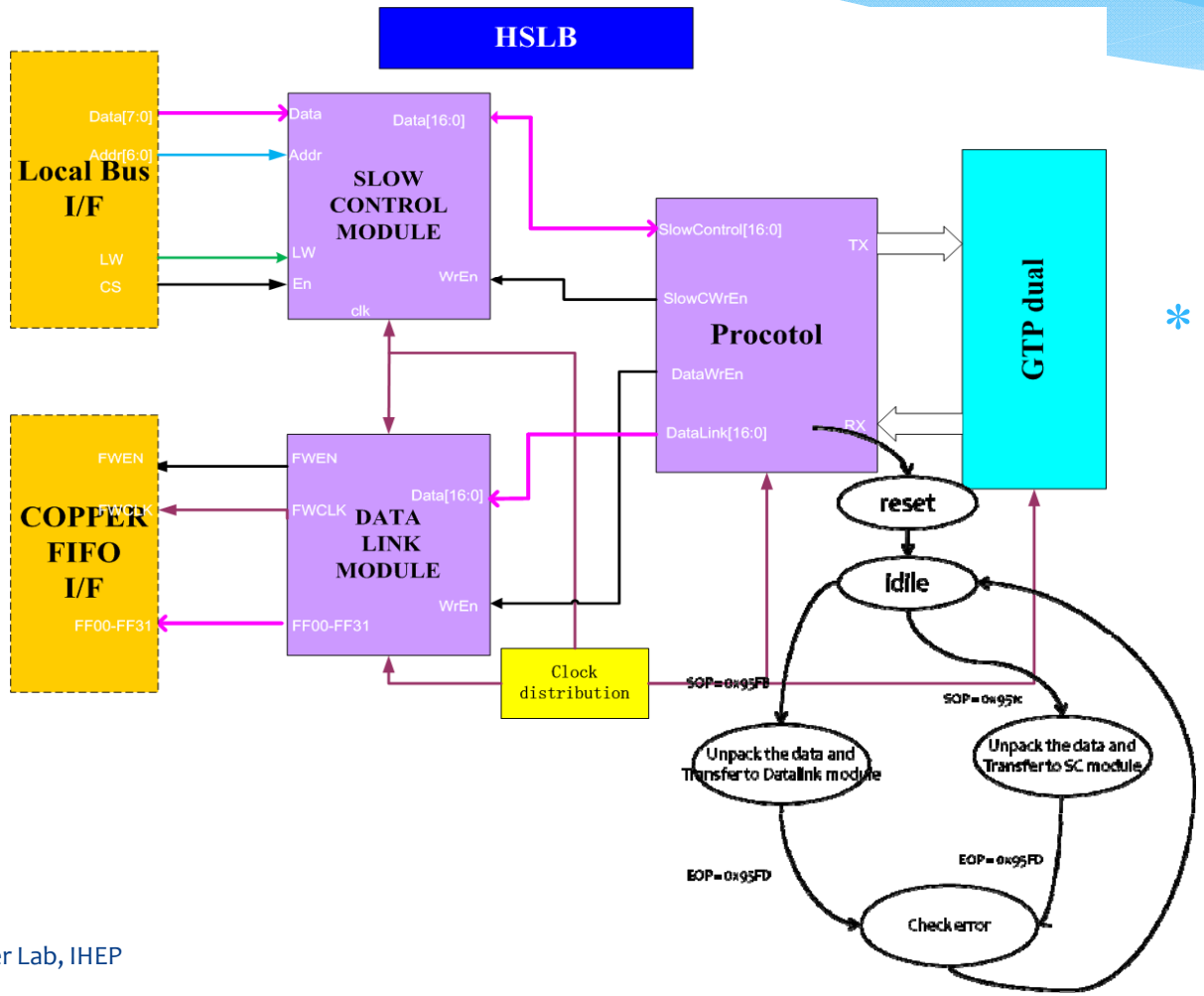
—Structure of Belle2lin firmware in FEE



- Data Link module
  - FEE data readout
- Protocol
  - Receive the package from GTP module, check the packages and unpack them
  - Transfer the data form FEE, and arbitrate the priority between slow control module and data link module

Firmware Description

——Structure of HSLB firmware



- Data Link module
  - Receive the data of FEE, communicate with COPPER through DMA
- Protocol
  - Receive the package from GTP module
  - Check the packages and unpack them
  - Separate the data and transfer them to slow control module or data link module

Implementation of Slow Control

* General Consideration
  * Task for Belle2link
    * Parameter setting
  * Aim
    * Unification suitable for all systems, not system dependent
    * Easy implementation for FEE
    * Provide CDC implementation as an example for other subsystem

Slow control

- CDC so far requires ~50 8-bit parameters for 48ch
  IHEP will implement them in their first version of Belle2link
- SVD's parameters will be set up not through Belle2link
- ECL is willing to set up parameters through Belle2link including DSP code, it will be up to 20 Mbytes
- Madatory registers
  - FINESSE has 8 pre-defined mandatory registers including the board type and serial number for each board
  - It would be nice to have a similar set of registers for the frontend boards
  - To store the serial number, an EEPROM would be the best way (part number of protocol to be defined)
- (not discussed) How to write the front-end register is straighforward. How to read is not trivial.

Local Bus Interface

Local Bus Interface

- **Local bus: A7D8 (addr: 0x00-0x7f)**
  - To configure chips,
  - To monitor module status.
  - To download a firmware.
- **Signals**
  - LA0-LA6 Local address bus.
  - LD0-LD7 Local data bus.
  - LWR Read/write direction indicator.
  - $\overline{CS}$ FINESSE module selector.

Address	Description	Note
0x00 - 0x77	User defined	–
0x78	CSR (active H)	
	bit 0: Initialize all registers and FIFOs in the FINESSE module	*mandatory*
	bit 1: Busy out emulation	
0x79		
0x7a		
0x7b		
0x7c		
0x7d		
0x7e		
0x7f		

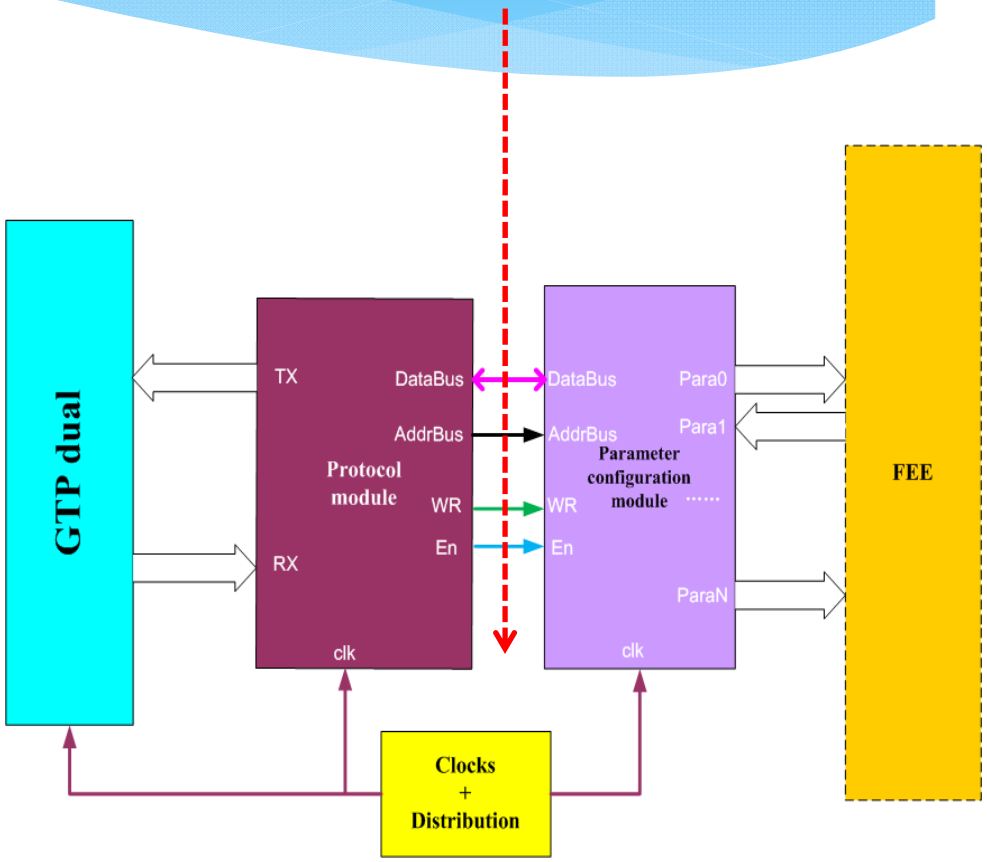
Address	Description	Note
0x00-0x74	User defined	
0x75	HSLB CSR	
0x76	FEE FW Ver. #	Mandatory
0x77	FEE HW Ver. #	Mandatory
0x78	FEE Type	Mandatory
0x79	Belle2link FEE FW ver. #	Mandatory
0x7a	HSLB Download Flag2	
0x7b	HSLB Download Flag1	
0x7c	Belle2link HSLB CPLD Ver.	
0x7d	Belle2link HSLB FW ver. #	Mandatory
0x7e	Belle2link HSLB HW ver. #	Mandatory
0x7f	Reserved	mandatory

* Difficulties
  * Larger parameter data size(>128byte) ne
  * How to make the belle2link transparent
* New scheme has to be defined
  * FEE and HSLB share the address on local bus
  * Both FEE board and HSLB have the independent version records.

Implementation of Slow Control

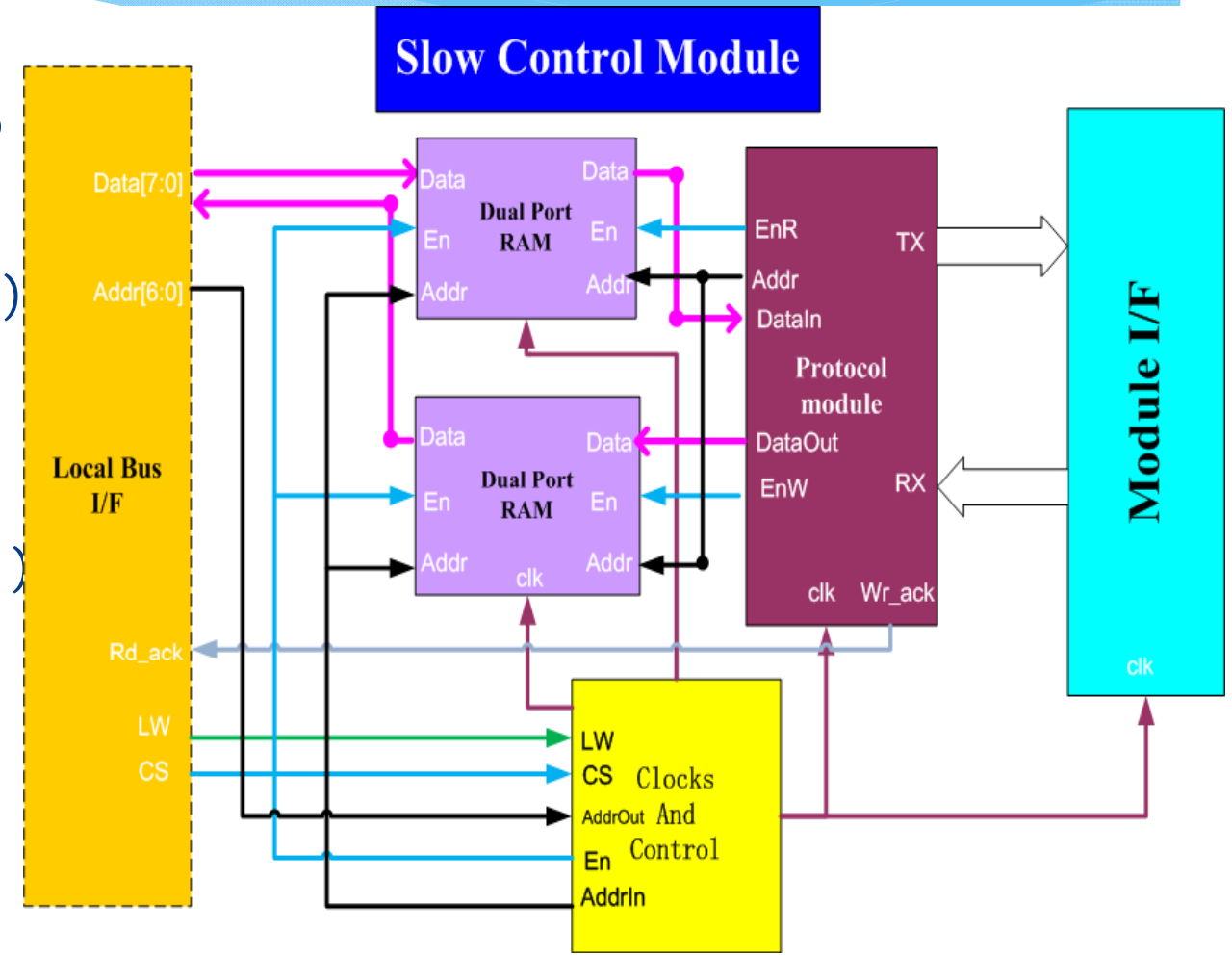
* FEE side(Parameter Bus)
  * Keep the definition of local bus of COPPER.
    * AB0-AB6 Local address bus.
    * DB0-DB7 Local data bus.
    * LWR Read/write direction indicator.
    * EN ready signal.
  * An indicated address 0x00 is for serial transmission

The Belle2link is transparent to the COPPER and FEE.



Implementation of Slow Control

* HSLB/FINESSE side(Two approaches)
* First approach
  * Large stream(>128B)
  * Address 0X00: for this approach
* Second approach
  * Large stream(<128B or individual setting)
  * Address 0X01-0x74: Length up to 127B
  * Address/Data meaning definition by system



Model system

Purpose

* Working system for each detector system

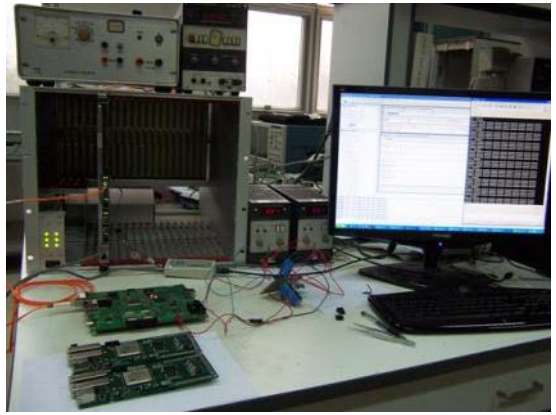
Hardware

* FEE board(CDC board as model)
* Optic fibers
* High Speed Link Board (HSLB, Plugged to COPPER)
* COPPER board
* Server PC (file system server)

CDC board linked to HSLB

COPPER board

HSLB



COPPER plugged in VME crate with a File server

Model system

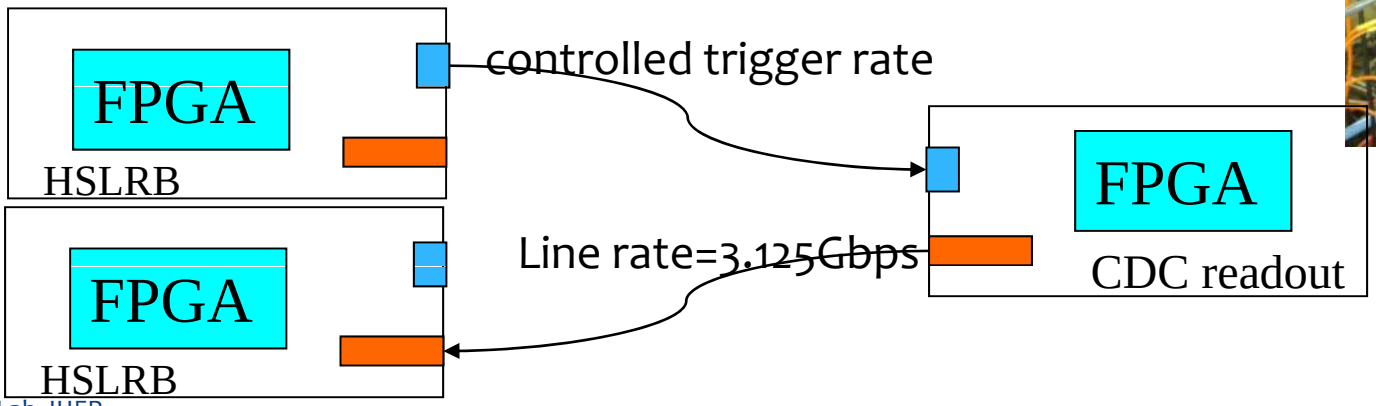
- Firmware
  - FEE
    - Belle2Link in FEE part
  - HSLB
    - Virtex 5 Firmware (Belle2link in HSLB part)
    - CPLD Firmware (online downloading)
- Software
  - Driver: HSLB Finesse card driver
  - Data processing
    - readhslb : read the data of FEE from the COPPER;
  - Slow control
    - paraconf : read or configure the register of HSLB and FEE
    - fileconf : dedicated configuration file to FEE, such as a DSP ROM file

Model system--Joint test at KEK

Setup: CDC-Prototype + 16ch FEE + fiber+ HSLB +COPPER + VME crate + File server

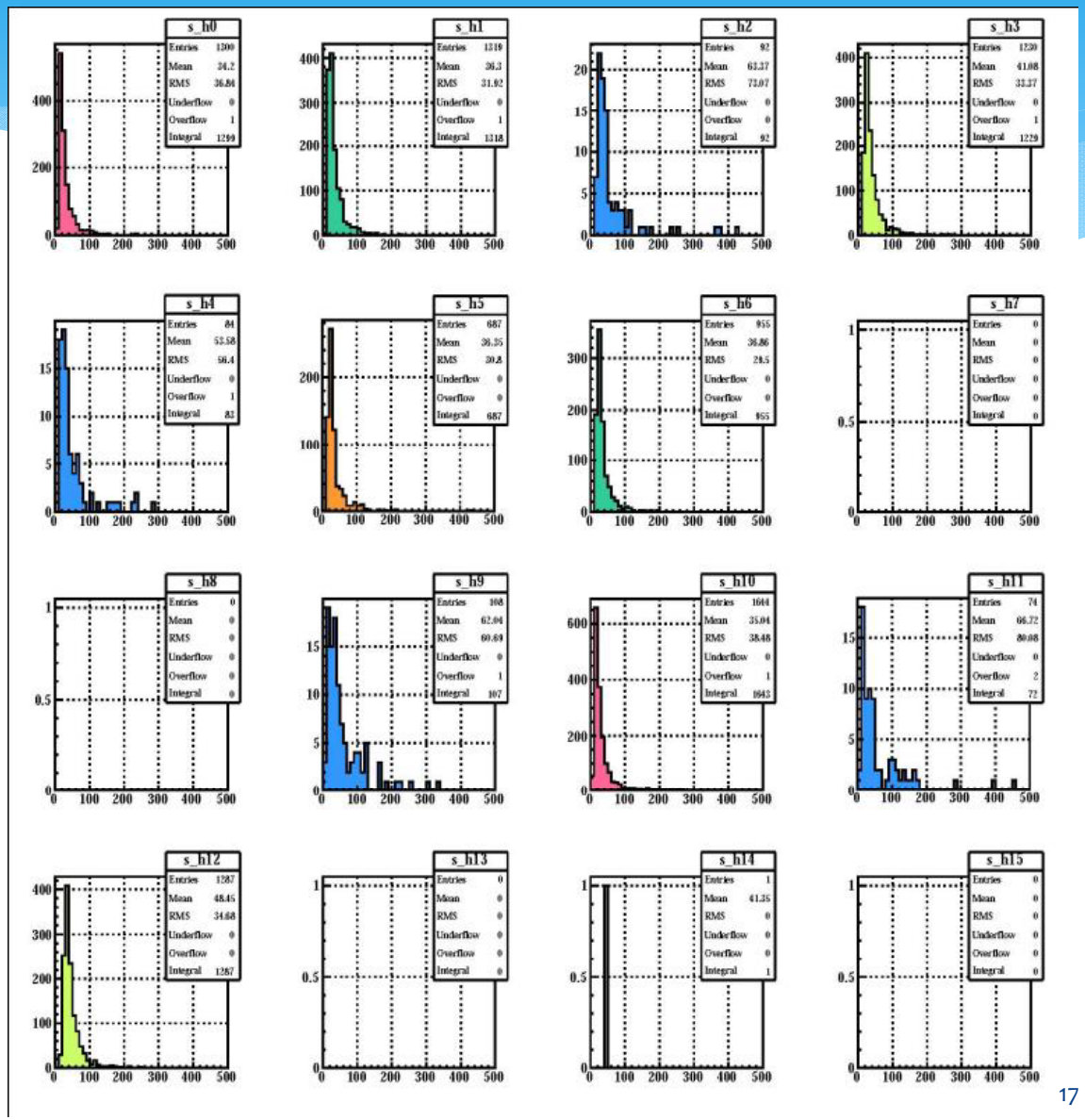
July,2010 KEK Tsukuba center

- Data from radioactive source
- Lane rate: 3.125Gbps
- Data sample
  - 3M events collected
  - 10k events analyzed



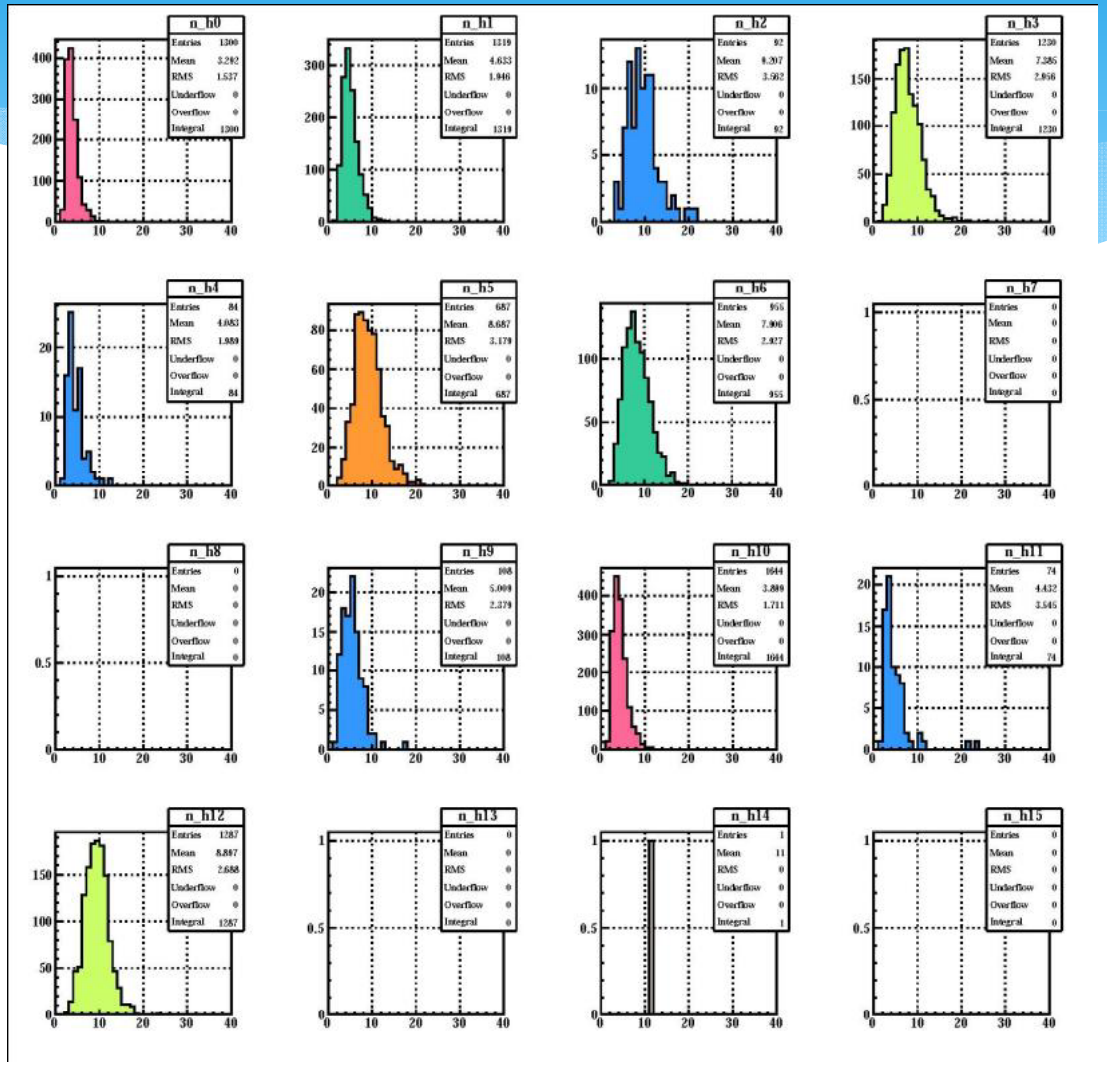
Data Analysis

- s_h* means the sum of ADC value which are lager than the value of 2xsigma(pedestal)
- The mean of pedestal is subtracted from ADC value before calculation. The value of sum correspond to energy loss of beta-ray in the chamber.
- Dead channels
  - Ch7,ch8,ch13-15



Data Analysis

- n_h* means the number of ADC bin which are used in sum calculation in 1-event
- Dead channels
  - Ch7,ch8,ch13-15

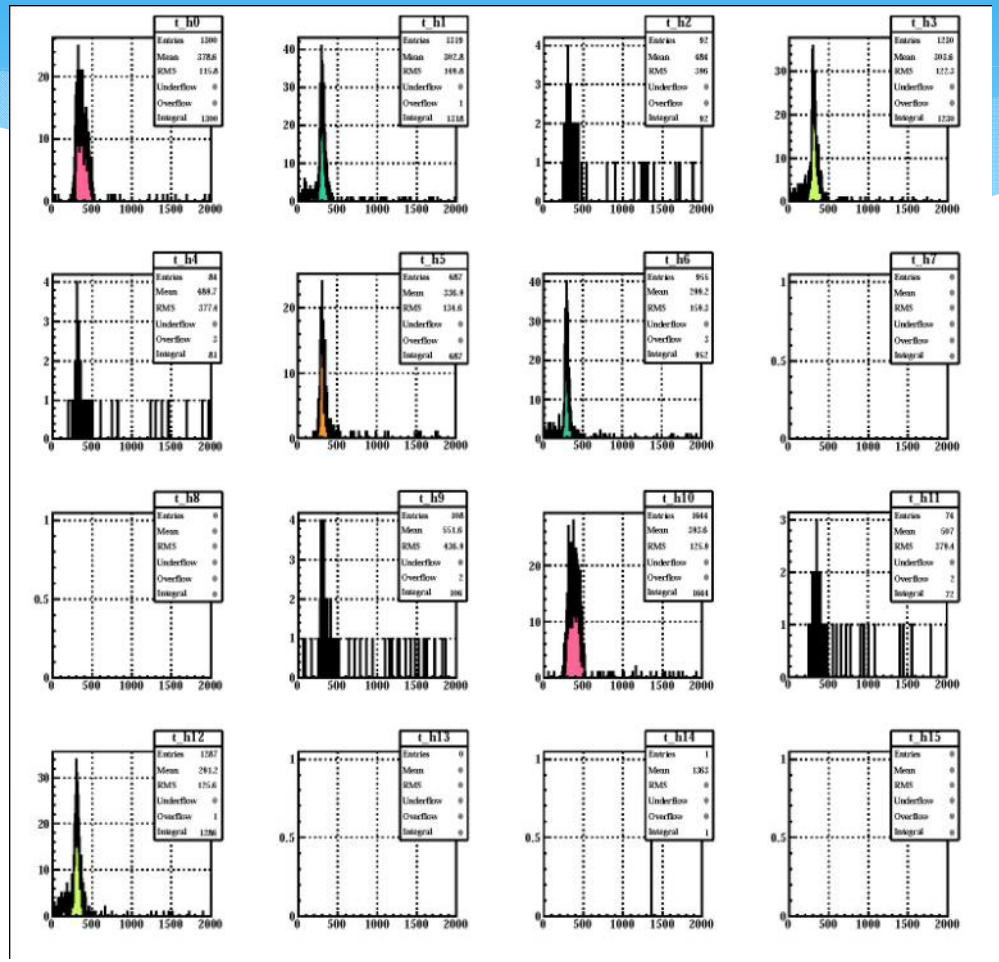


Data Analysis

- t_h* means the difference between trigger timing and timing when signal go over threshold.
- Dead channels
  - Ch7,ch8,ch13-15

We can confirm that timing is similar in all channel and sum (energy loss) is almost similar in all. It means that the data is correct.

The model system is reliable.



Summary

* The Belle2link has been accepted by the Belle II collaboration and documented in TDR
* Model system is successful and Joint tested with CDC detector Model
* The model system is in production for each detector system

Many Thanks for your attention !