A Gigabit Transceiver for Data Transmission in Future HEP Experiments

and

An overview of optoelectronics in HEP

Outline

Optoelectronics

- What? Why? How?
- Experience in HEP (LHC) & future

Gigabit Transceiver Project (GBT)

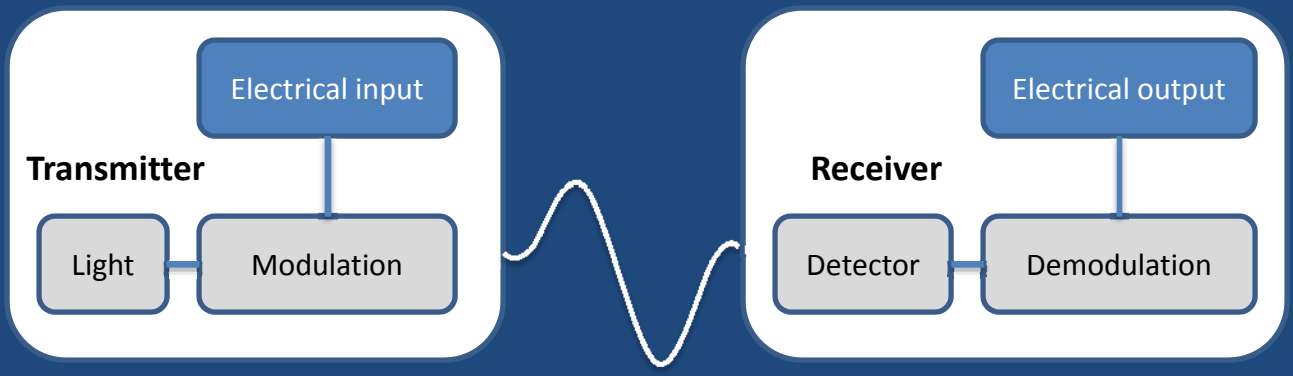
- Motivation & Concept
- Specific constraints
- Design
- Results
- Future

Optoelectronics – what?

Electronic devices that source, detect and control light

Typical system:

active elements coupled to passive elements (lens, fiber....)
to form fibre-optic communication systems – rest of this talk



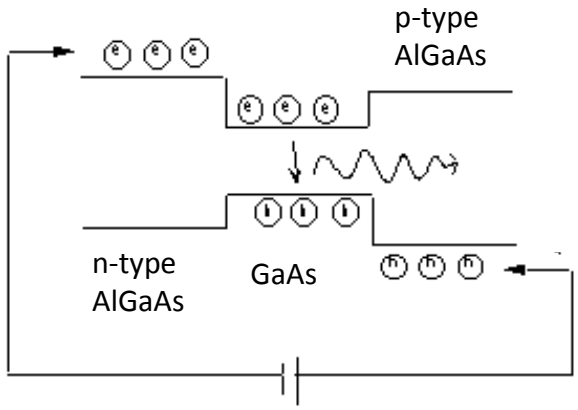
Active elements

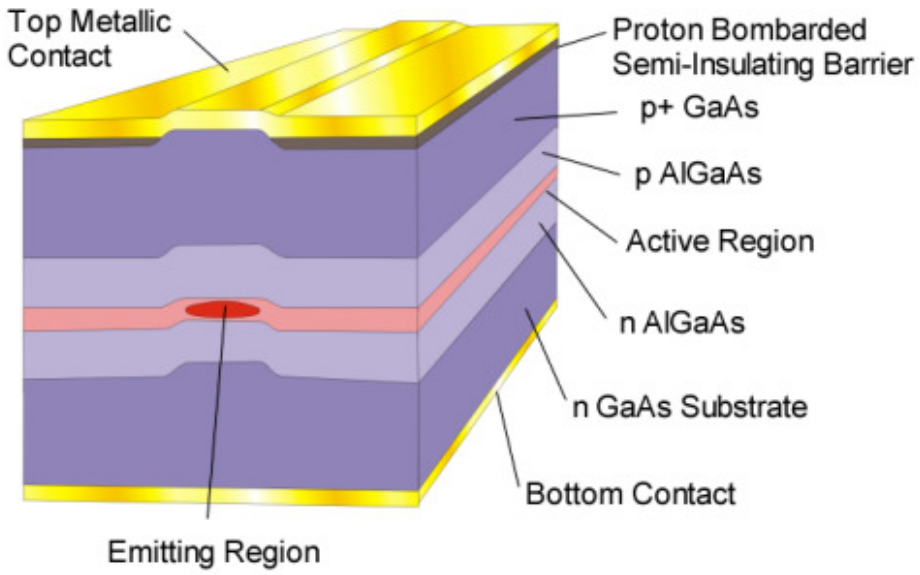
⇒ semiconductor technology (lasers, photo-diodes.....)

⇒ quantum mechanical effects translate between electrical & optical domains

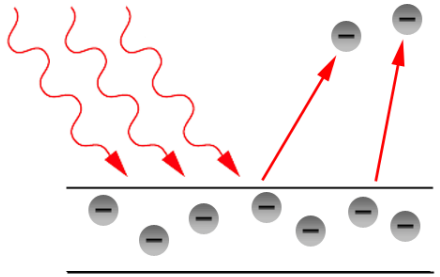
Typical devices

Light from lasing:
Electrical pumping & band-gap engineering





Photon detection by photoelectric effect
eg photo diode



Optoelectronic communication – why use it in particle physics?

We gain a lot from the commercial world!

- **Speed: bandwidth driven by global market**
  fast, compact devices

40Gbit/s
Parallel optics

- **Signal integrity**
  insensitive to EM noise, no EM emission, distance, coding
- **Galvanic isolation**
- **Low mass cabling**
- **Power: driven down by global market**
  more Gbit/s per joule……

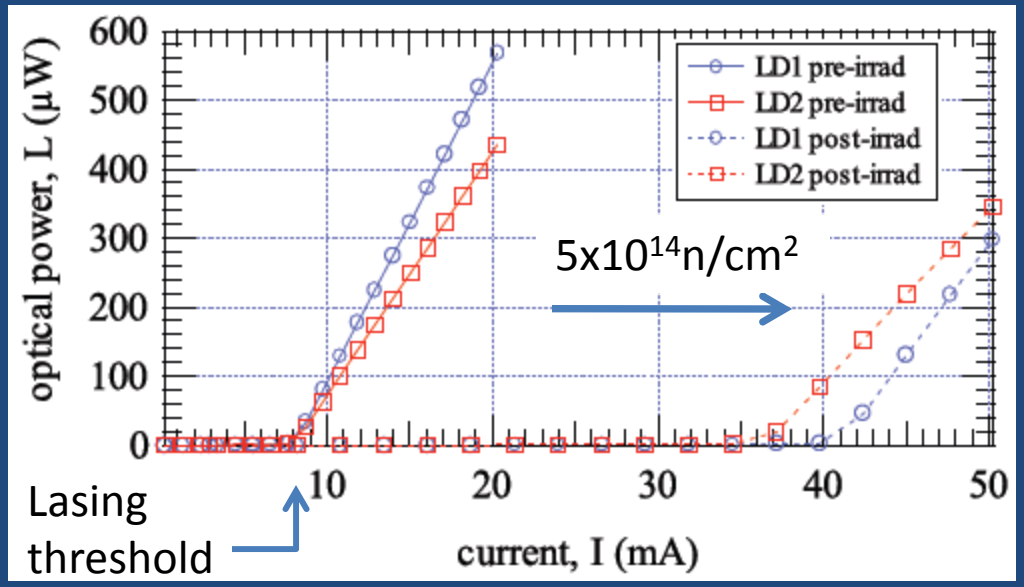
Radiation effects.....?

No help from the commercial world!

Optoelectronics devices are sensitive to:

- **Displacement damage**
  (eg neutrons)

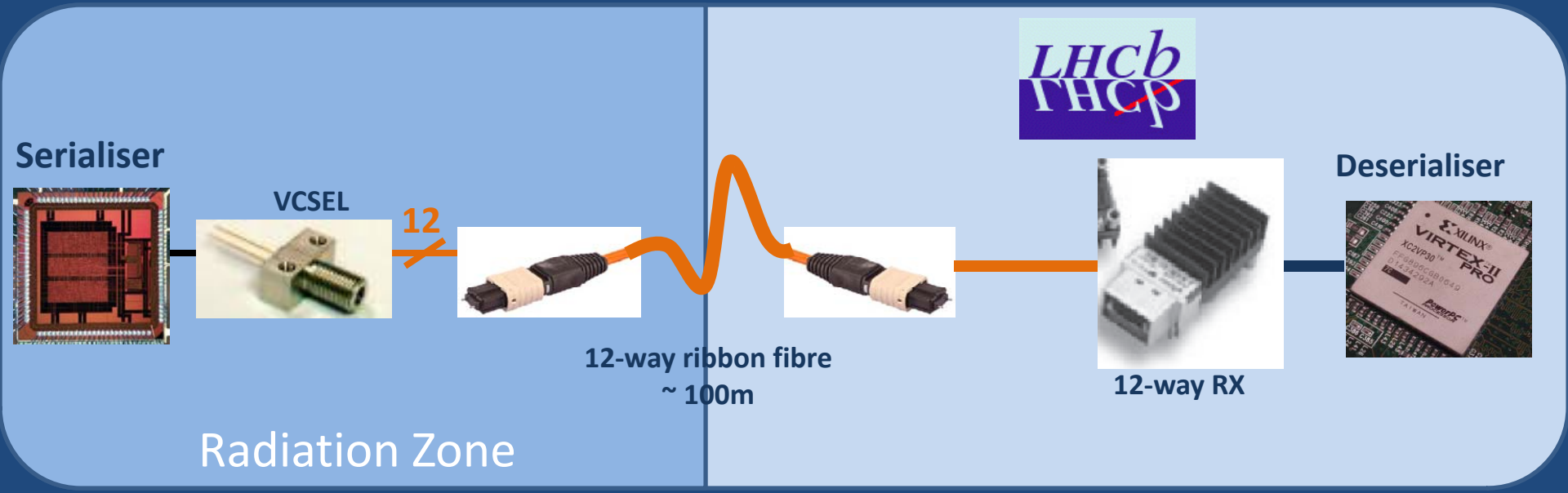
  => Tuneable modulation required



From Jan Troska, CERN

- **Transient effects (photodiode is excellent particle detector!)**
  ..... See later

Example from particle physics



Custom Serialiser Chip	Radiation-tolerant design for HEP
Vertical Cavity Surface Emitting Laser	Commercial device, radiation qualified
1.6 Gbit/s serial data	Line coding 8b/10b for DC balance
5000 channels	850nm, multi-mode 50/125 fibre

Future developments & references

- **Bandwidth needs continually rising**
  - a common solution is parallelism of 10Gbit/s
- **In HEP, radiation always a constraint**
  - BUT selected opto devices appear robust
- **Electronics to transmit (& receive) are complex**
  - high speed, error correction, rad-tolerance.... (this talk)

TIPP talks on optoelectronics
Xiang, Strang, Liu later this morning
Thanks to Francois Vasey & Jan Troska, CERN

The Gigabit Transceiver (GBT) project

On behalf of collaborators at CERN, CPPM, Torino, SMU

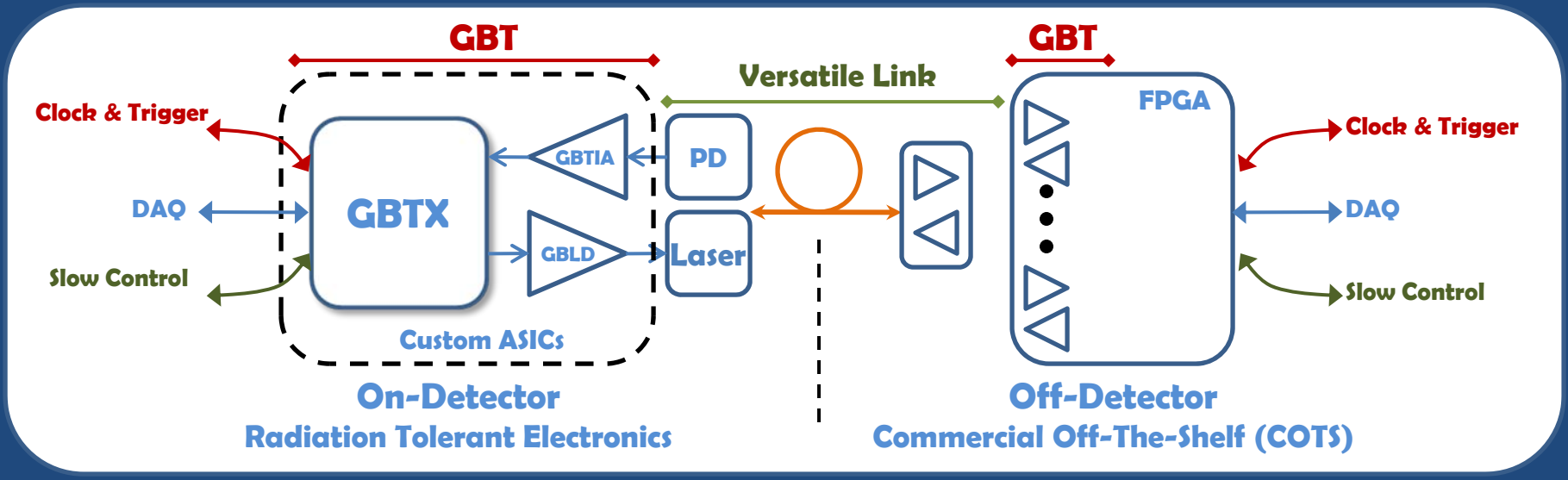
Motivation

- Data volume from detectors will only increase
- Power (& material) budgets cannot increase
- Transmission of Data, Slow-controls, Clock/Trigger

Develop a data link: minimal power
high bandwidth
radiation-tolerant
bi-directional & versatile
compact

Benefit from advances in optoelectronics industry
Maturity of deep sub-micron CMOS in HEP

Concept



Sister project: Versatile Link to develop optoelectronic components (see Xiang)

Constraints

Link robustness

Constant latency

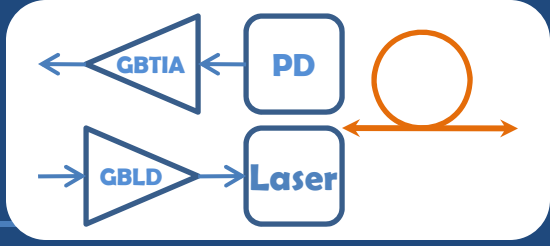
Versatility

Radiation tolerance
triple redundancy (reduced bit rate)
error correction (reduced bandwidth)
phase locked loop current (higher power)
130nm CMOS for tolerance to ionising rad

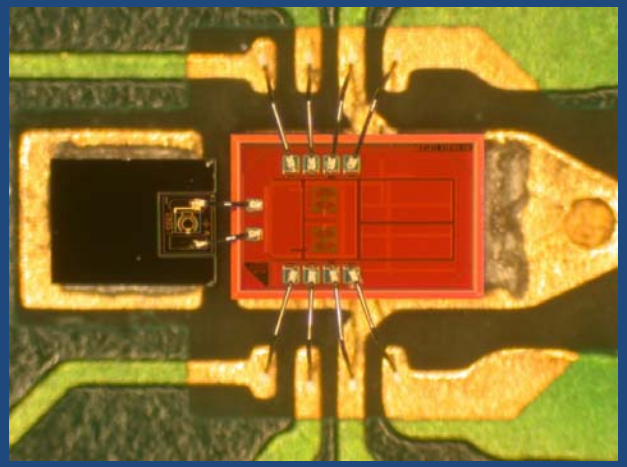
Not an issue in industry!
Implications on clock/data recovery

Drive different types of laser
Interface to different front-end electronics

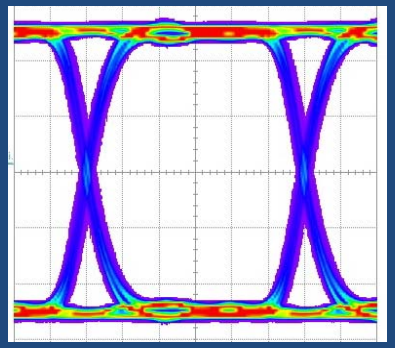
GBTIA & GBLD



Trans-impedance amplifier
Amplify signal from PIN diode

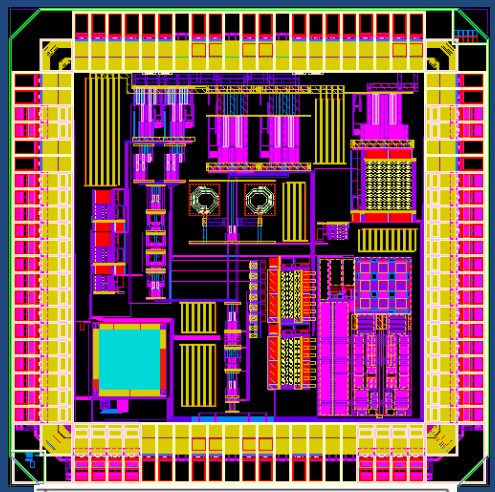


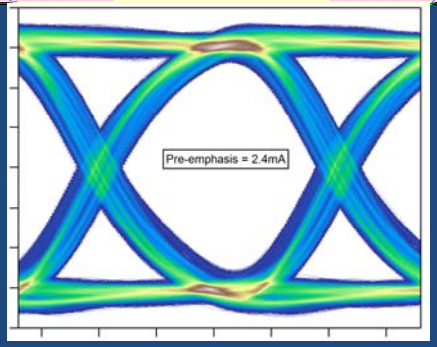
Eye diagram at 5Gbit/s



Fully functional
Tested OK beyond 200Mrad

Laser driver (edge-emitting or VCSEL)
Line equalisation



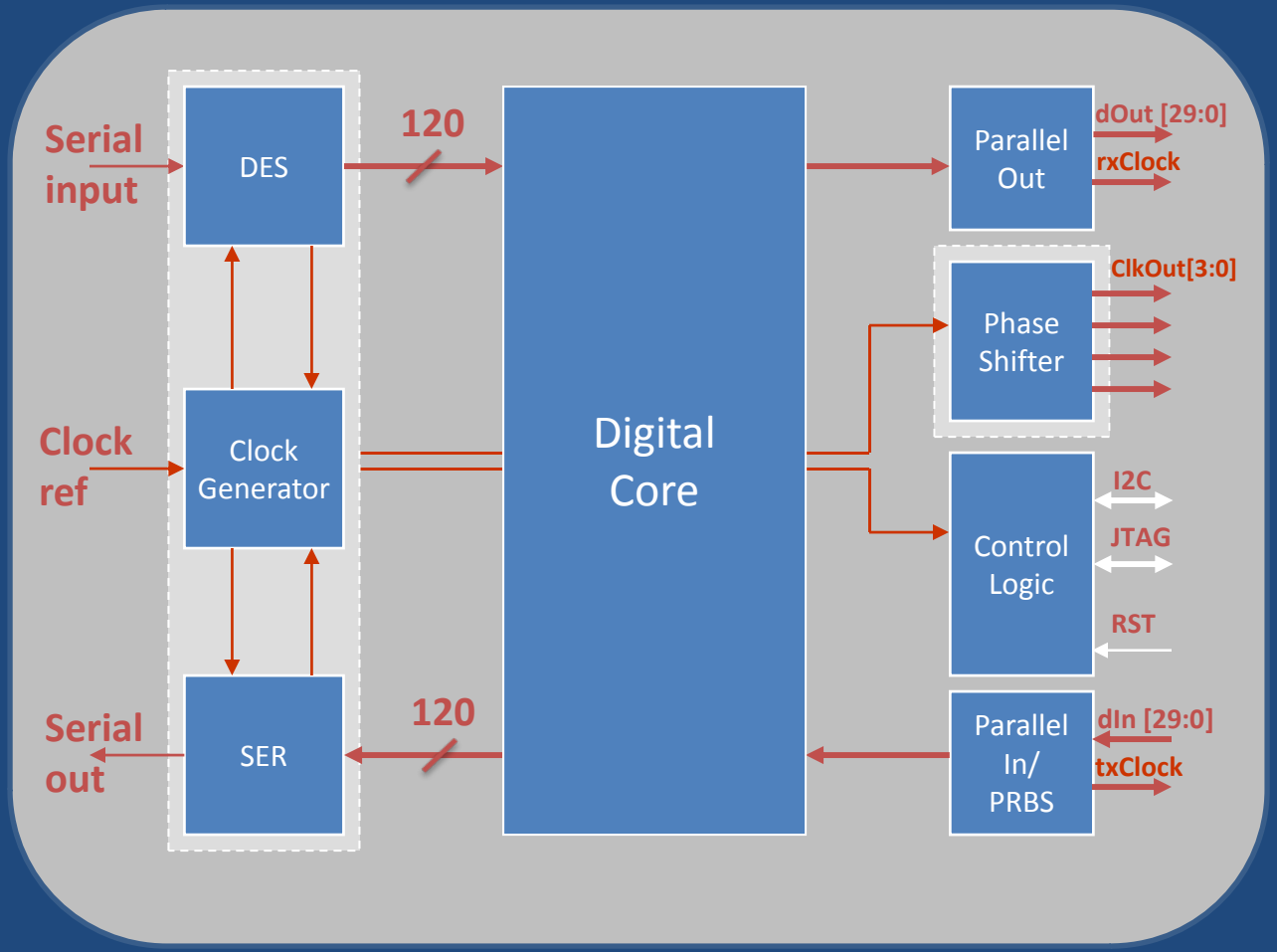


Functional, but some bandwidth limitation
Re-design soon

GBT-SERDES (prototype GBTX)

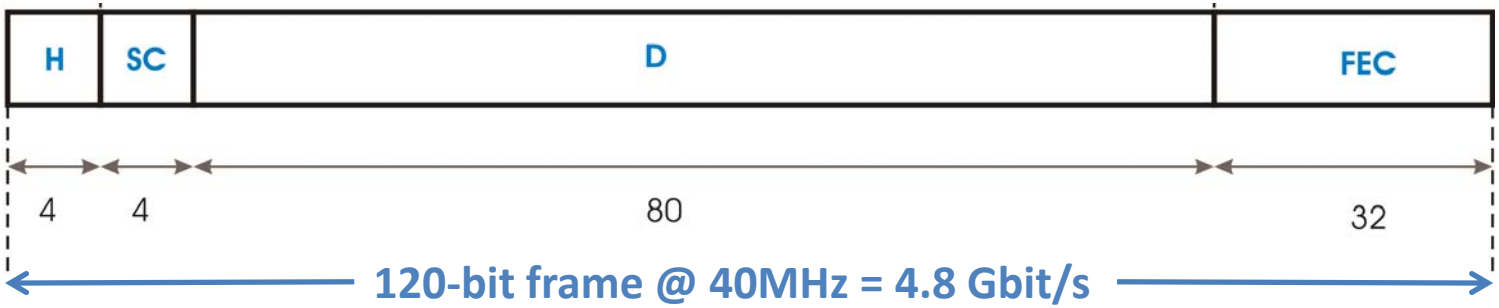
4.8 Gbit/s serial data

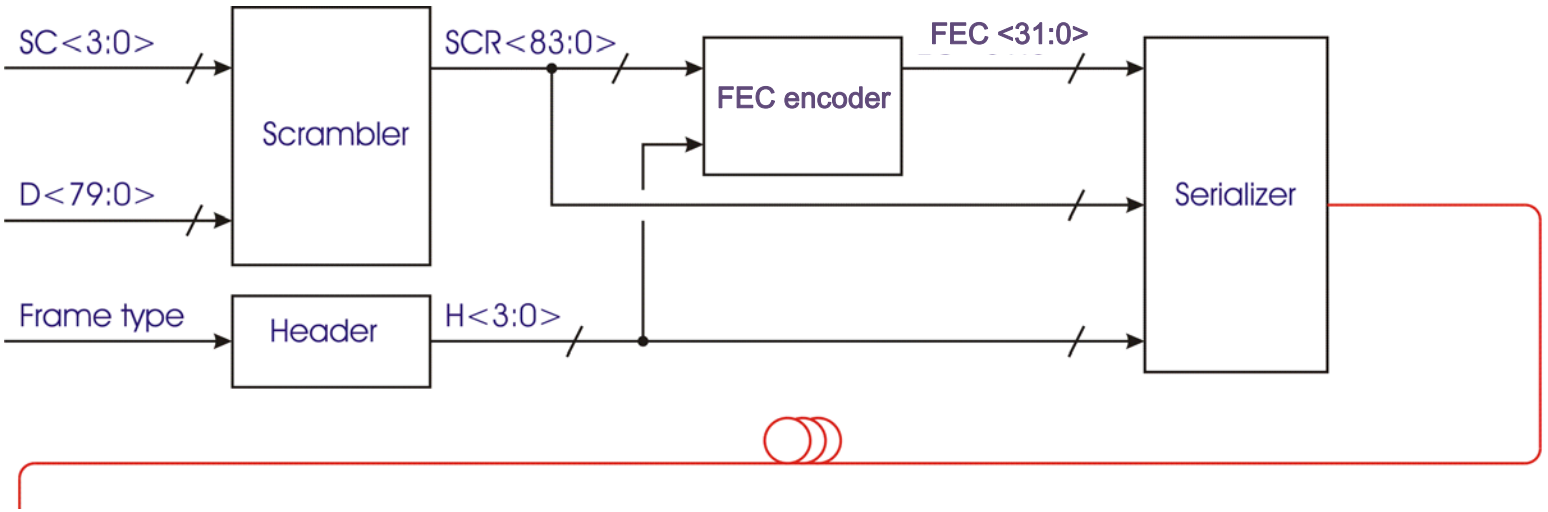
4.8 Gbit/s serial data



60-bit I/O bus 160 MHz

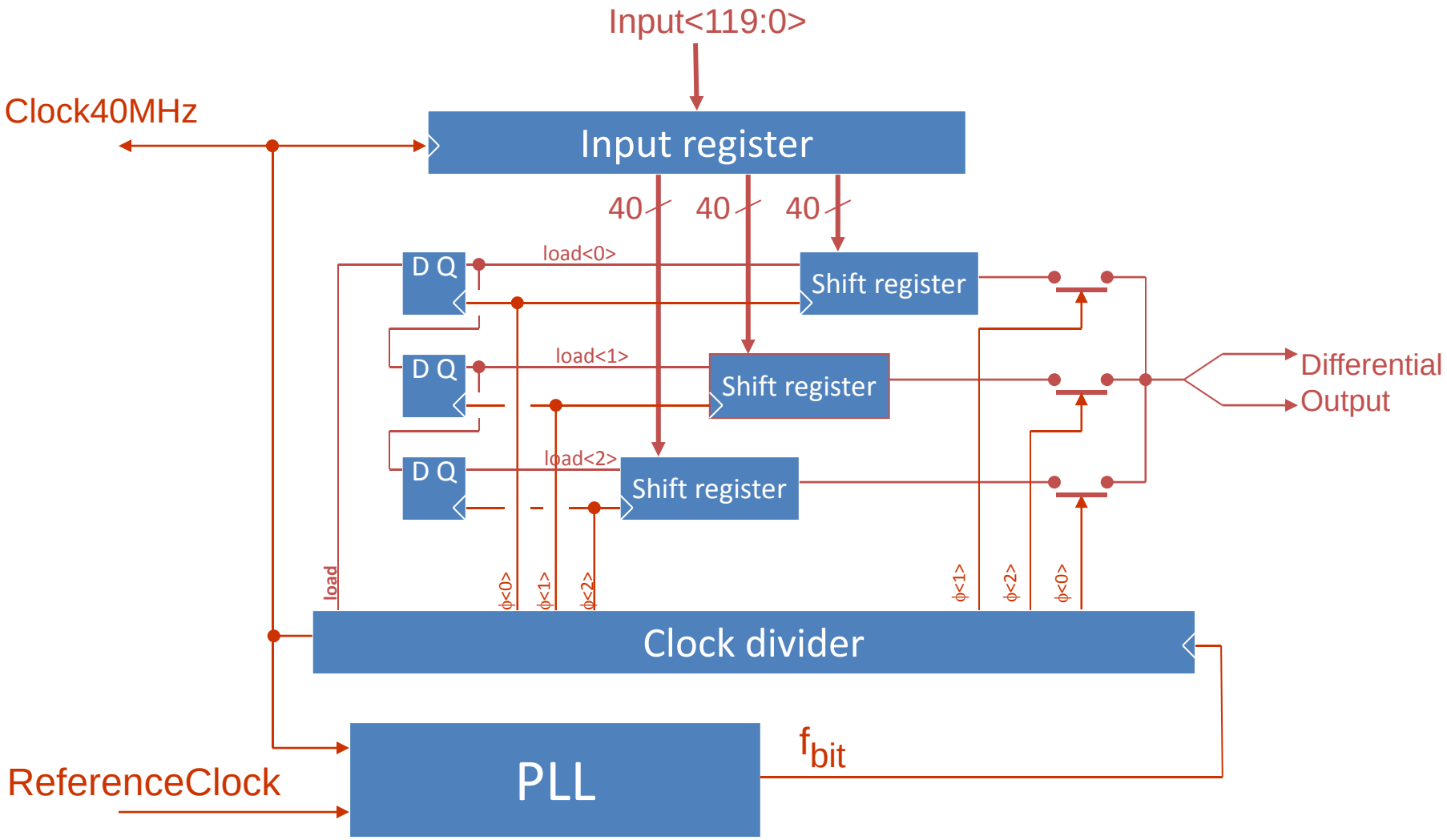
GBT protocol



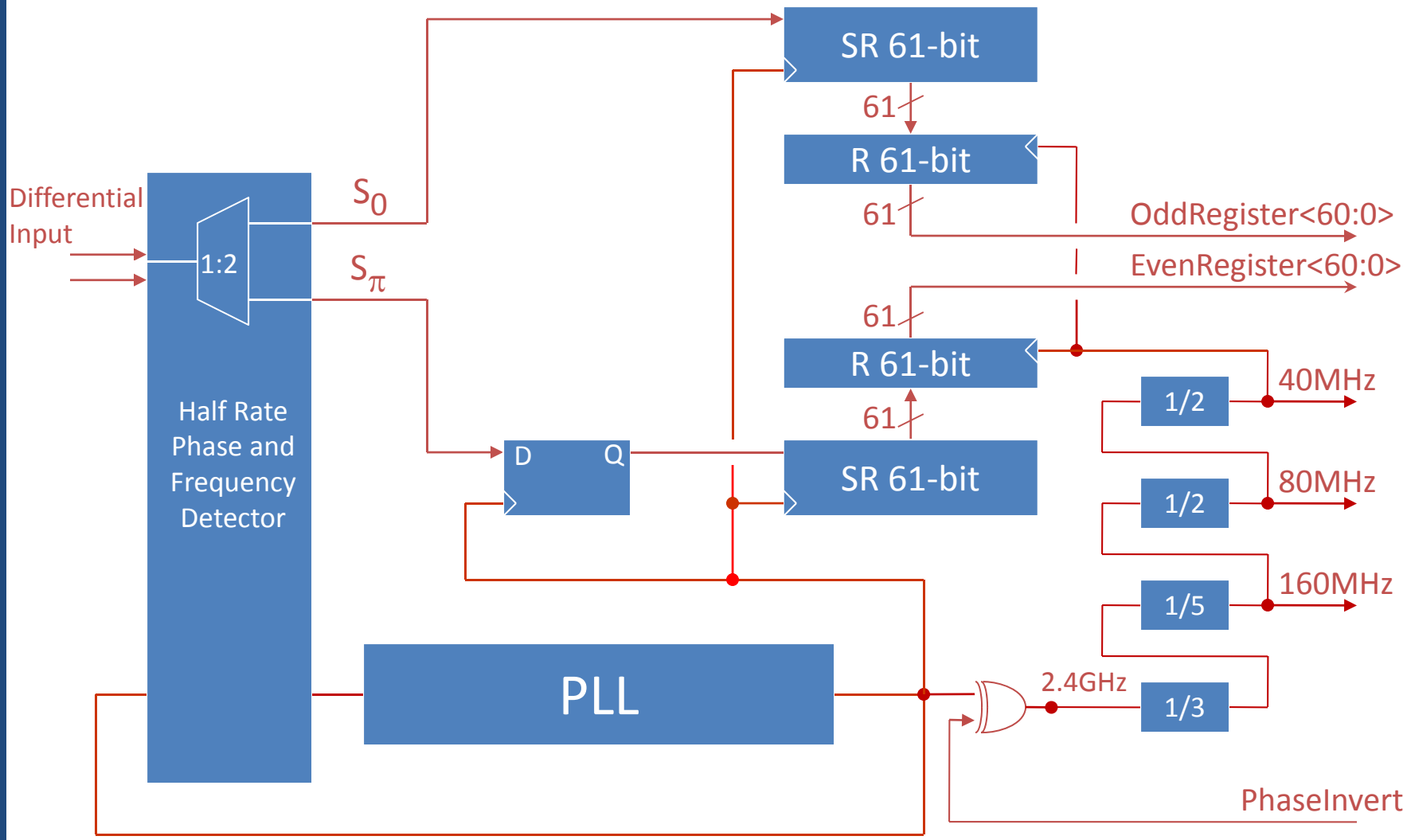


Header: frame synchronisation
Scrambler: DC-balance, transitions for clock recovery
Forward Error Correction: detect & correct errors

SERIALISER


Input<119:0>
Clock40MHz
Input register
40
40
40
load<0>
load<1>
load<2>
D Q
D Q
D Q
Shift register
Shift register
Shift register
Differential
Output
load
ϕ<0>
ϕ<1>
ϕ<2>
ϕ<1>
ϕ<2>
ϕ<0>
Clock divider
ReferenceClock
PLL
f_{bit}

DESERIALISER



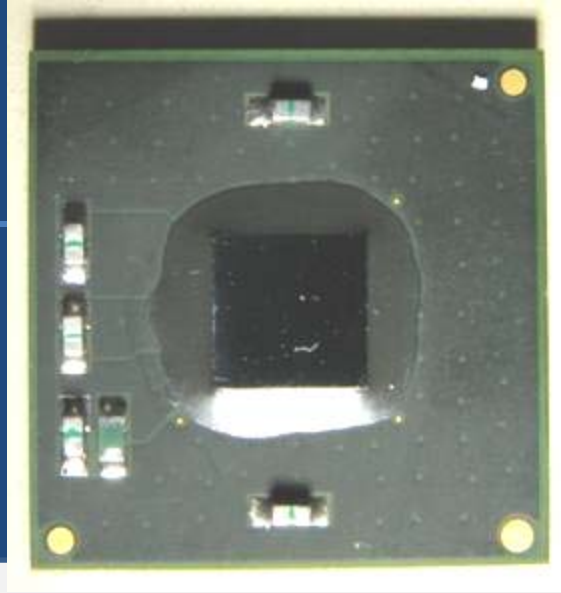
Die & Package

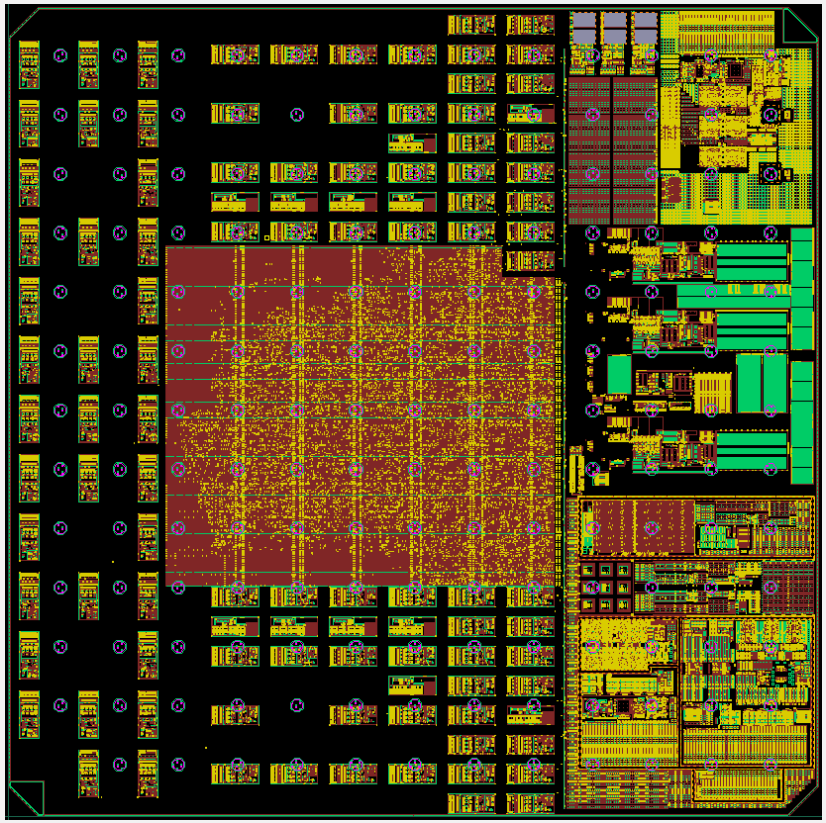
Used flip-chip (C4) interconnects

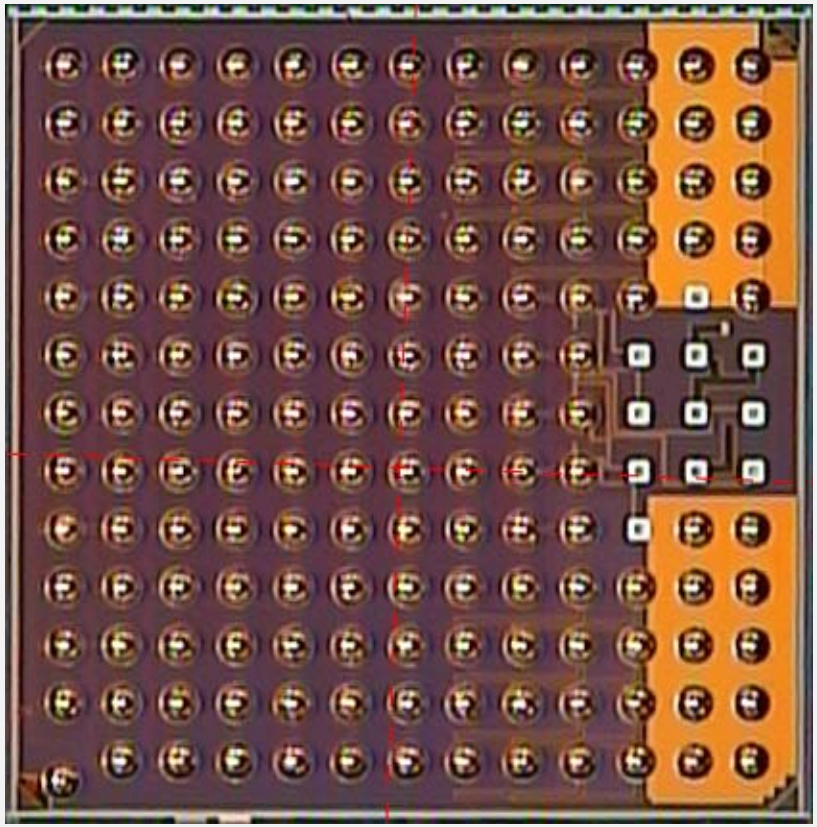
High speed, direct powering to blocks

Direct cooling on back-side

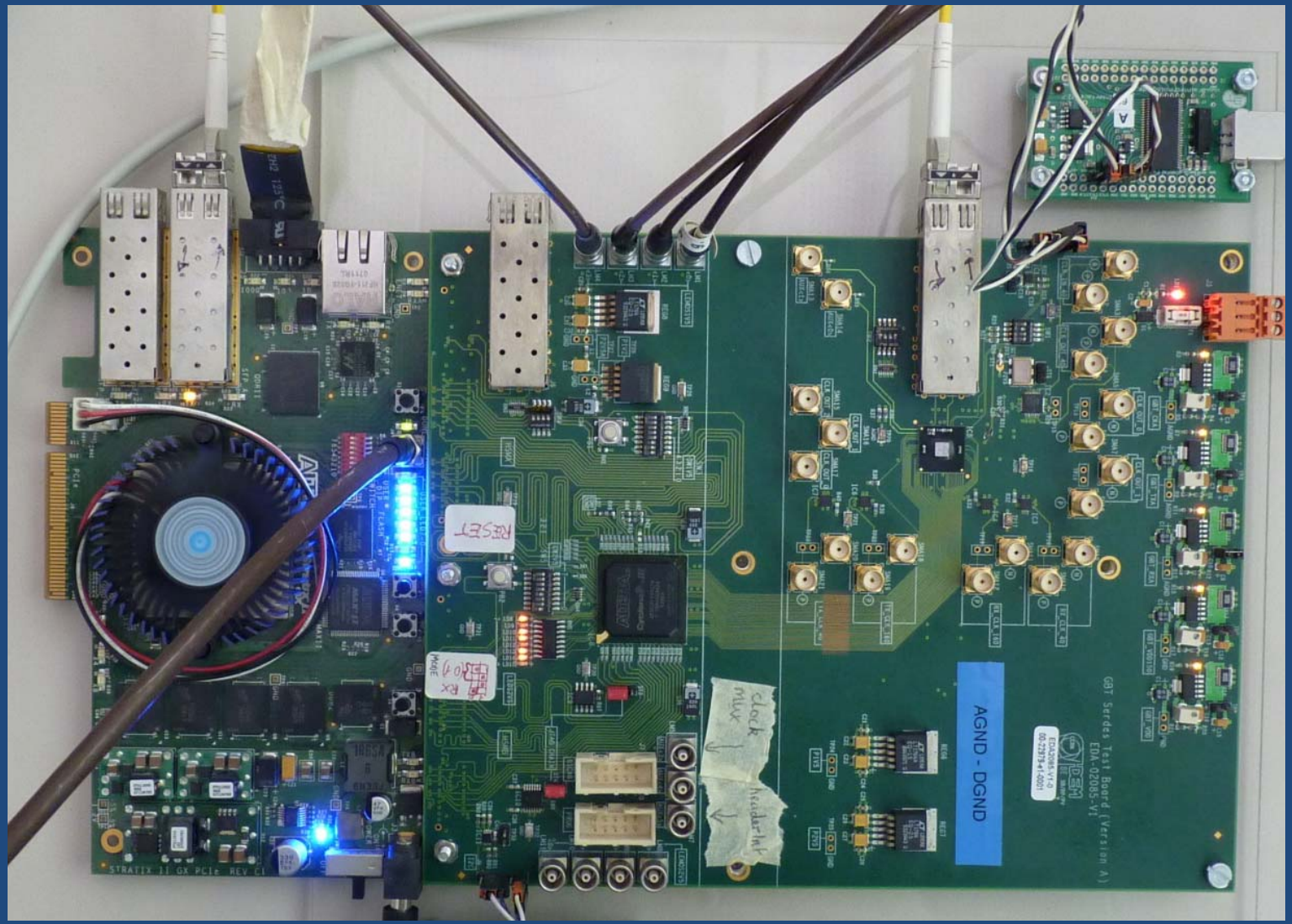
Die size is pad-limited; extra Si (400 I/Os in GBTX)







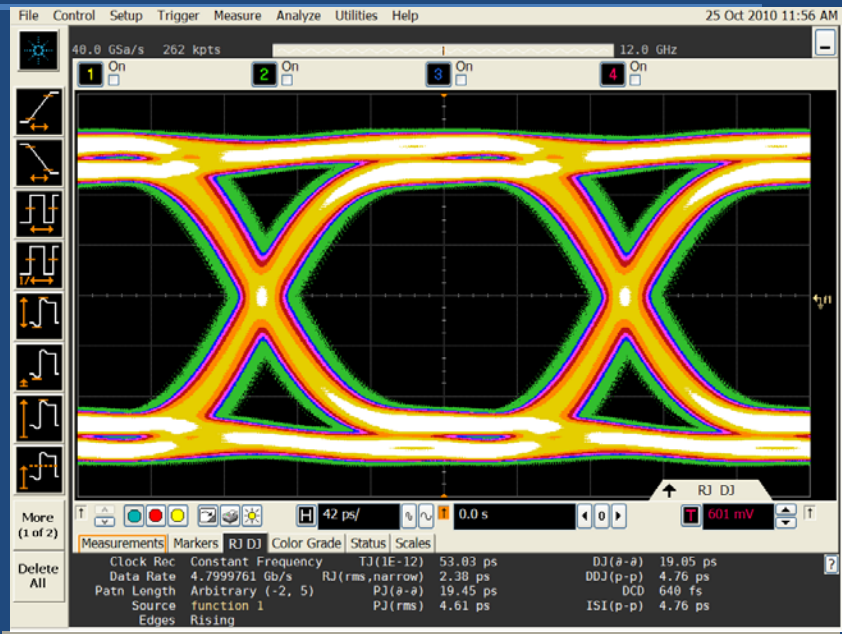
Test System



RESULTS I

Serialiser works well

eg Total jitter = 53ps

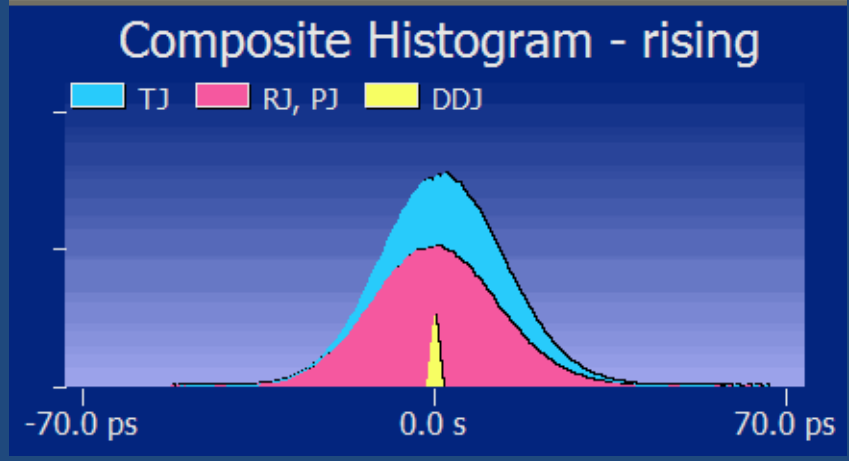


Deserialiser: some problems

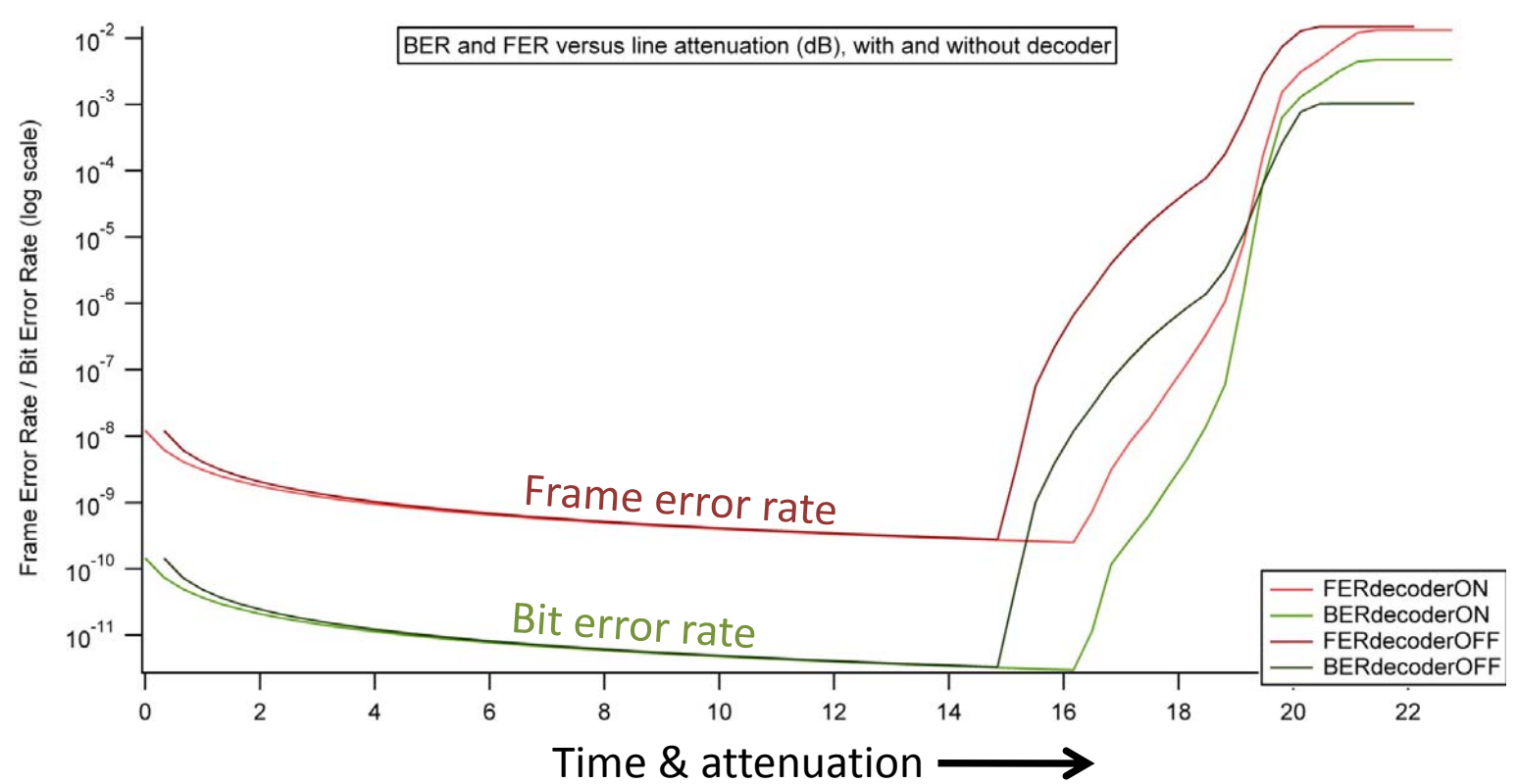
Clock recovery works well

But data errors at 4.8 Gbit/s
No errors below 2.4 Gbit/s

=> Design error found in clock distribution to shift registers



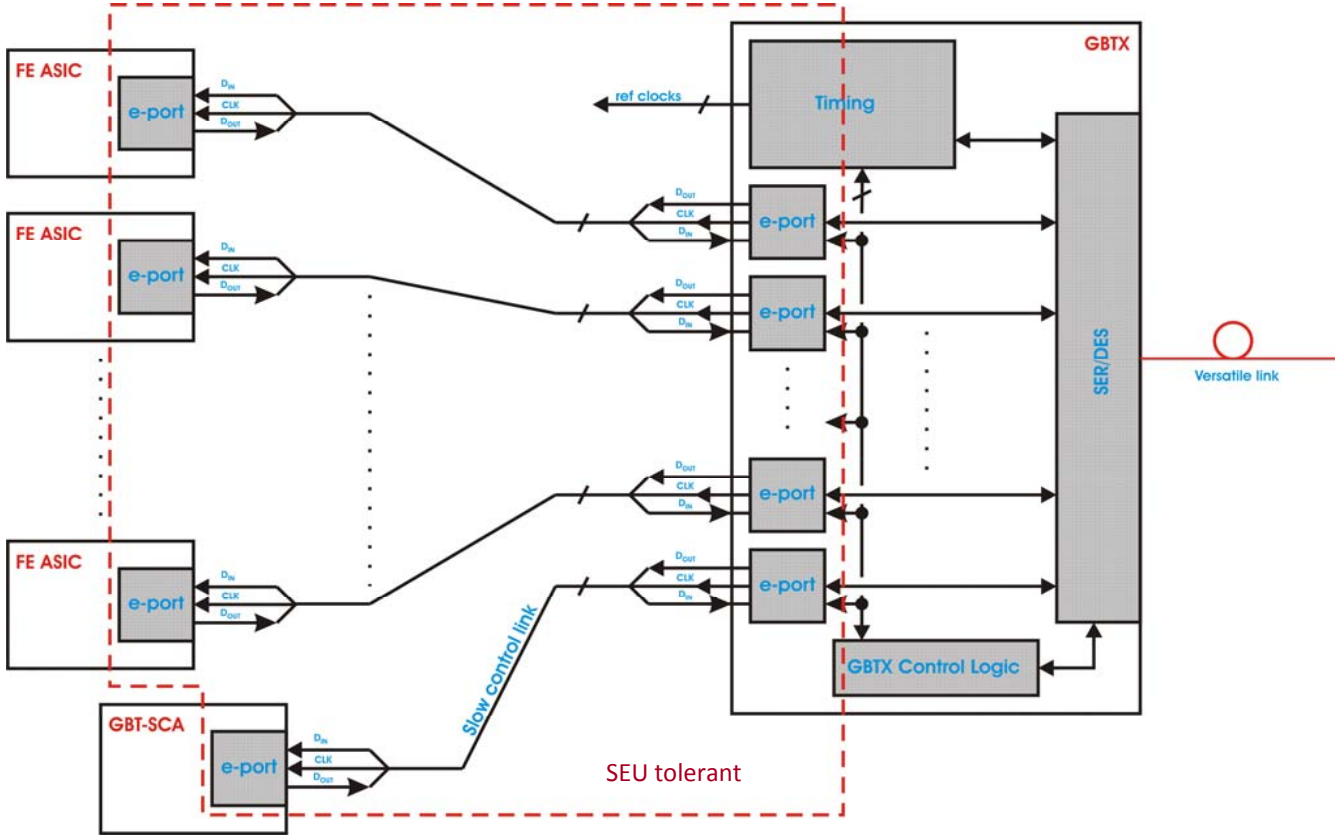
RESULTS II



In transceiver mode
=> transmitting using recovered clock
BERT < 9 x 10^{-16} (time limited!)

Final design

Use Serialiser & corrected Deserialiser
Add versatile interface: parallel/serial modes



Parallel:
40bits @ 80 Mbit

Serial:
40 @ 80 Mbit
20 @ 160 Mbit
10 @ 320 Mbit

Conclusions

Chips in GBT project all prototyped

Bugs found & understood

GBT-SERDES SEU tests ongoing

Final submissions planned for 2011/2012

1st customers: LHC experiment upgrades ~ 2017