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Cold CMOS Electronics for the readout of very large LAr TPCs

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On behalf of the LBNE LAr Working Group

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Outline

- LAr40 overview
- The Cold Electronics System
- Analog Front End
- ADC
- Summary

Other presentations at TIPP 2011 describing LBNE LAr40:

- *[412] Membrane cryostat technology and prototyping program towards kton scale Neutrino detectors,* ***Rucinski***
- *[422] Designs of Large Liquid Argon TPCs — from MicroBooNE to LBNE LAr40,* ***Yu***
- *[223] Front End Readout Electronics of the MicroBooNE Experiment,* ***Chen***

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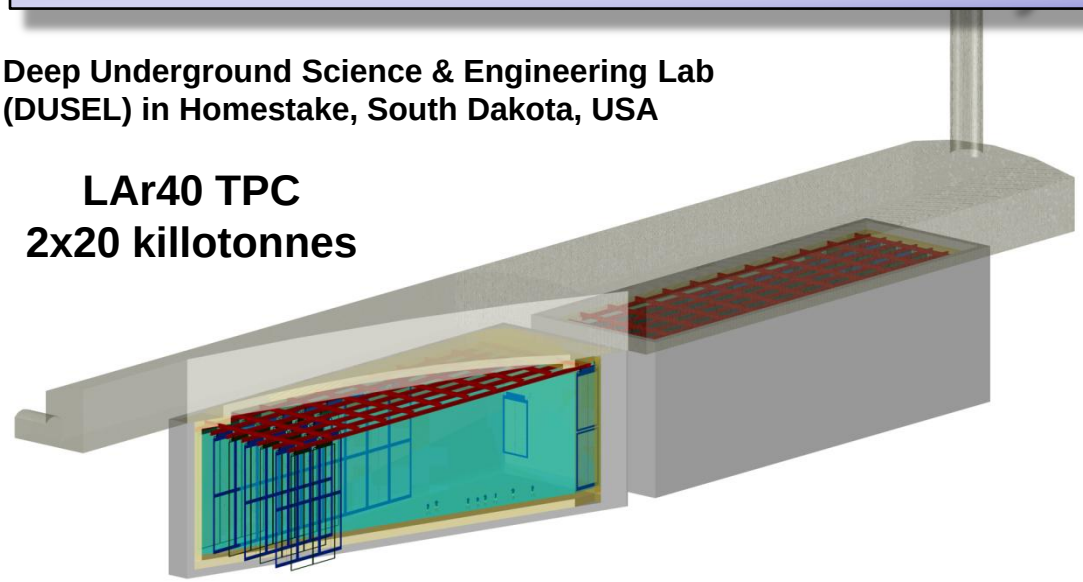
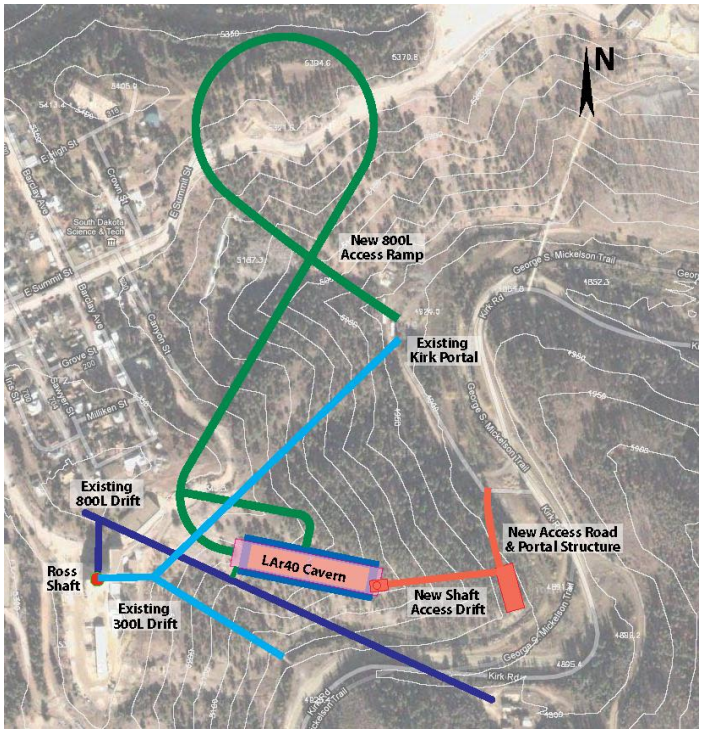
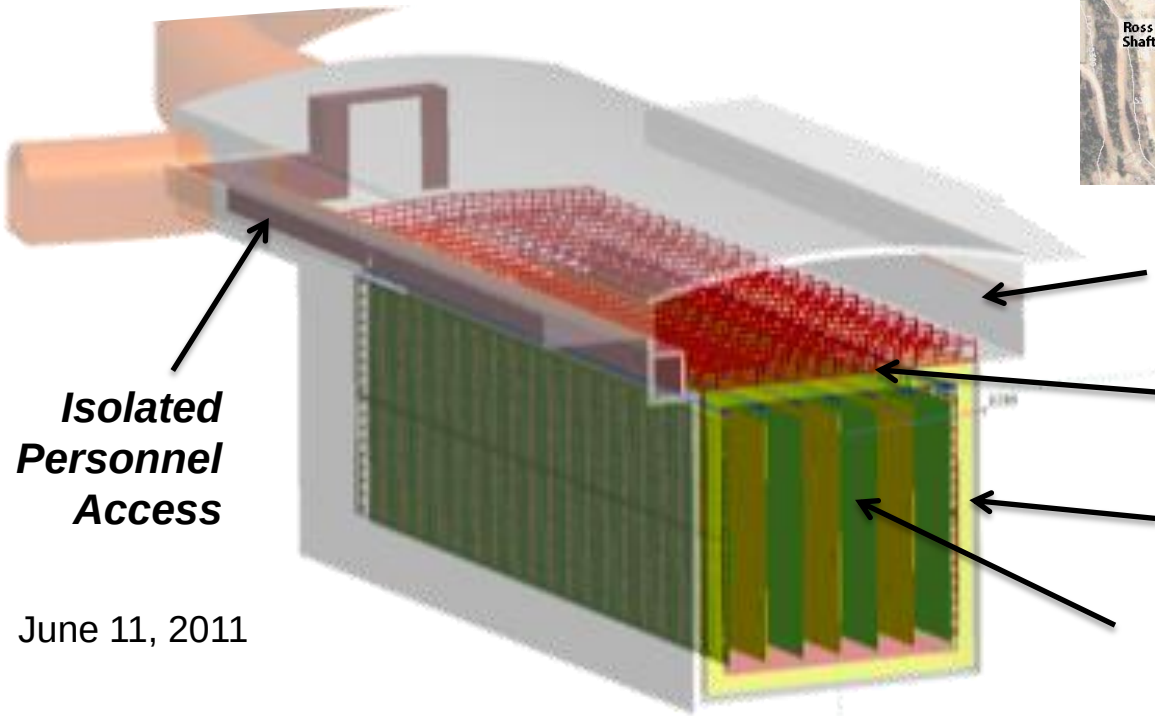
LBNE LArTPC inside Cryostats in Cavern

Deep Underground Science & Engineering Lab (DUSEL) in Homestake, South Dakota, USA

LAr40 TPC
2x20 killotonnes







Isolated Personnel Access

High Bay Access

Truss Lid for Cryostat

Membrane Cryostat

TPC Arrays

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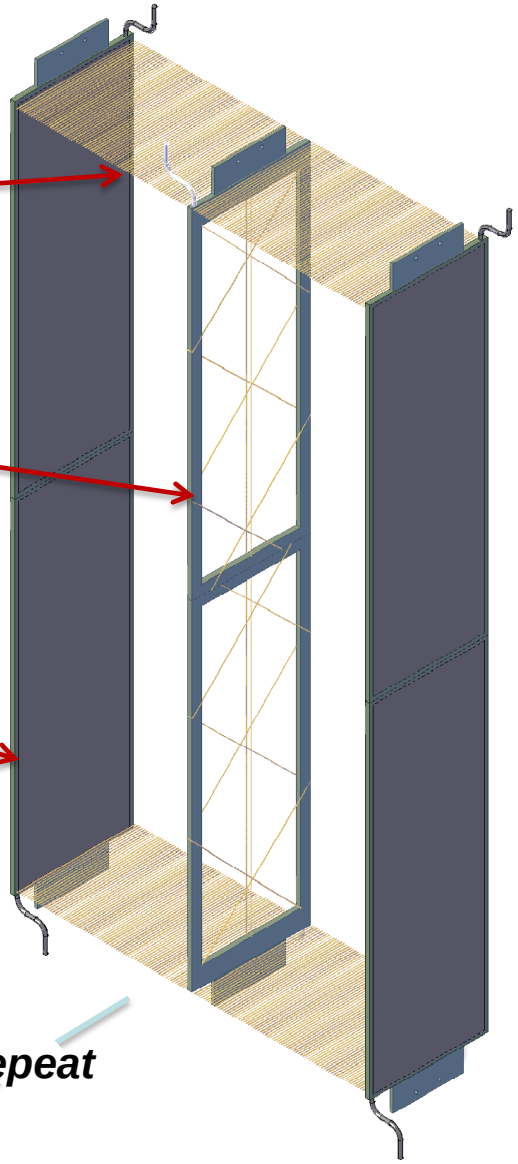
APA + CPA Assemblies form TPC modules in the Cryostat



Field Cage Bars

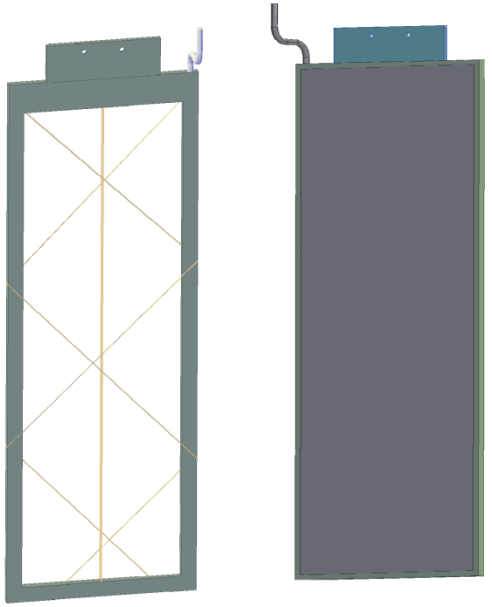
APA = Anode Plane Assembly

CPA = Cathode Plane Assembly

Repeat

Repeat

Unit Cell
TPM = TPC Module
= 1 APA + 1 CPA
(+1 "terminal" CPA)

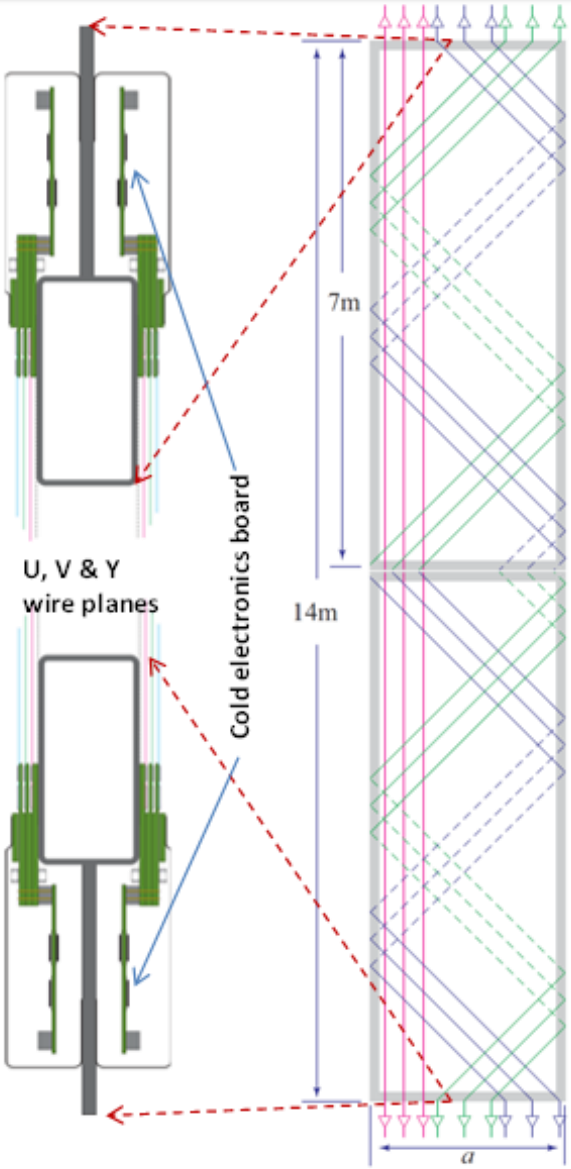


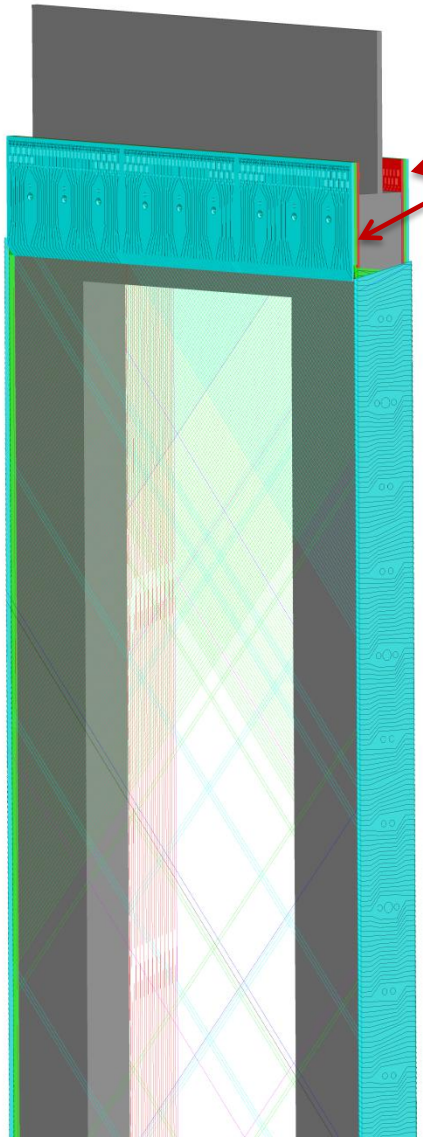
APA

CPA

Volume
~ 0.5 x ICARUS
~2 xMicroBooNE

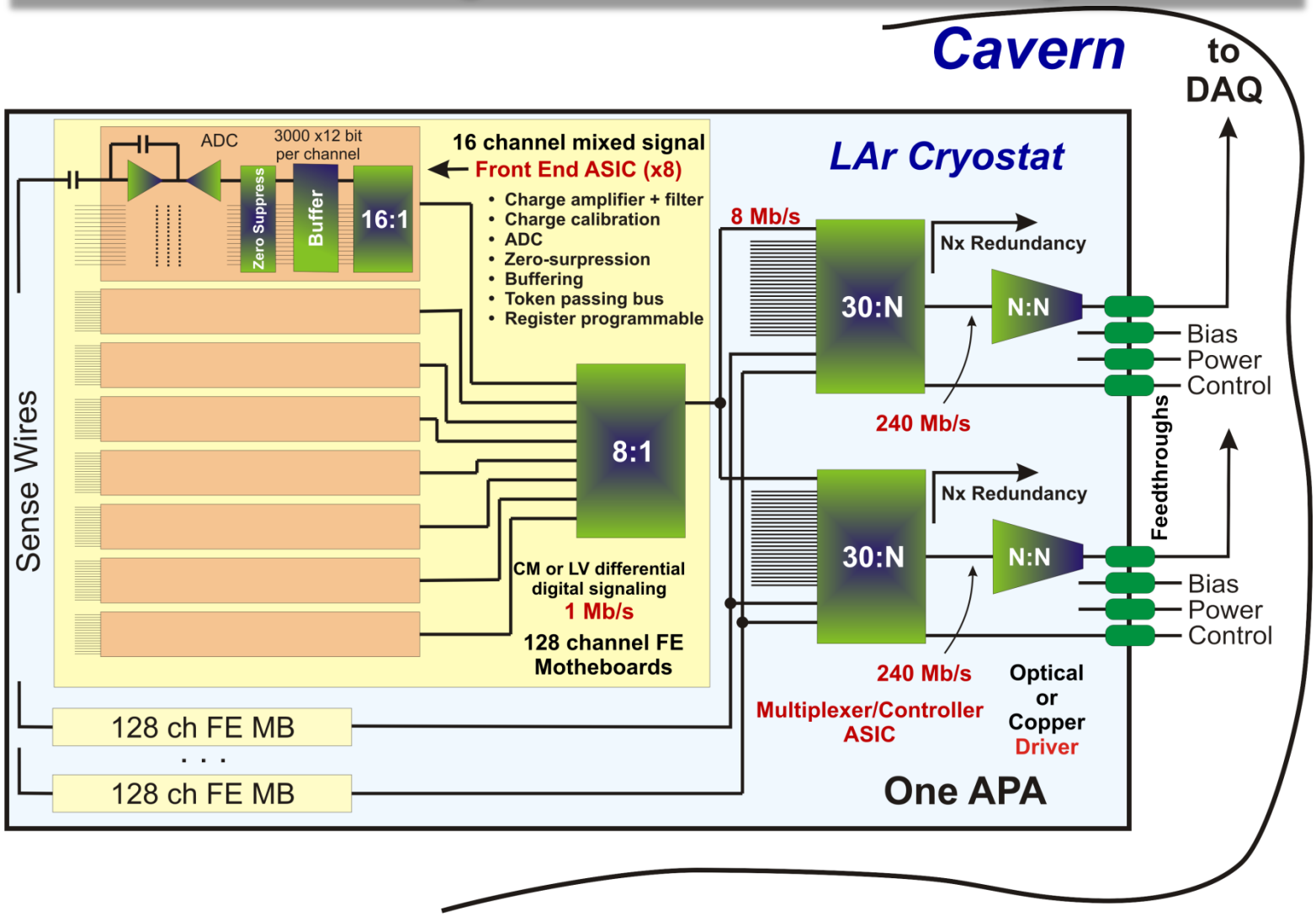
Anode Plane Assembly (APA): the core element of a TPC unit





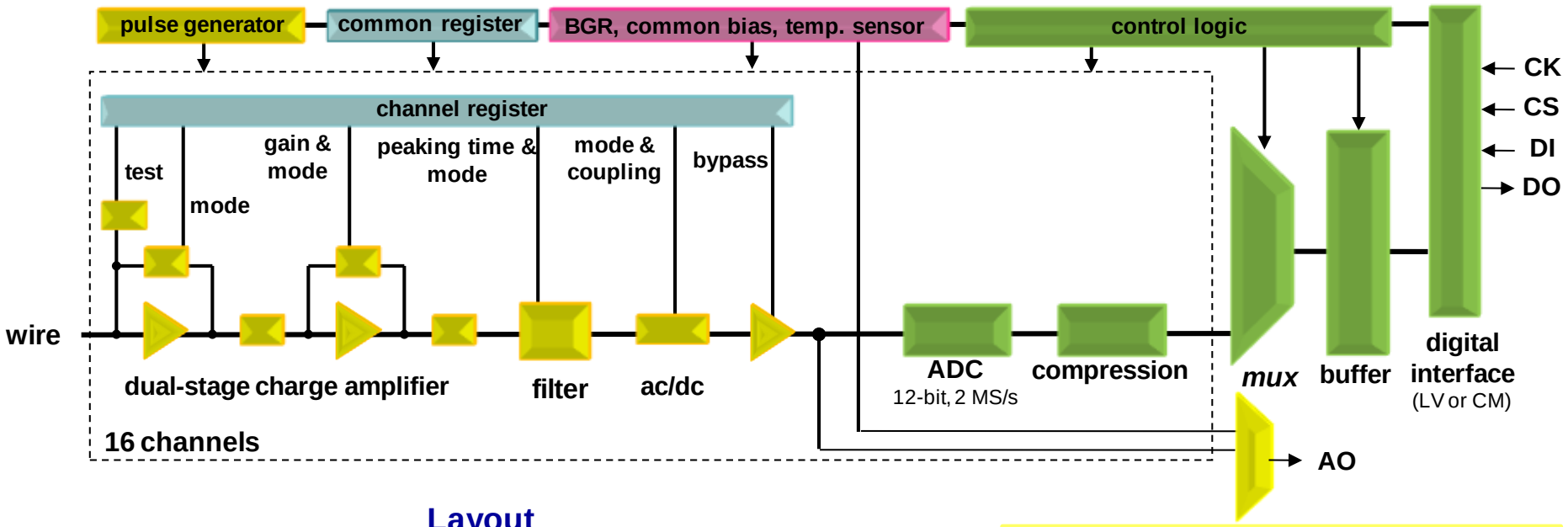
APAs are structural and electrical units containing all sense wires and readout electronics. They can be tested in LN2 and stored and transported in shipping containers.

LAr TPC - Cold CMOS Electronics Block Diagram – Reference Design

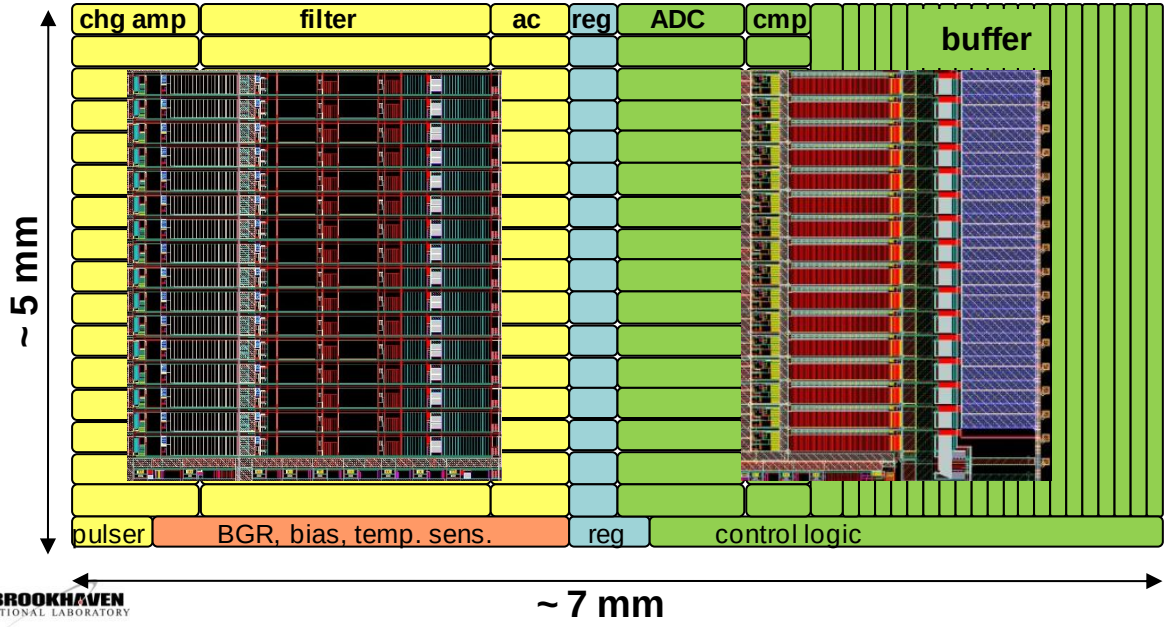


LAr TPC Front-End ASIC

Block Diagram



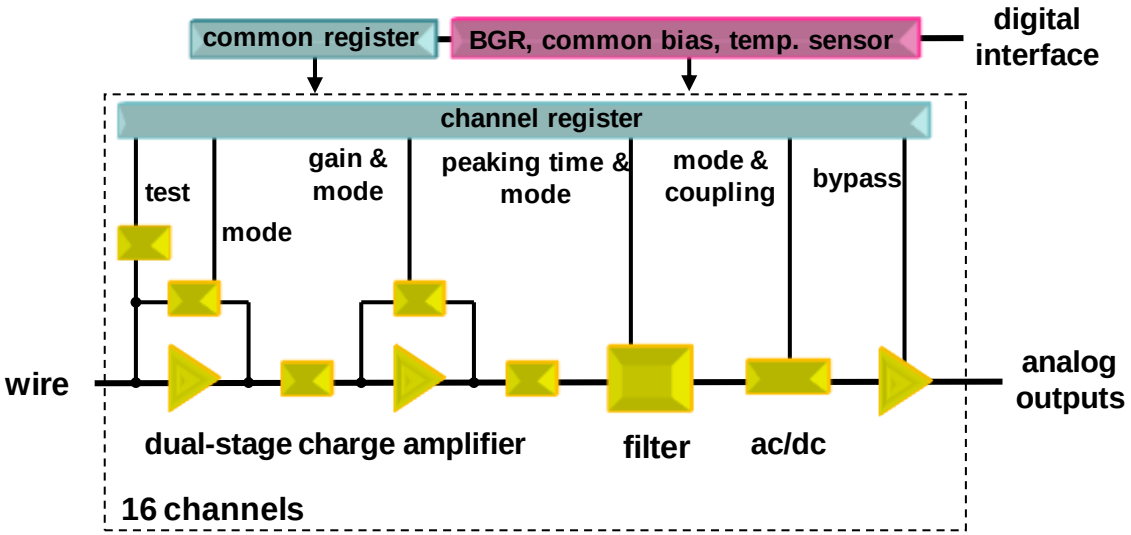
Layout

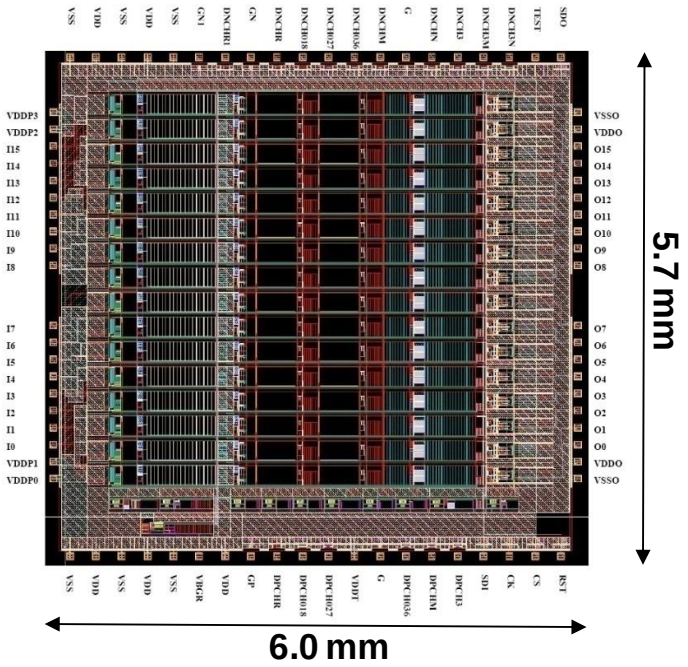


- 16 channels
- charge amplifier (adj. gain)
- high-order filter (adj. time constant)
- ac/dc, adjustable baseline
- test capacitor, channel mask
- ADC (12-bit, 2 MS/s)
- compression, discrimination
- multiplexing and digital buffering
- LV or CM digital interface
- pulse generator, analog monitor
- temperature sensor
- **LAr environment (> 20 years at 88K)**
- estimated total size ~ 6 x 8 mm²
- estimated power ~ 10 mW/channel

Analog ASIC

Block Diagram





- 16 channels
- charge amplifier, high-order filter
- adjustable gain: 4.7, 7.8, 14, 25 mV/fC
  (charge 55, 100, 180, 300 fC)
- adjustable filter time constant
  (peaking time 0.5, 1, 2, 3 μs)
- selectable collection/non-collection mode
  (baseline 200, 800 mV)
- selectable dc/ac coupling (100μs)

- rail-to-rail analog signal processing
- band-gap referenced biasing
- temperature sensor (~ 3mV/ C)
- 136 registers with digital interface
- 5.5 mW/channel (input MOSFET 3.9 mW)
- single MOSFET test structures
- ~ 15,000 MOSFETs
- designed for room (300K) and cryogenic (77K) operation
- technology CMOS 0.18 μm, 1.8 V

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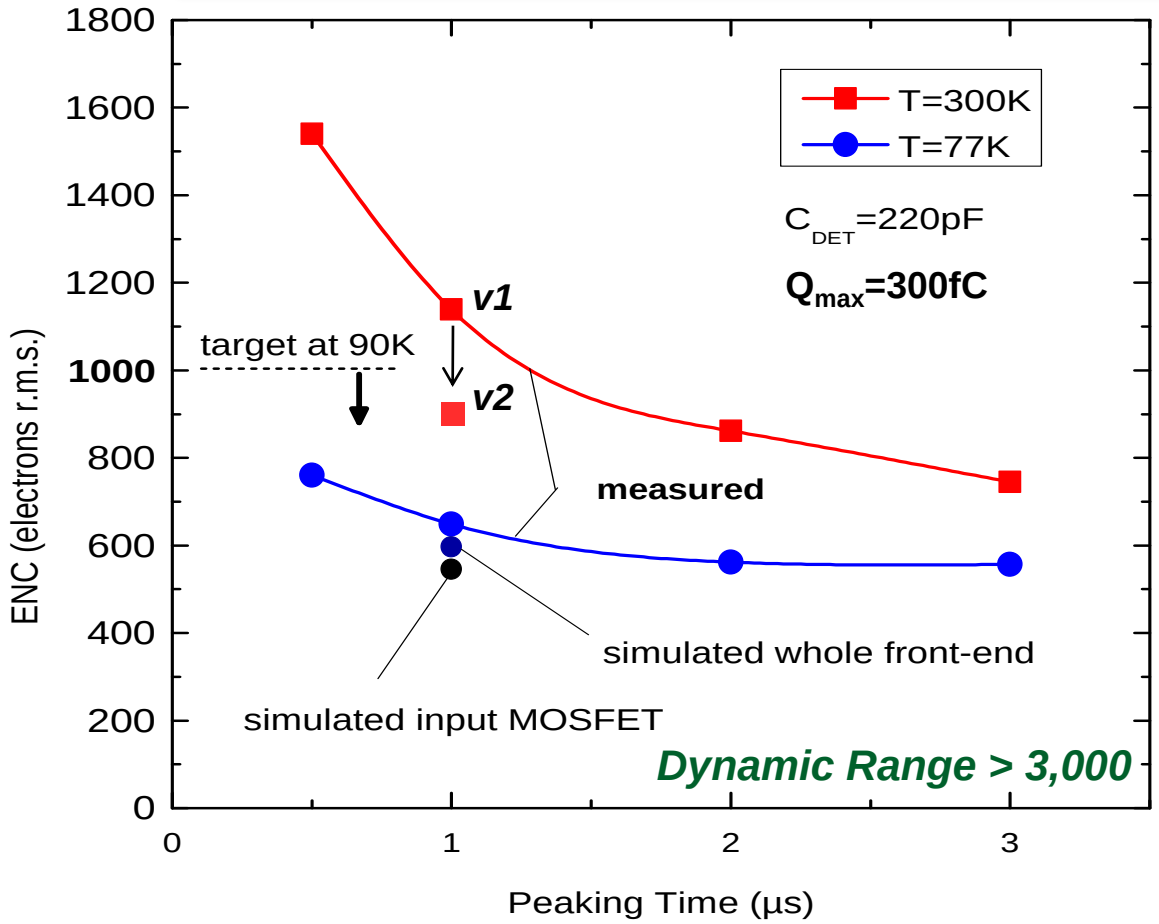
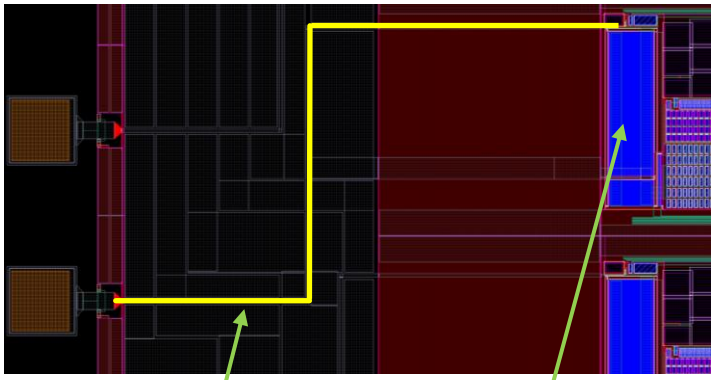
Noise Measurements

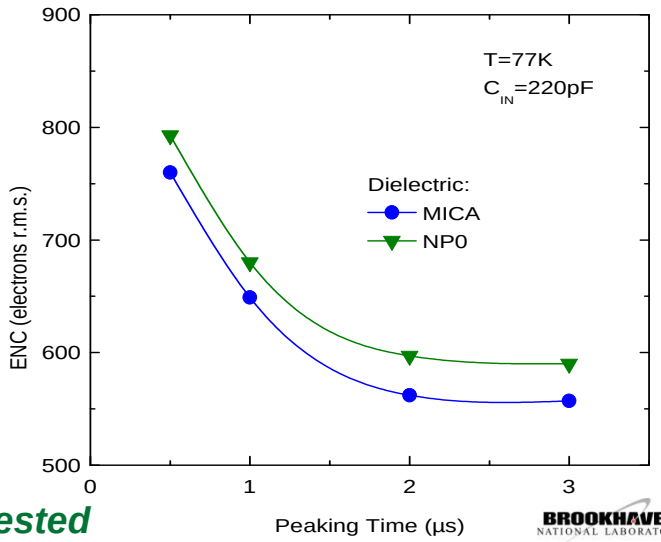


Layout Detail



Input Line
L ≈ 1 mm
W = 3.5 µm
(M3 + M4)
R_{77K} ≈ 3 Ω
R_{300K} ≈ 12 Ω

Input MOSFET
L = 270 nm
W = 10 mm
(50µm x 200)
$g_{m,77K}$ ≈ 90 mS (11 Ω)
$g_{m,300K}$ ≈ 45 mS (22 Ω)



Measurements affected by:

- **input line parasitic resistance**
  - **~ 150 e⁻ at 77 K (~ 590 e⁻ at 300K)**
  - **addressed in next revision**
- **C_{IN} dielectric noise (not present in wire)**
  - **~ 60 e⁻ at 77 K**

$$dENC \approx \sqrt{2kTC_{IN}tg\delta} \approx \begin{cases} 200\,e^- \text{ for NPO} \\ 60\,e^- \text{ for MICA} \end{cases}$$

ASIC revision 2 designed and fabricated, currently being tested

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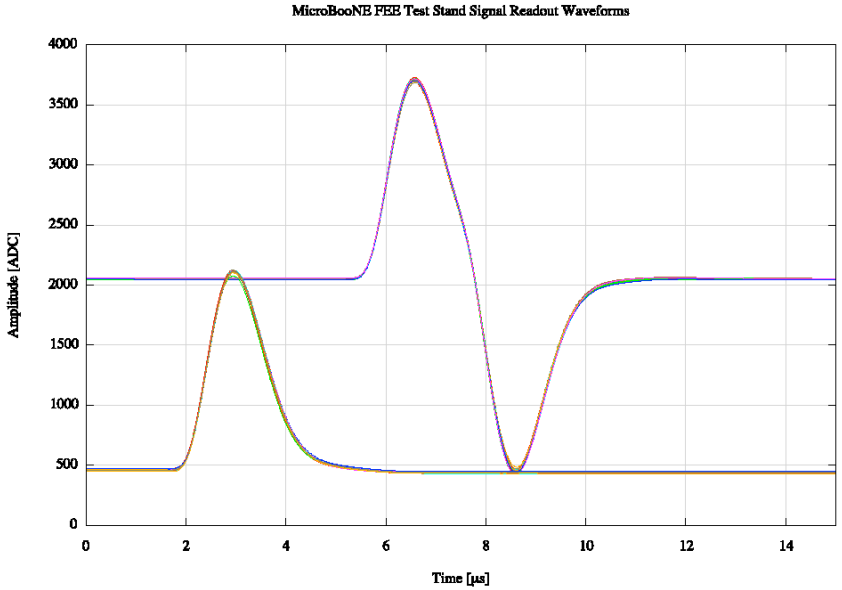
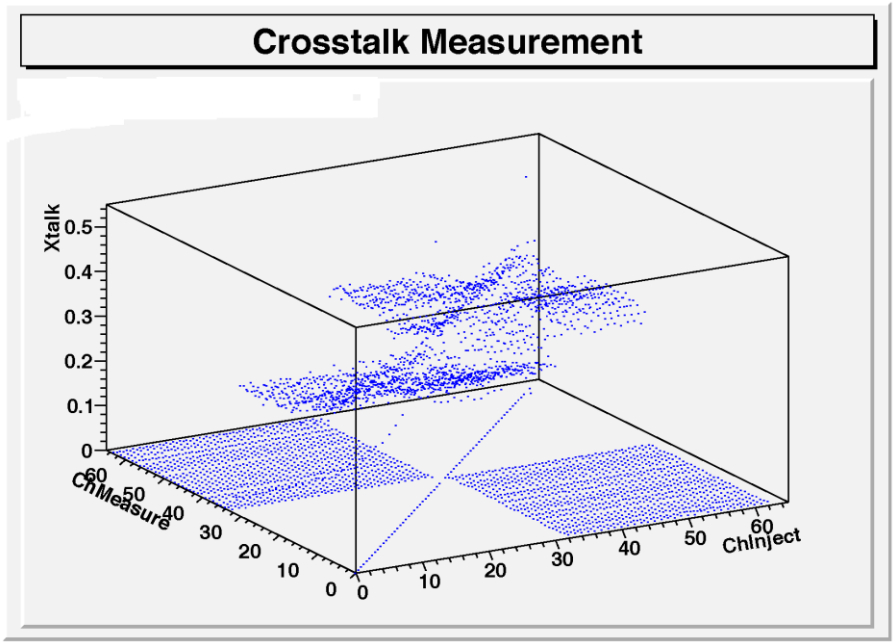
FEE ASIC Evaluation





FEE Test Stand for MicroBooNE is operational

- **Full front end electronics chain, from CMOS ASIC to Receiver/ADC board, data is acquired to PC through FPGA board and Gigabit Ethernet**
- **One temporary 32 channel cold cable is available which has one broken channel**
- **Without detector capacitance, noise is ~200e$^-$ with 1us peaking time**
- **Nonlinearity and crosstalk are less than 0.5%**
- **FEE test stand will be upgraded with the second version of ASICs and two prototype cold cables, more tests to follow**

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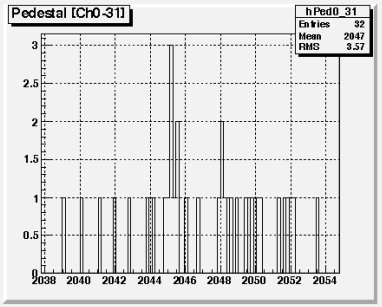
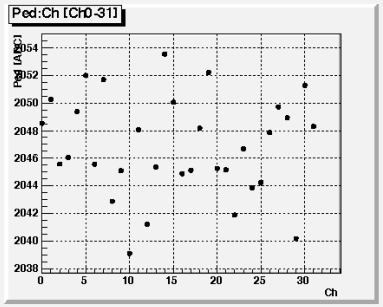
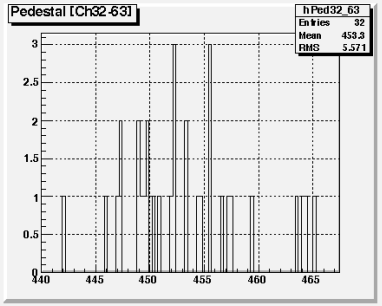
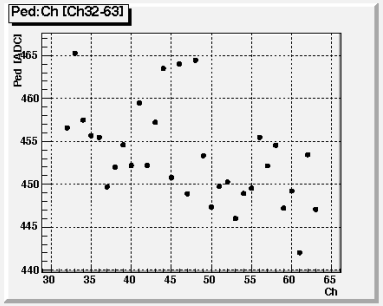
FEE Analog ASIC Evaluation
Noise, Gain & Shaping Time

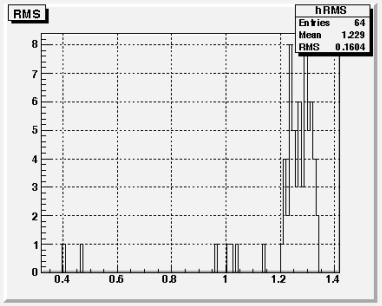
Noise Measurement

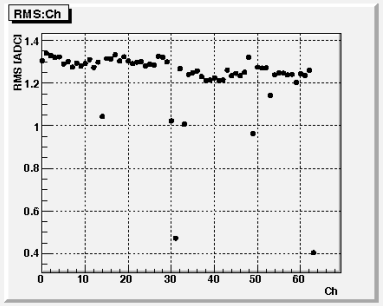




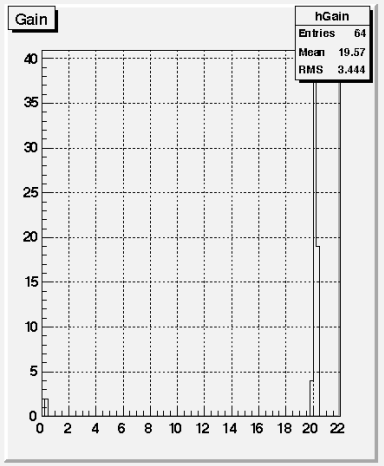


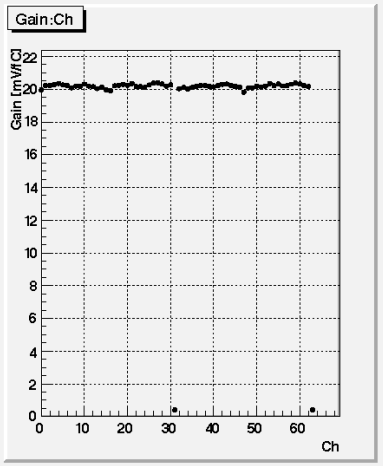


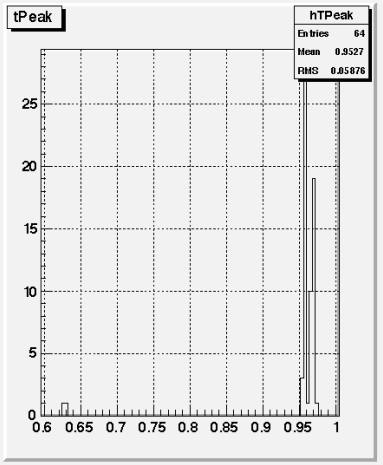


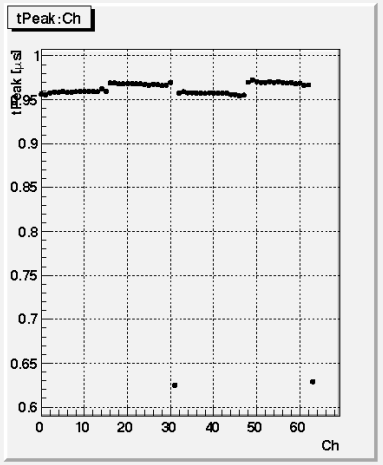


Gain & Peaking Time Measurement









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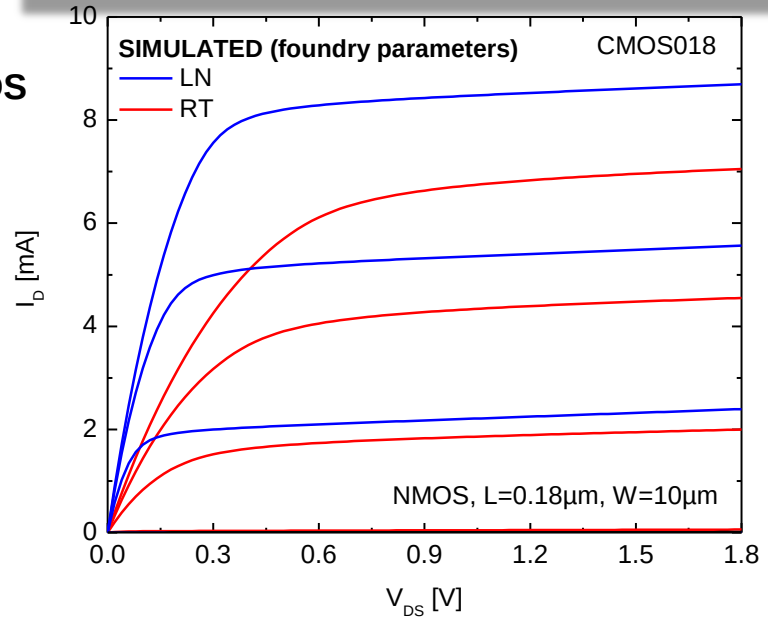
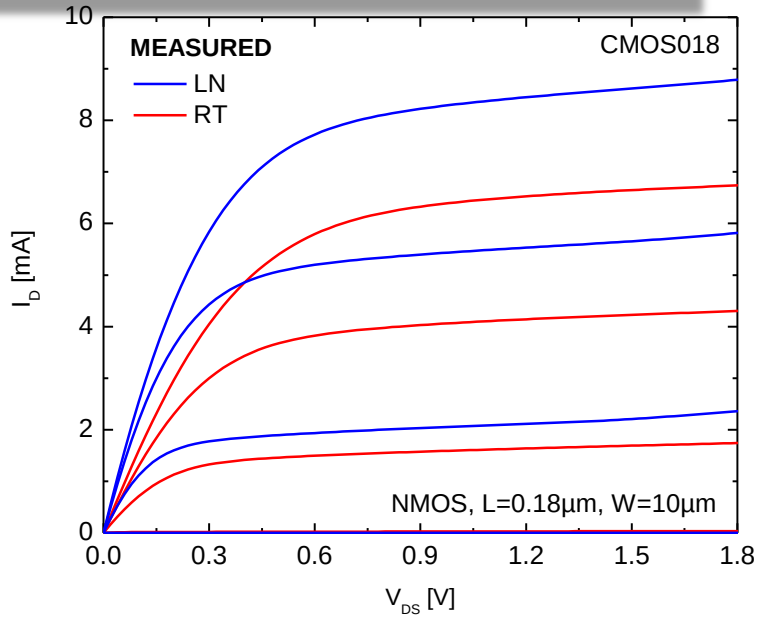
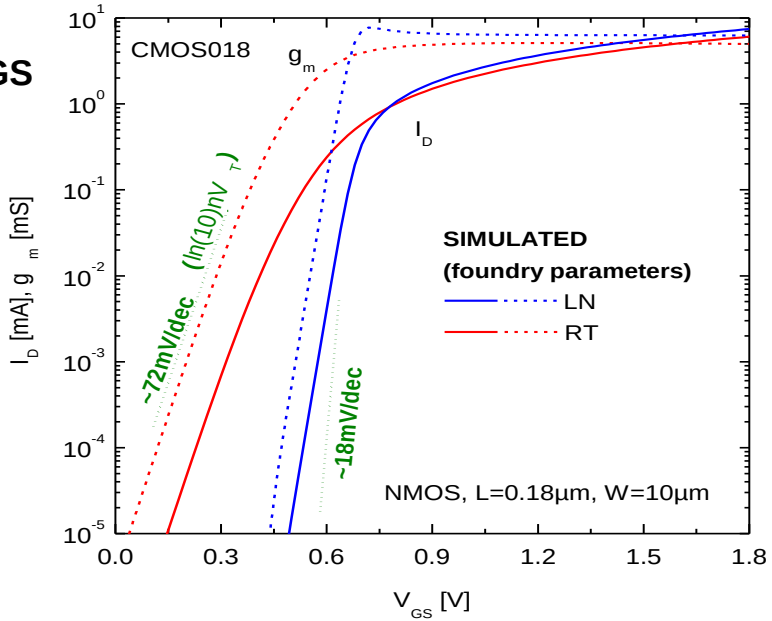
MOS Static Model

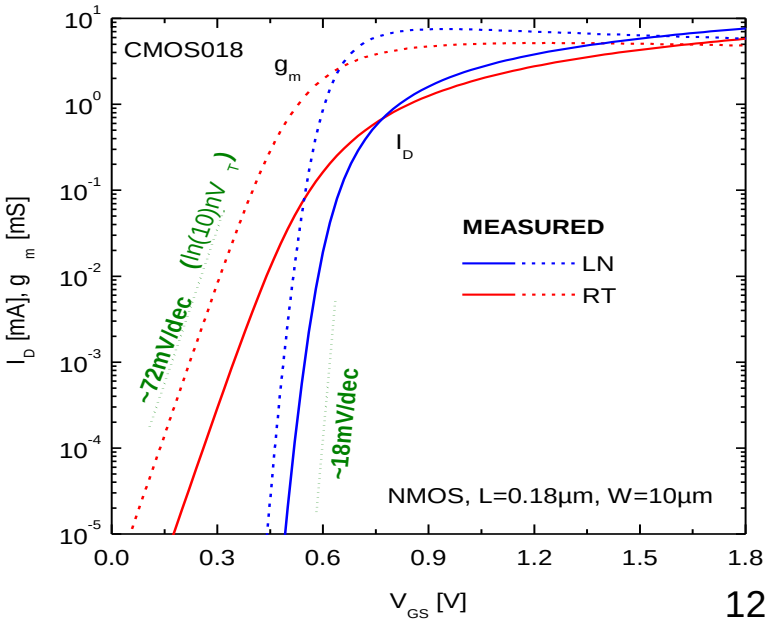
I_D vs V_{DS}





I_D vs V_{GS}





Some differences in saturation voltage, sub-threshold slope, transconductance

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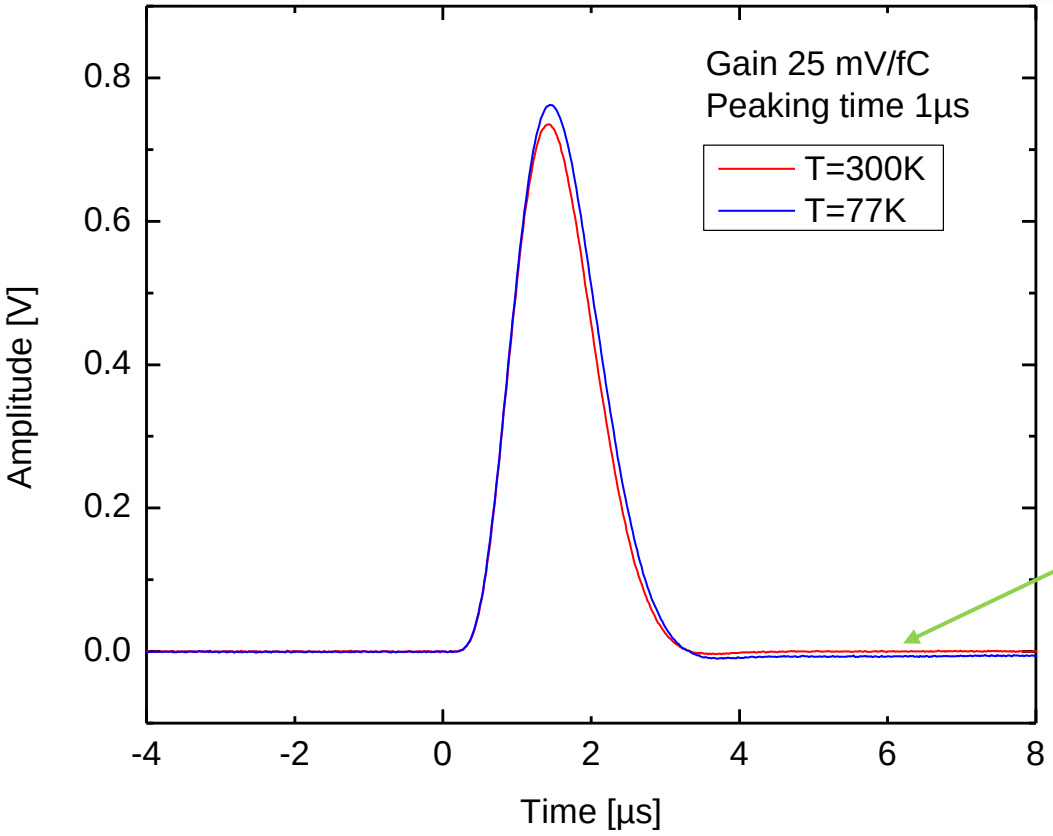
Signal Measurements



Bandgap Reference

$$V_{BGR} \approx \begin{cases} 1.185\ V \ \text{ at } \ 300\ ^{\circ}K \\ 1.164\ V \ \text{ at } \ 77\ ^{\circ}K \end{cases}$$

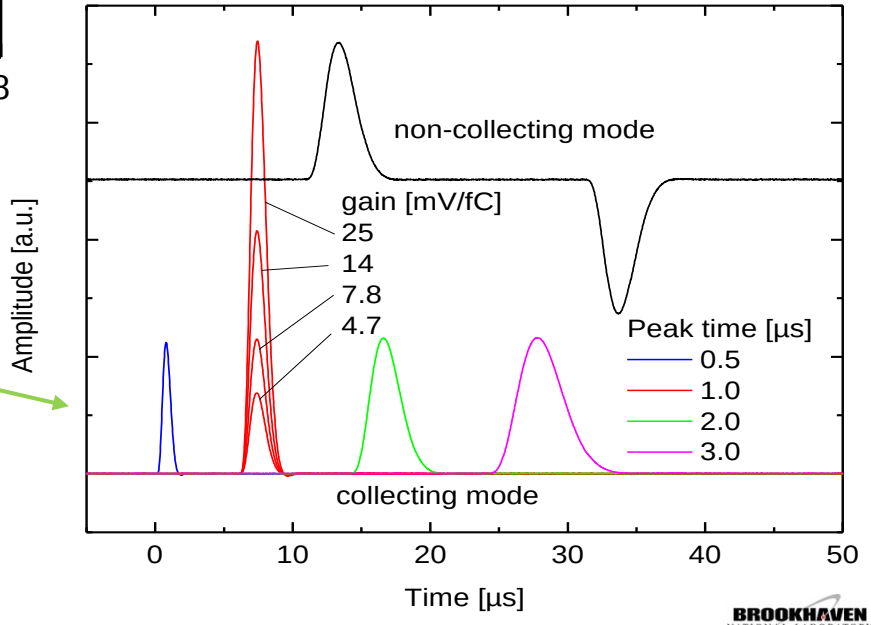
variation ≈ 1.8 %

Temperature Sensor

$$V_{TMP} \approx \begin{cases} 867.0\ mV \ \text{ at } \ 300\ ^{\circ}K \\ 259.3\ mV \ \text{ at } \ 77\ ^{\circ}K \end{cases}$$

~ 2.86 mV / K

Pole-zero cancellation at 77K to be addressed in next revision



Adjustable gain, peaking time and baseline

maximum charge 55, 100, 180, 300 fC

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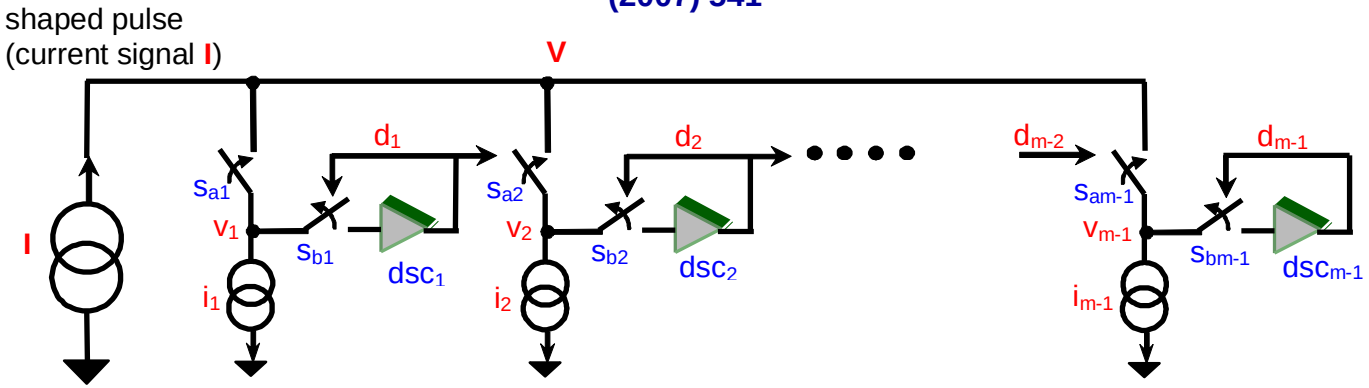
ADC - Architecture

Clockless low power ADC stage

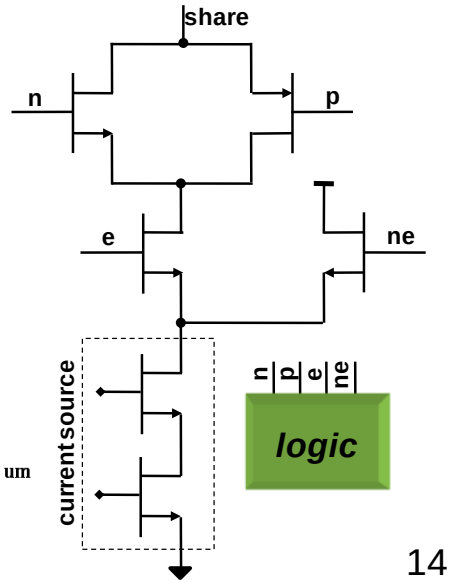
Demonstrated in ASIC for SNS, see De Geronimo, *et al*., IEEE Trans NSS, 54 (2007) 541

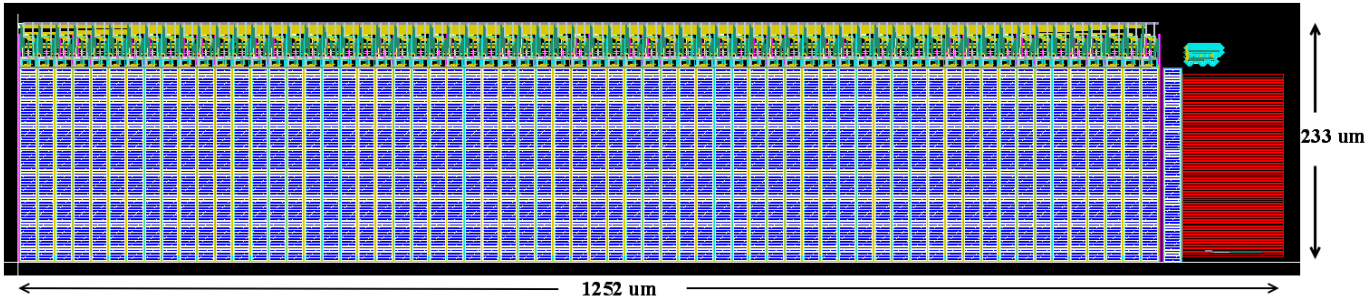


Current mode ADC

- **dual stage** 6-MSBs in 150ns, 6-LSBs in 250ns
- single trigger conversion per stage
- **12-bit resolution**
- **2 MS/s** conversion rate
- power dissipation **3.6 mW at 2 MS/s**
- **power-down** option for low rate applications
  - wake up in few tens of ns
- layout size: 0.23 mm x 1.25 mm

ADC cell





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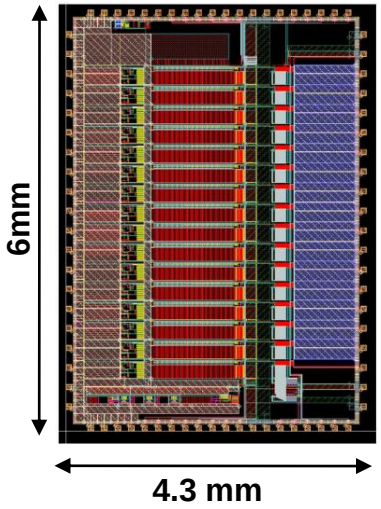
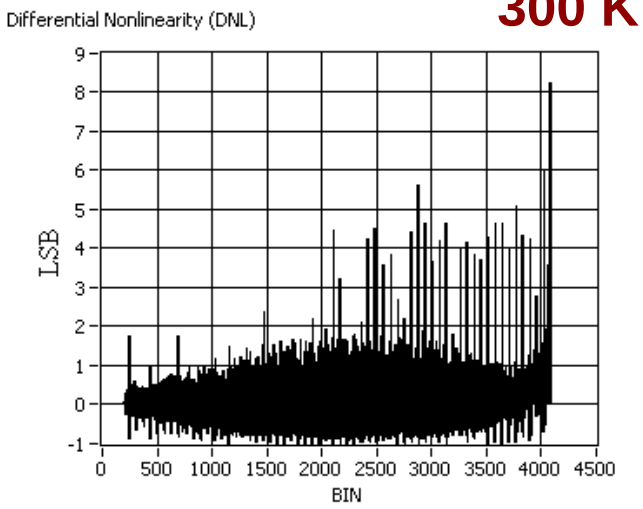
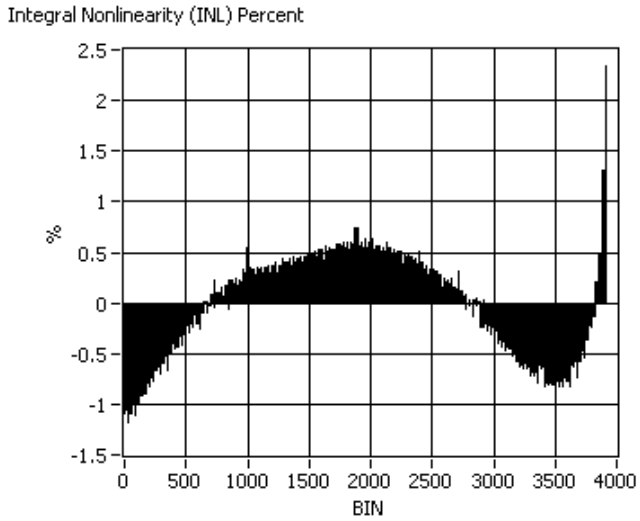
ADC - Preliminary Results

16-channel ADC+buffer



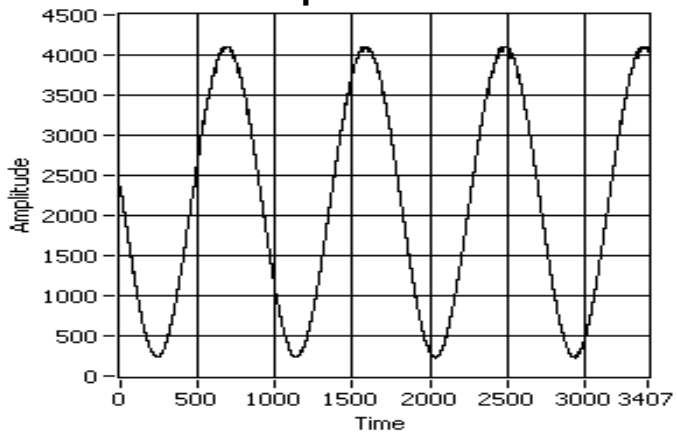
300 K



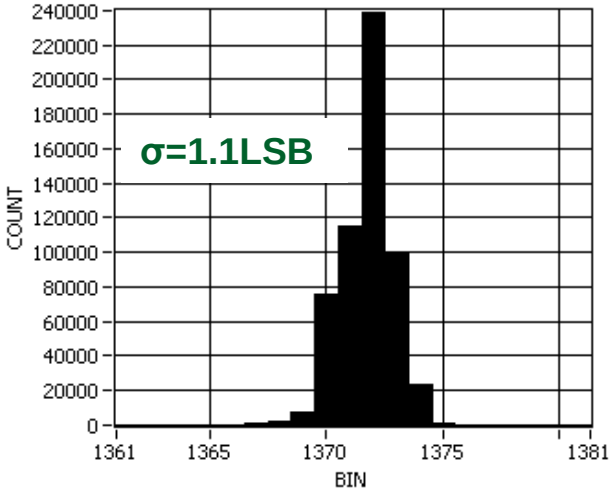


77 K

ADC output - 1.4 V sine



ADC output - 500mV dc



- operation **verified at room and cryogenic temperatures**
- **differential non-linearity** limited by **timing design error** in control circuit
- **integral non-linearity** limited by **mismatch (linear → common centroid)**

ASIC revision being designed, to be fabricated in July

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Conclusions and Future Work

- CMOS performs better at cryogenic temperatures
- Defined and predictable design for cryogenic T is possible
- Low-noise at cryogenic T demonstrated
  - ENC < 1,000 e^- at 200pF ~5mW/ch.
  - characterization and modeling of CMOS 180nm
- Long lifetime at cryogenic T possible with guidelines
- Critical building blocks - front-end & ADC - developed
- Future work
  - Improve cryogenic static models
  - Optimize ADC
  - Merge, add zero-suppression & buffering, and finalize

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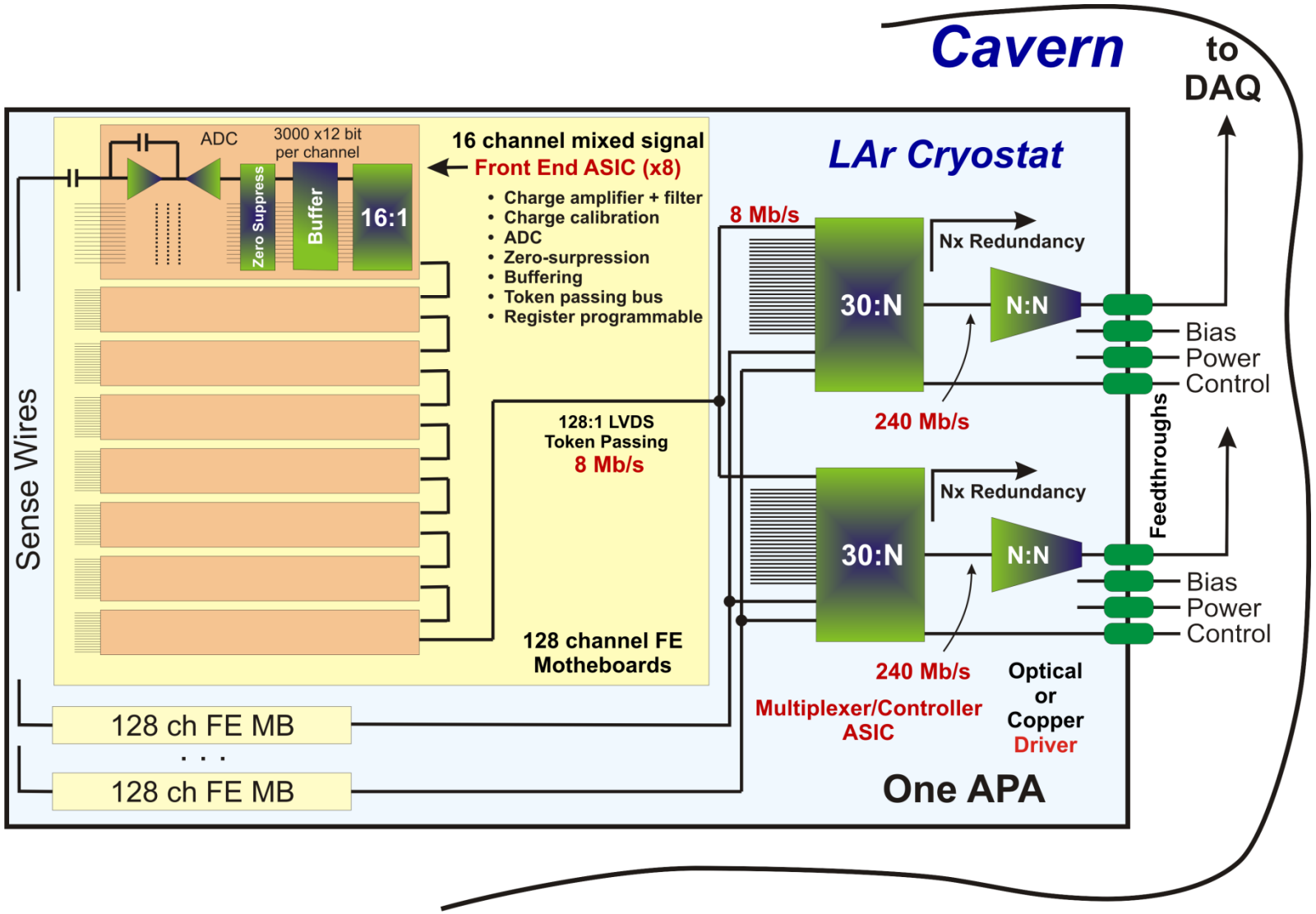
Backup Slides

LAr TPC - Cold CMOS Electronics Block Diagram – Alernate Design



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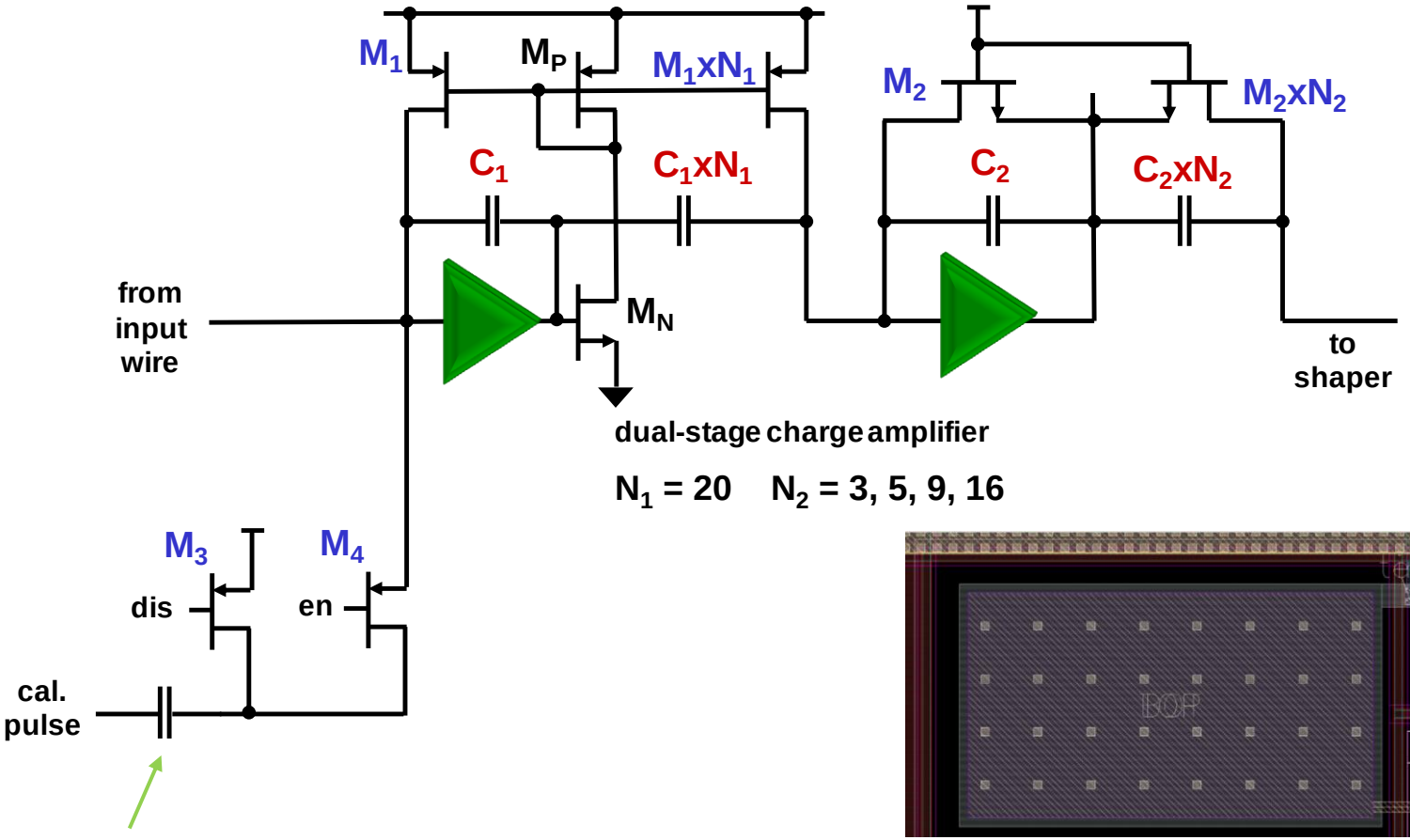
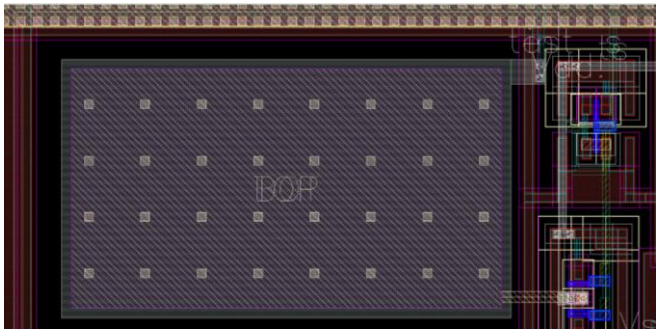
Calibration Scheme





C_{INJ} = 180 fF nominal

Integrated injection capacitance (10 x 18 μm²)

Disabled (grounded) when unused

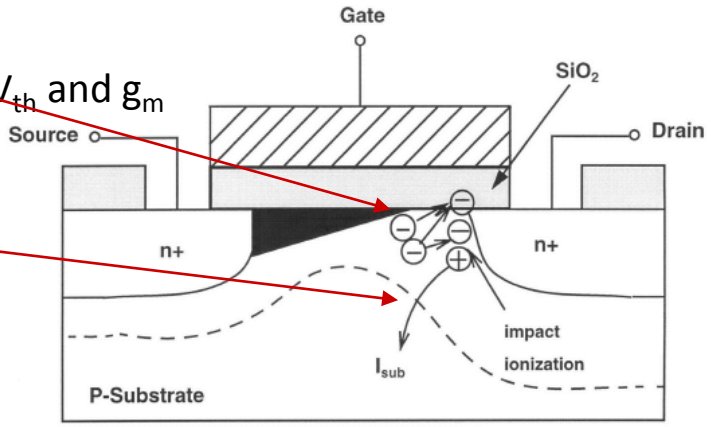
Measured with high-precision external capacitance

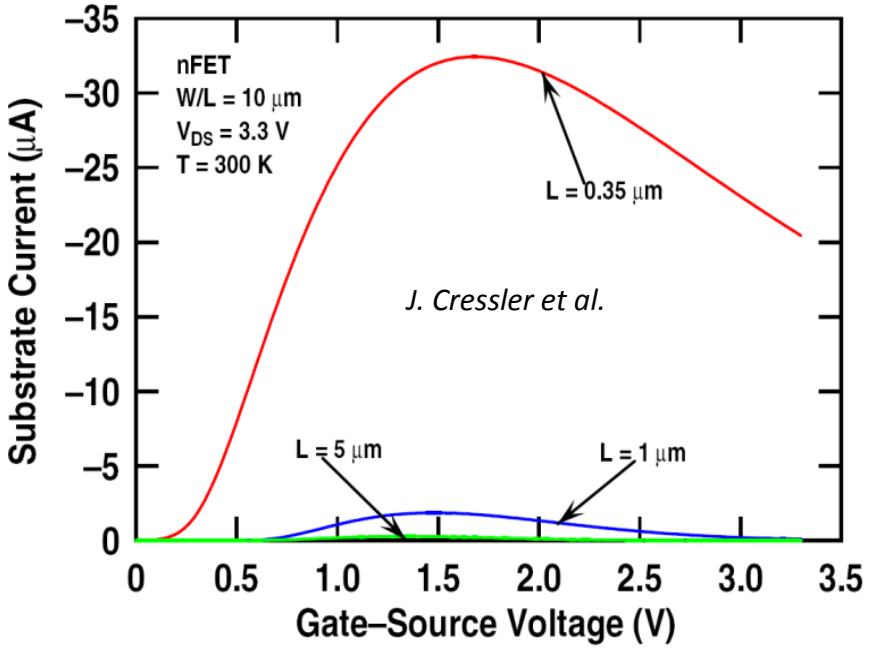
$$C_{INJ} \approx \begin{cases} 184 \text{ fF at } 300K \\ 183 \text{ fF at } 77K \end{cases}$$

change ~ 0.5%

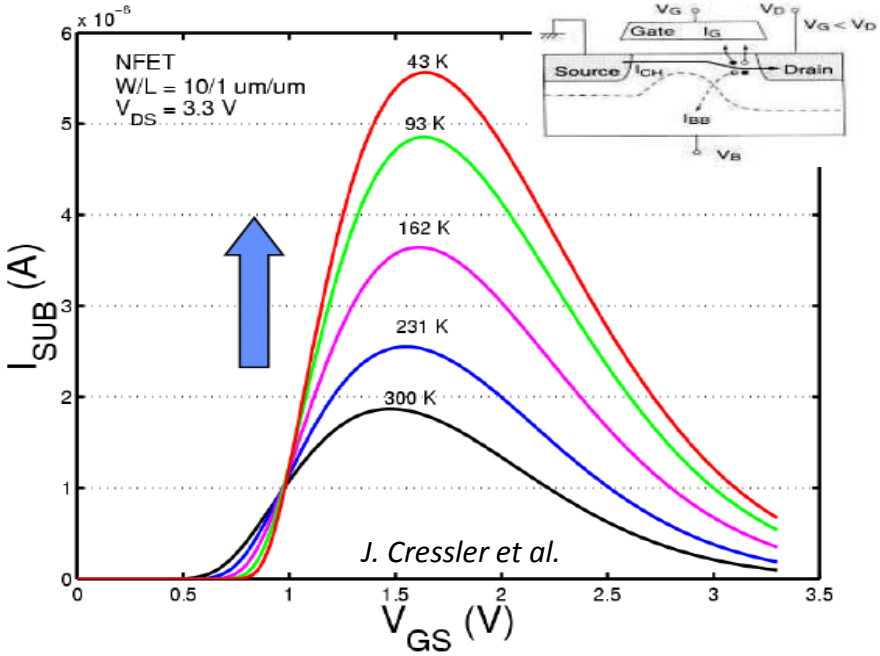
Lifetime - Basic Mechanism

- **Degradation is due to impact ionization**
  - charge trap in oxide, interface generation → shift in V_{th} and g_m
- **Substrate current is a monitor of impact ionization**
  - increases with **drain voltage**
  - is higher in **short channel** devices
  - has a **maximum** at $V_{GS} \approx V_{DS}/2$





- **increases as the temperature decreases**



Commercial technologies are rated 10 years lifetime (10% g_m shift) in continuous ring oscillator operation: T = 300 K, L = L_{min}, V_{ds} = nominal V_{DD}+5%, $V_{GS} \approx V_{DS}/2$)

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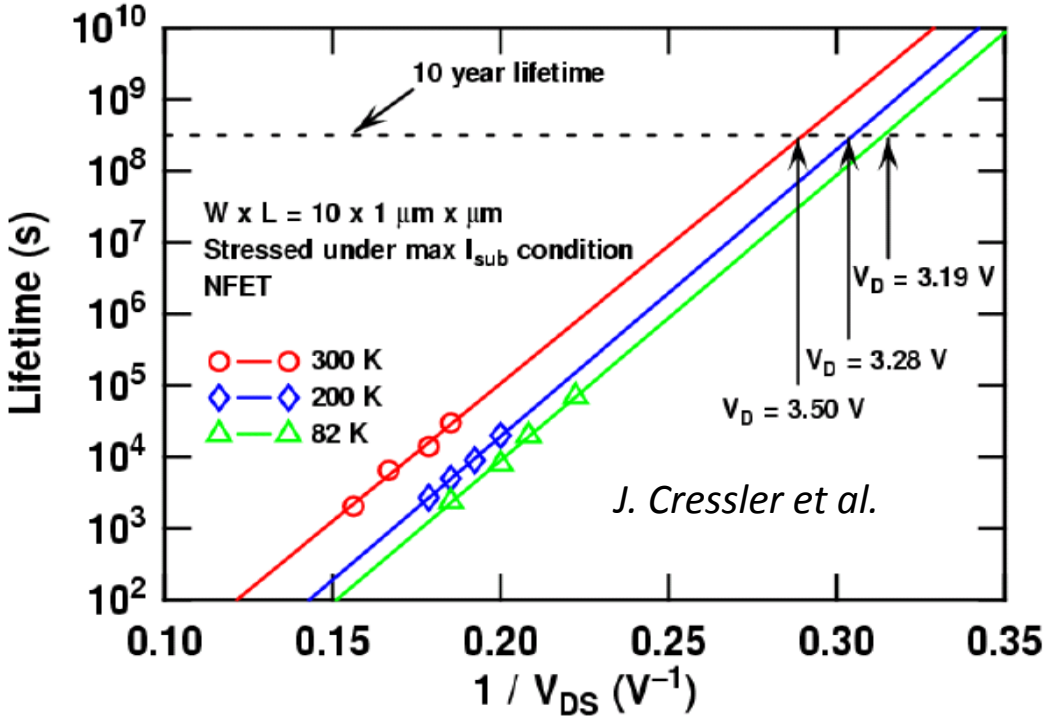
Lifetime - Design Guidelines

Accelerated tests at increased V_{DS} allow extrapolation of lifetime



Desired lifetime at low temperature can be achieved by:

1. **decreasing V_{DS}** (e.g. decreasing the supply voltage)
2. **decreasing J_D** (i.e. decreasing the drain current density)
3. **increasing L** (i.e. non-minimum channel length devices)

Design guidelines can be obtained for:

analog circuits

- operate devices at **low current density**
- use **non-minimum channel length L**

digital circuits

- operate devices at **-10% of nom. V_{DD}**
- use **non-minimum channel length L**
- operate at **low clock frequency**

Accelerated tests at cryogenic temperature are being performed to verify guidelines

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