

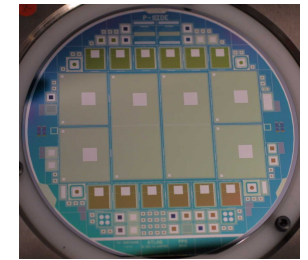
# Recent progress of the ATLAS Upgrade Planar Pixel Sensor R&D Project



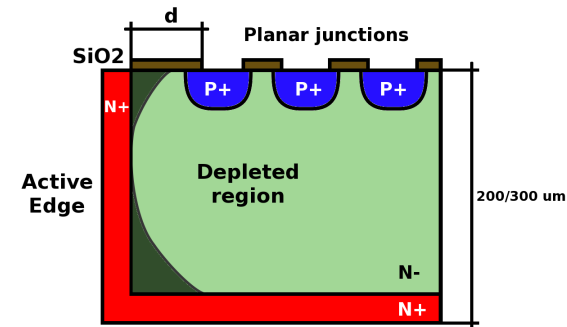
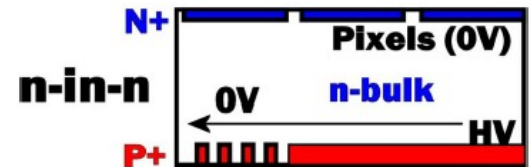
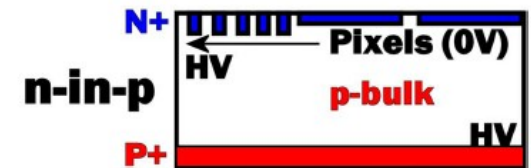
Marco Bomben  
LPNHE – Paris



on behalf of the ATLAS PPS collaboration

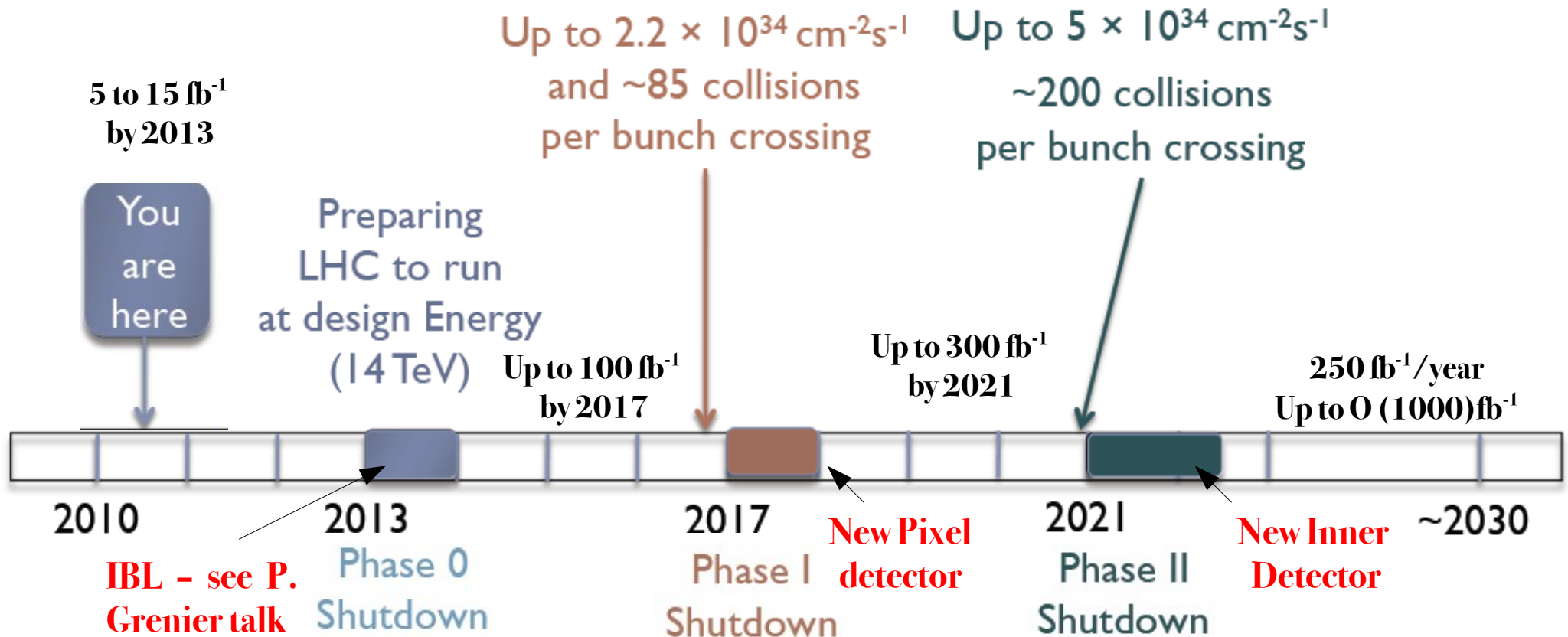
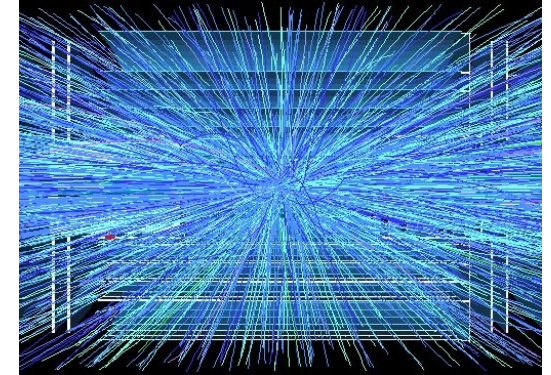


- The LHC future plans
- A new Atlas Pixel Detector
- The Atlas Upgrade **Planar Pixel Sensor** R&D Project
- N-in-p: overview
- N-in-n: irradiation & test beams results
- Thin n-bulk production
- Simulation studies
- Slim / Active edge
- Conclusions & outlook

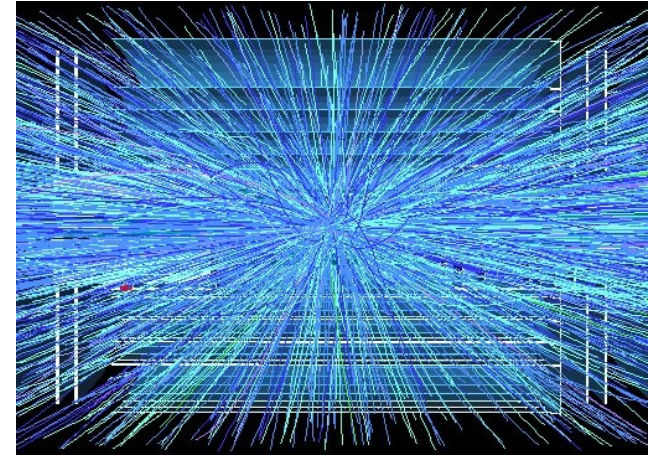


# The LHC future plans

- The **discovery** potential of the **LHC** can be **enhanced** by increasing its **luminosity**
- HL-LHC plans**
  - Caveat: this schedule spans decades



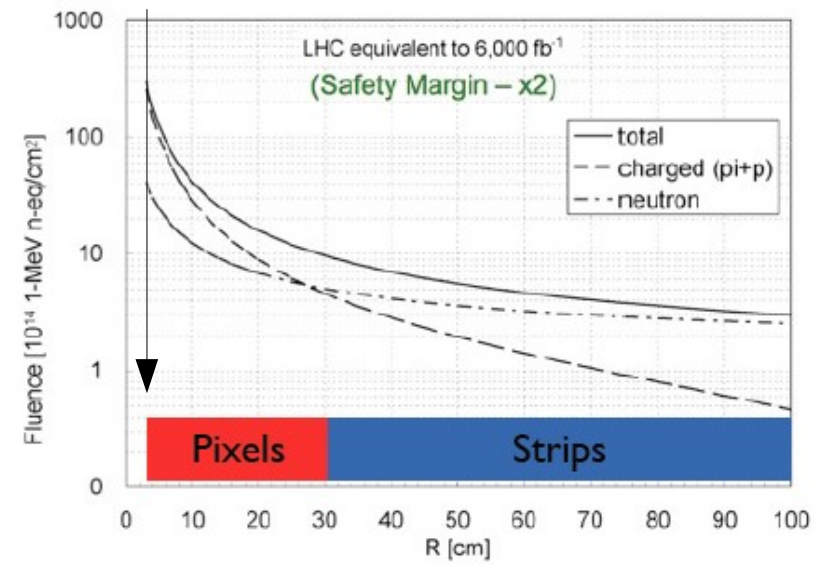
- Higher luminosity means
- ✓ More pile-up & higher rate events
- Higher granularity

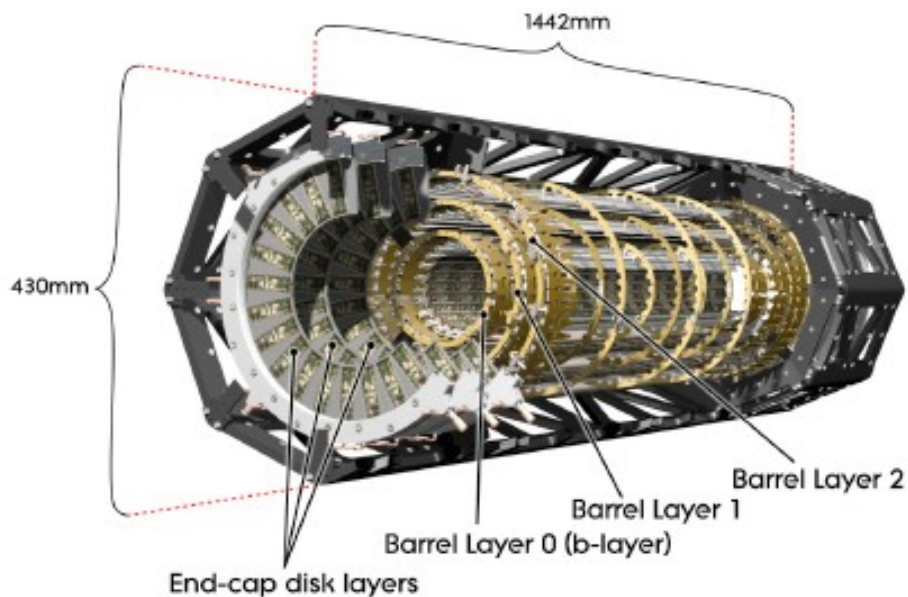


- ✓ Large fluences
  - × Dark current increase
  - × Change of working voltage
  - × Reduced charge collection eff.

fluences for the innermost pixel layer:  
 **$1-2 \times 10^{16} \text{ n}_{\text{eq}} / \text{cm}^2 (3 \text{ ab}^{-1})$**

→ Radiation hard components



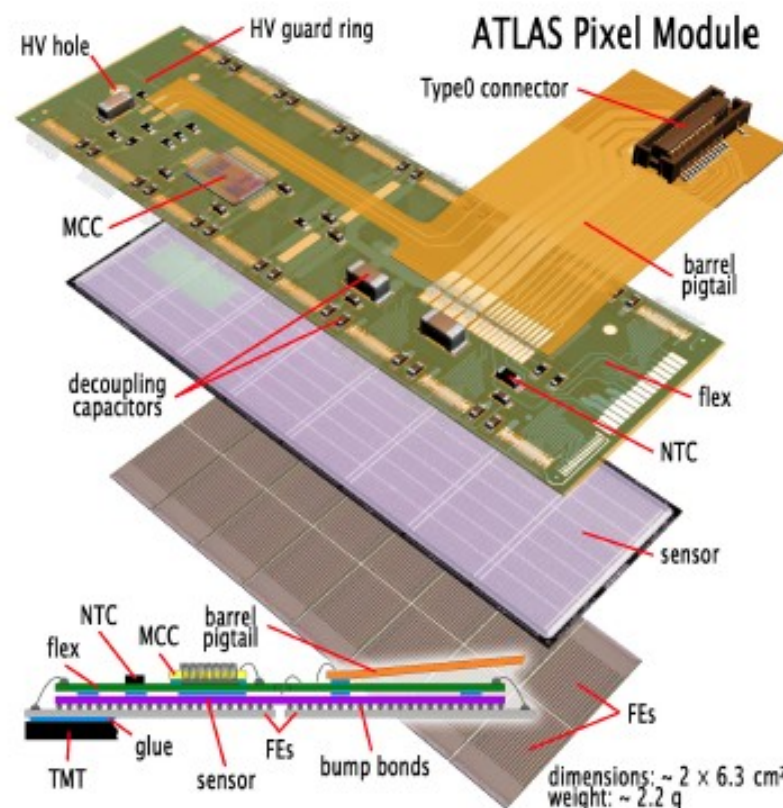


- **ATLAS Pixel Module**

- 16 front-end chips (FE-I3) module with a Module Controller Chip (MCC)
- 46080 R/O channels  $50\ \mu\text{m} \times 400\ \mu\text{m}$  ( $50\ \mu\text{m} \times 600\ \mu\text{m}$  for edge pixel columns between neighbour FE-I3 chips)
- Planar n-in-n DOFZ silicon sensors, 250 $\mu\text{m}$  tick
- Designed for  $1 \times 10^{15}$  1MeV fluence and 50 Mrad
- Optolink R/O: 40÷80 Mb/link

- **ATLAS Pixel Detector**

- 3 barrels + 3 forward/backward disks
- 112 stave and 4 sectors
- 1744 modules
- 80 million channels



# The PPS R&D project

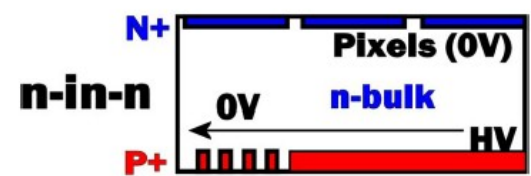
- Aim: Explore the suitability of **planar** pixel sensors for **highest fluences** Timeline: new Pixel (2017) + new ID (2021)

- Approved ATLAS R&D project since 2009: 17 institutes, > 80 scientists

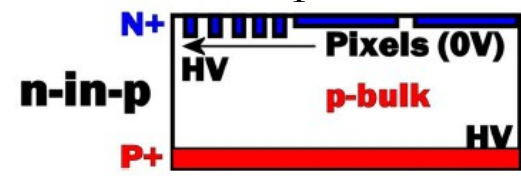


- **Planar pixel is a proven technology**

- the current n-in-n pixel detector.
- present modules already shown to work after  $10^{15} \frac{n_{eq}}{cm^2}$
- If strips not adequate any more, PPS would be the natural option

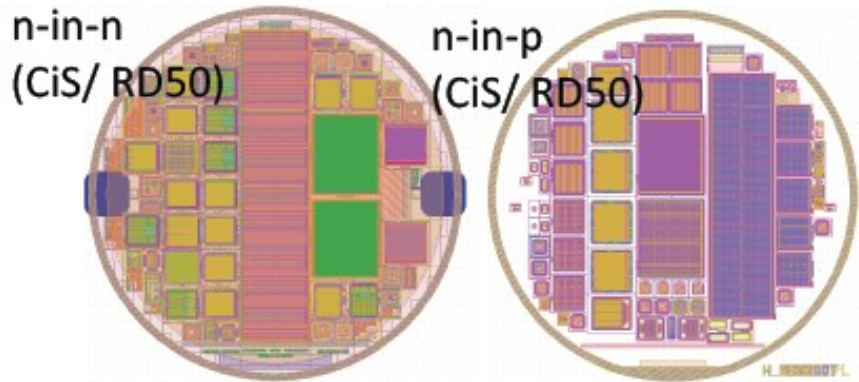


N-in-p: A. Macchiolo talk (09 June - 3pm)



- Research directions

- **Radiation damage studies**
- Active area optimization and geometry redesign
- **Advanced simulation studies**



## Participating Institutes

### **CERN**

D. Dobos, B. Di Girolamo, D. Muenstermann, H. Pernegger, S. Roe, A. La Rosa

### **AS CR, Prague (Czech Rep.)**

V. Vrba, P. Sicho, J. Popule, M. Tomasek, L. Tomasek, J. Stastny, M. Marcisovsky, M. Havranek, J. Bohm, Z. Janoska, M. Hejtmanek

### **LAL Orsay (France)**

M. Benoit, N. Dinu, D. Fournier, J. Idarraga, A. Lounis

### **LPNHE / Paris VI (France)**

M. Bomben, G. Calderini, Eve Chareyre, J. Chauveau, C. La Licata, G. Marchiori, P. Schwemling

### **University of Bonn (Germany)**

M. Barbero, F. Hüging, H. Krüger, N. Wermes

### **HU Berlin (Germany)**

H. Lacker

### **DESY (Germany)**

C. Hengler, I. M. Gregor, U. Husemann, V. Libov, I. Rubinsky

### **TU Dortmund (Germany)**

S. Altenheiner, C. Gößling, J. Jentsch, T. Lapsien, R. Klingenberg, A. Rummeler, G. Troska, T. Wittig, R. Wunstorf

### **University of Goettingen (Germany)**

J. Grosse-Knetter, M. George, A. Quadt, J. Weingarten

### **MPP und HLL Munich (Germany)**

L. Andricek, M. Beimforde, A. Macchiolo, H.-G. Moser, R. Nisius, R. Richter, P. Weigell

### **Università degli Studi di Udine – INFN (Italy)**

D. Cauz, M. Coba, C. del Papa, D. Esseni, M. P. Giordani, P. Palestri, G. Pauletta, L. Selmi

### **KEK (Japan)**

Y. Unno, S. Terada, Y. Ikegami, Y. Takubo

### **IFAE-CNM, Barcelona (Spain)**

M. Cavalli, S. Grinstein, Korolkov, M. Lozano, C. Padilla, G. Pellegrini, S. Tsiskaridze

### **University of Liverpool (UK)**

T. Affolder, P. Allport, G. Casse, T. Greenshaw, I. Tsurin

### **UC Berkeley/LBNL (USA)**

M. Battaglia, T. Kim, S. Zalusky

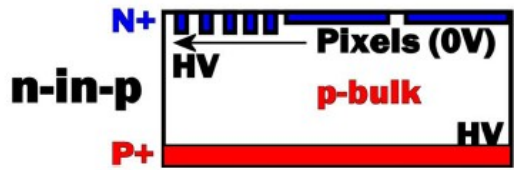
### **UNM, Albuquerque (USA)**

I. Gorelov, M. Hoferkamp, S. Seidel, K. Toms

### **UCSC, Santa Cruz (USA)**

V. Fadeyev, A. Grillo, J. Nielsen, H. Sadrozinski, B. Schumm, A. Seiden

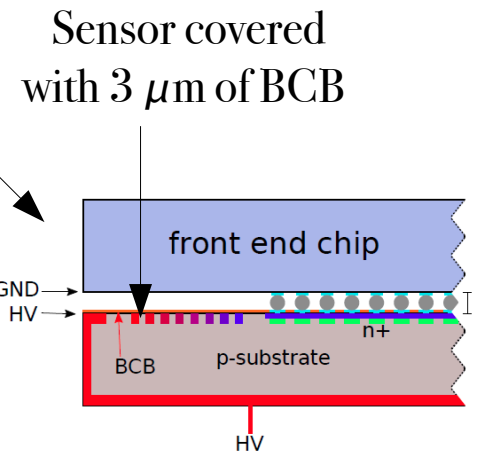
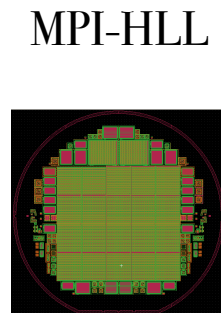
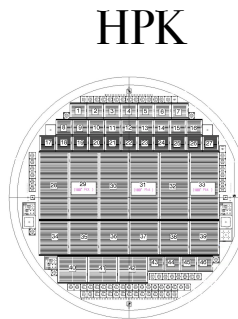
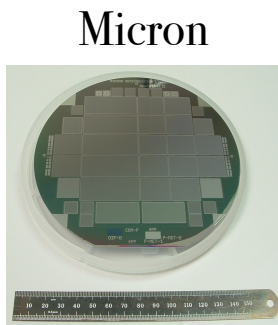
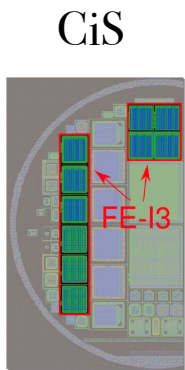
# PPS n-in-p overview



- ✓ Larger **areas** → larger **cost**: **single-side** patterned sensor can **help!** (e.g. An **ID** with **pixels** only → **10 m<sup>2</sup>**)
- ✓ **p**-type bulk does **not invert** → stable operation
- × Sensor **edge** at **HV**, facing **electronics** at **GND** → pixels can suffer from **sparks**

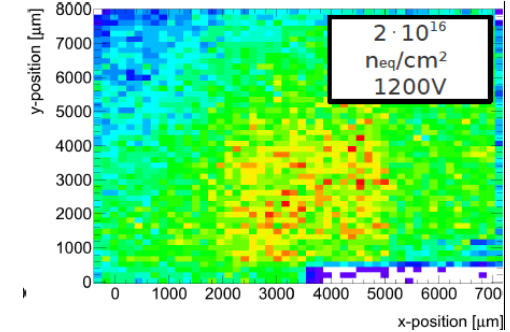
→ First countermeasures looks promising

## Contributors

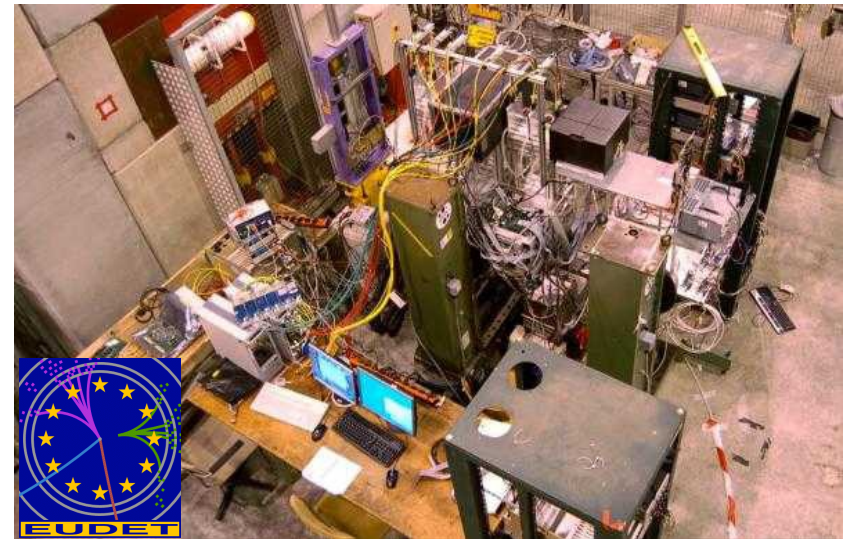


	Thickness (μm)	Material	PX Isolation	Tests
CiS (n-in-n too)	285/200/150 (more details later)	FZ	hom./mod. p-spray	See A. Macchiolo talk
Micron (n-in-n too)	300/150 (same)	FZ	p-spray	Irrad., CC, testbeams
HPK	320/150	FZ	p-stop/spray	Irrad., testbeams
MPI-HLL	150/75	FZ	p-stop/spray	Irrad.



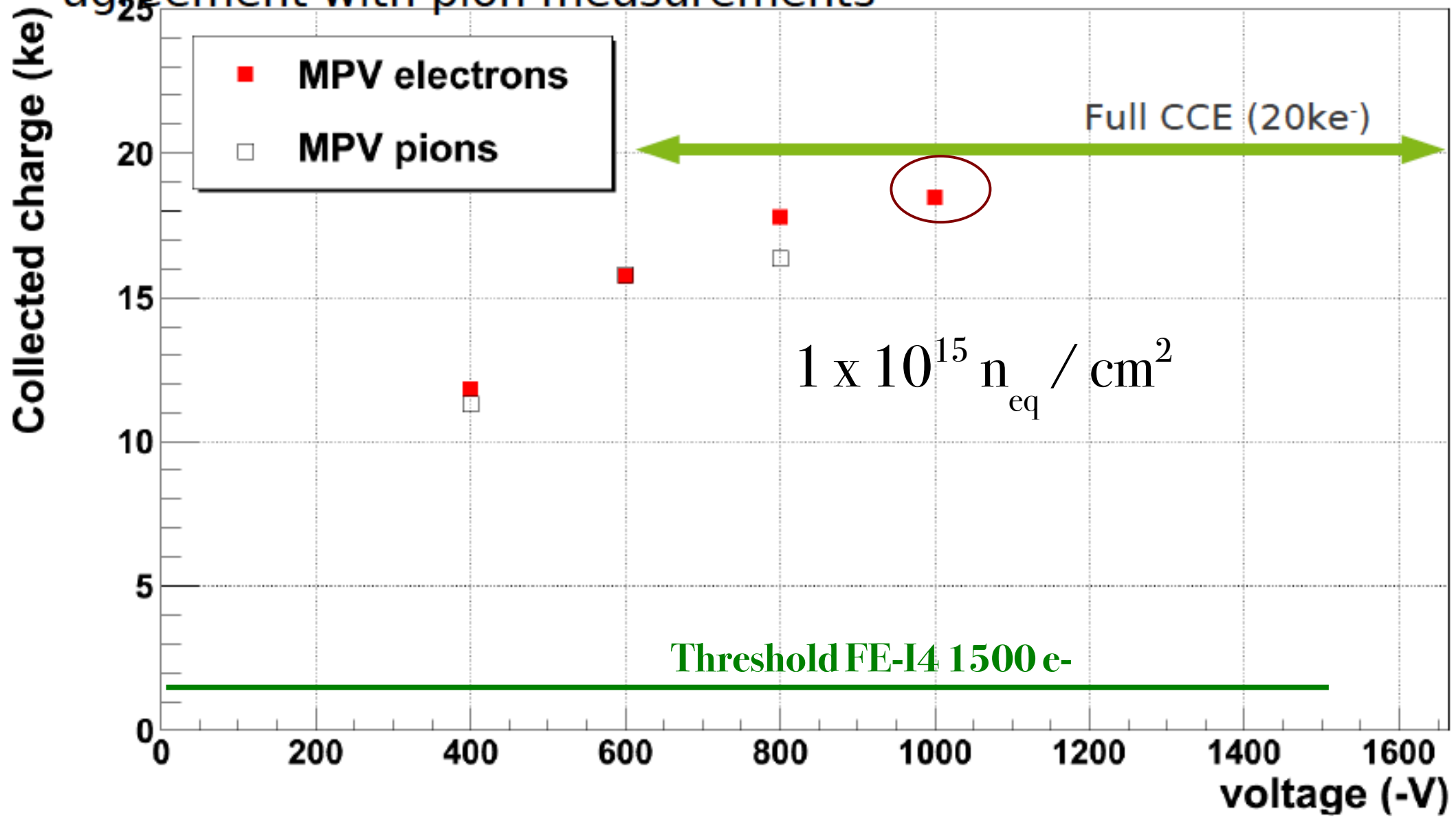


- Current Atlas Pixel modules used
- Fluences up to  $2 \times 10^{16} n_{eq} / cm^2$ 
  - Irradiations conducted with **neutrons** at the JSI TRIGA reactor in Ljublijana
- Very **cold** operation (operation **-25/-30 C** - test down to **-50 C**)
- Modules are tested with sources and on beam to measure:
  - **Collected charge**
  - **Efficiency**
  - ...



# Charge collection

- satisfactory results: 16 ke<sup>-</sup> at 600V, almost full CCE at 1kV
- agreement with pion measurements

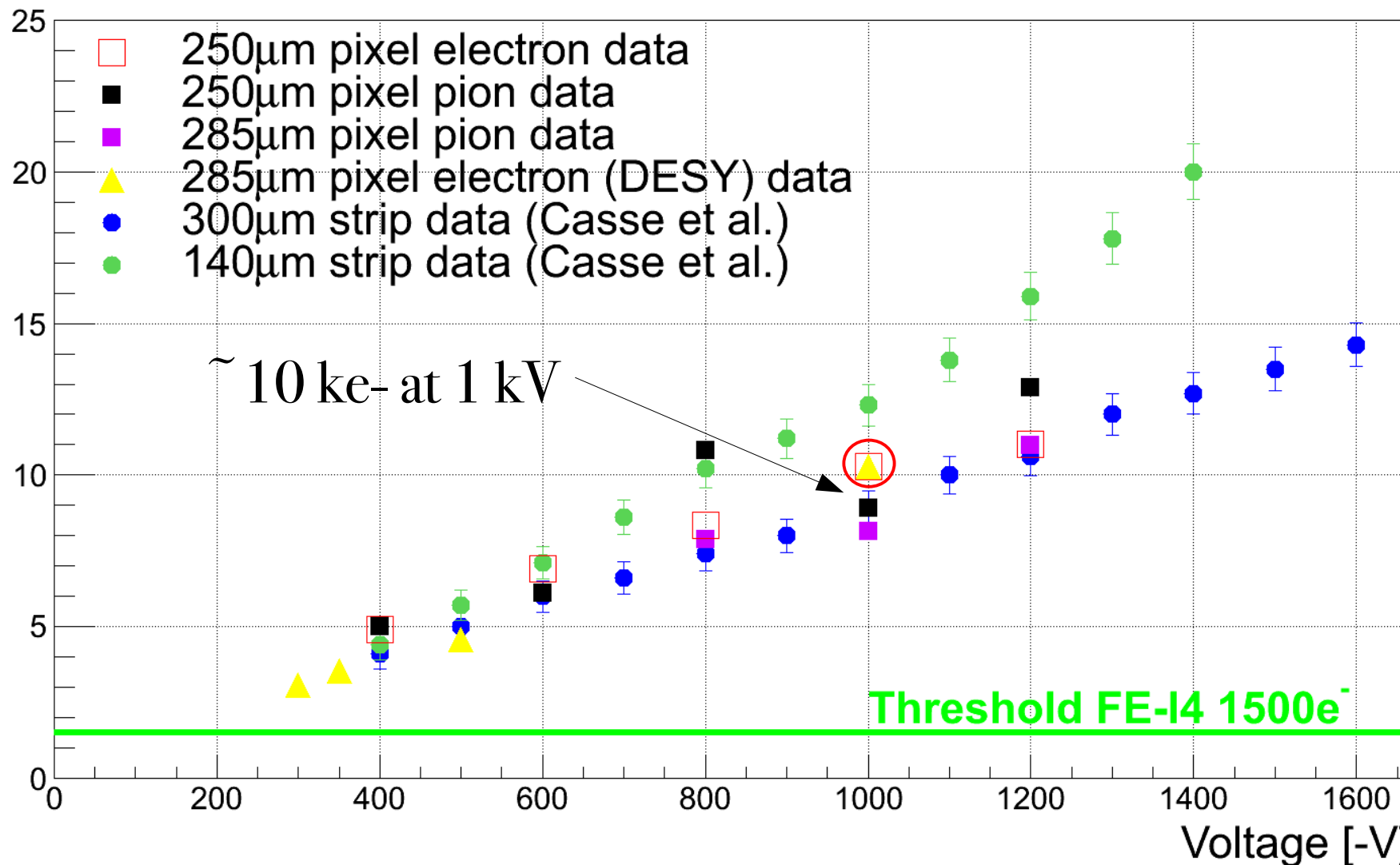


# Charge collection

$$5 \times 10^{15} n_{eq} / \text{cm}^2$$

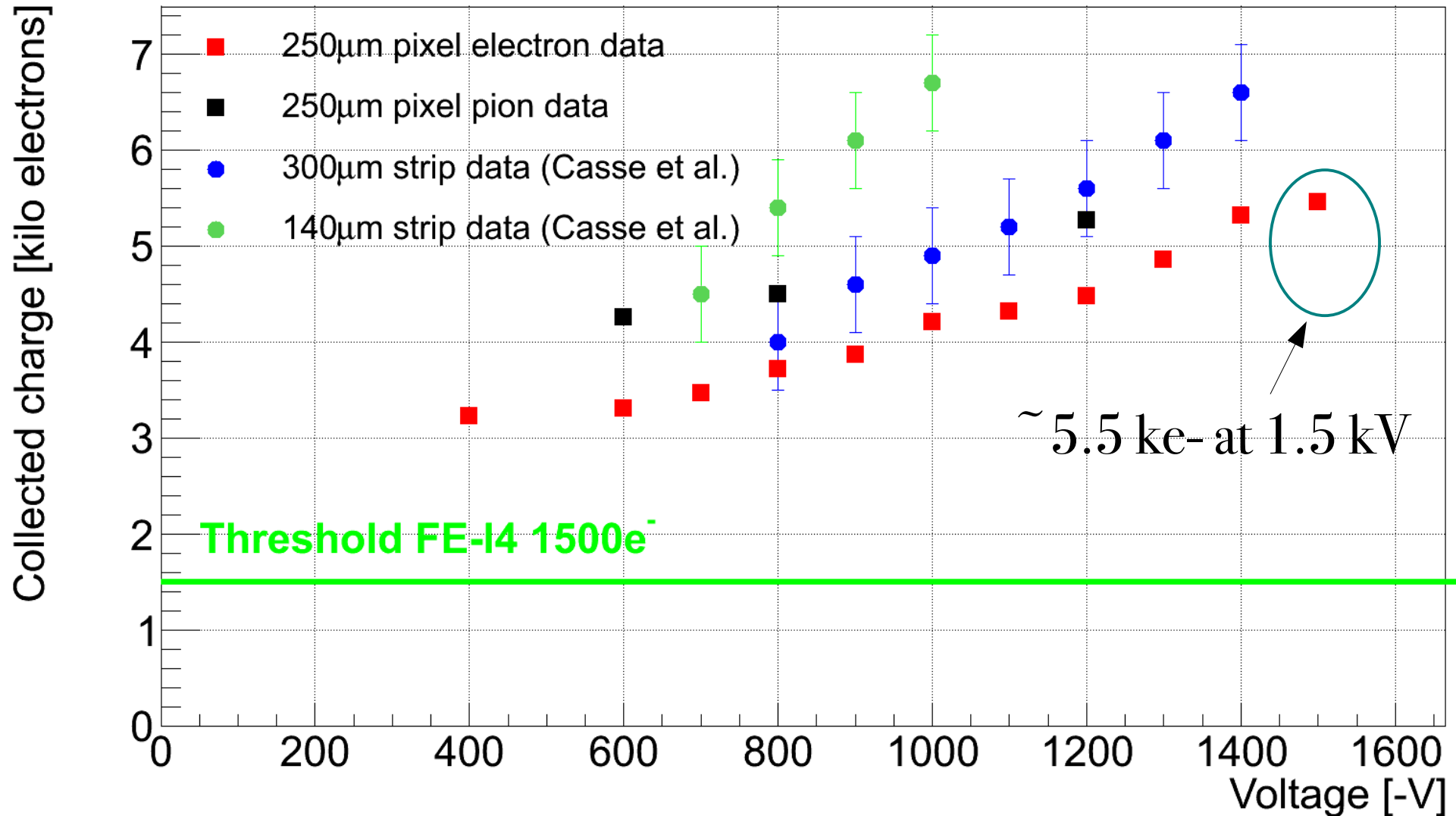
- data quite consistent
- MPV

Collected charge [kilo electrons]



# Charge collection

$2 \times 10^{16} \text{ n}_{\text{eq}} / \text{cm}^2$  - SLHC innermost Layer expected fluence

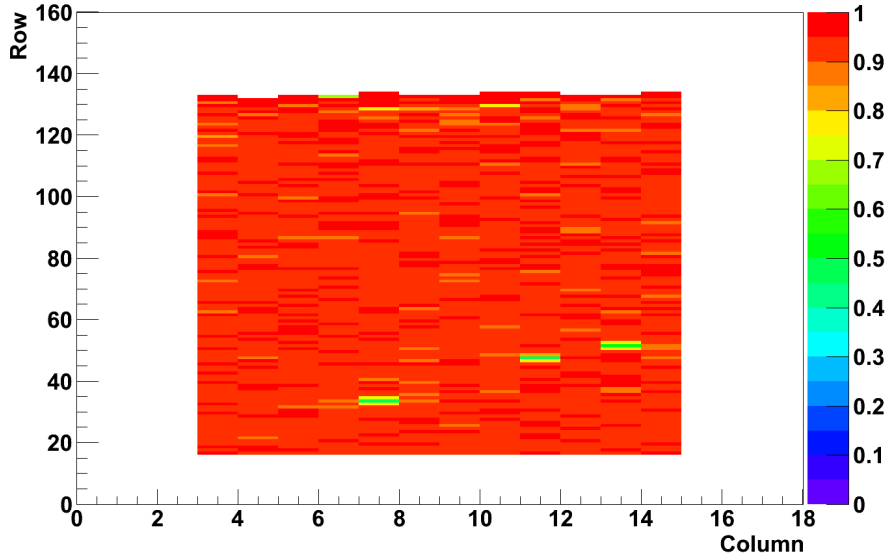


# Hit efficiency

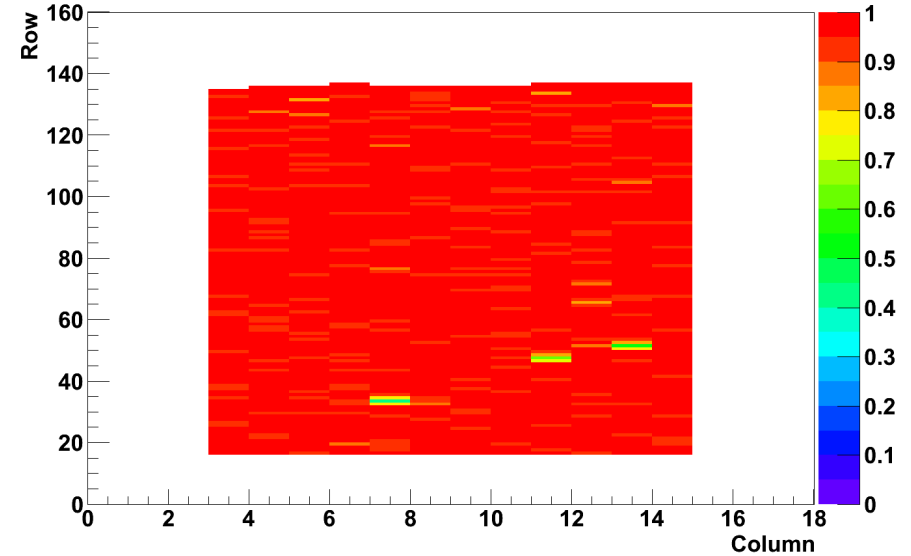
$5 \times 10^{15} \text{ n}_{\text{eq}} / \text{cm}^2 @ 350 \text{ V}$   
 $\rightarrow 93.2 \%$

$5 \times 10^{15} \text{ n}_{\text{eq}} / \text{cm}^2 @ 500 \text{ V}$   
 $\rightarrow 97.3 \%$

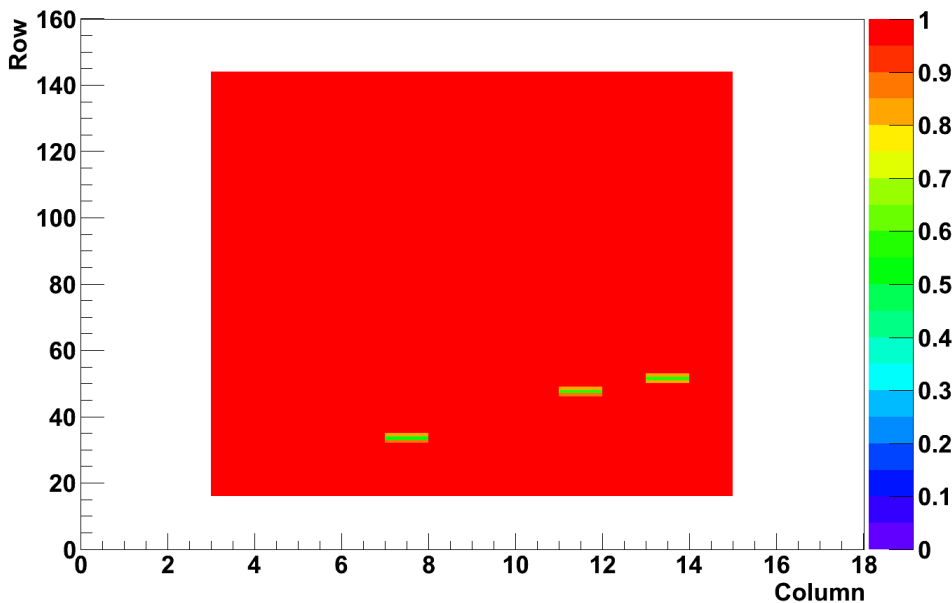
Efficiency Map



Efficiency Map

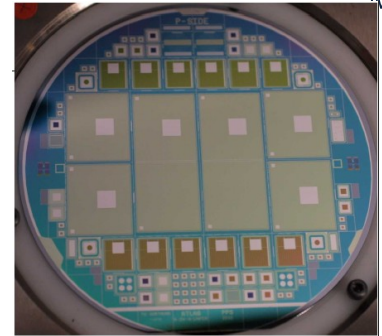


Efficiency Map

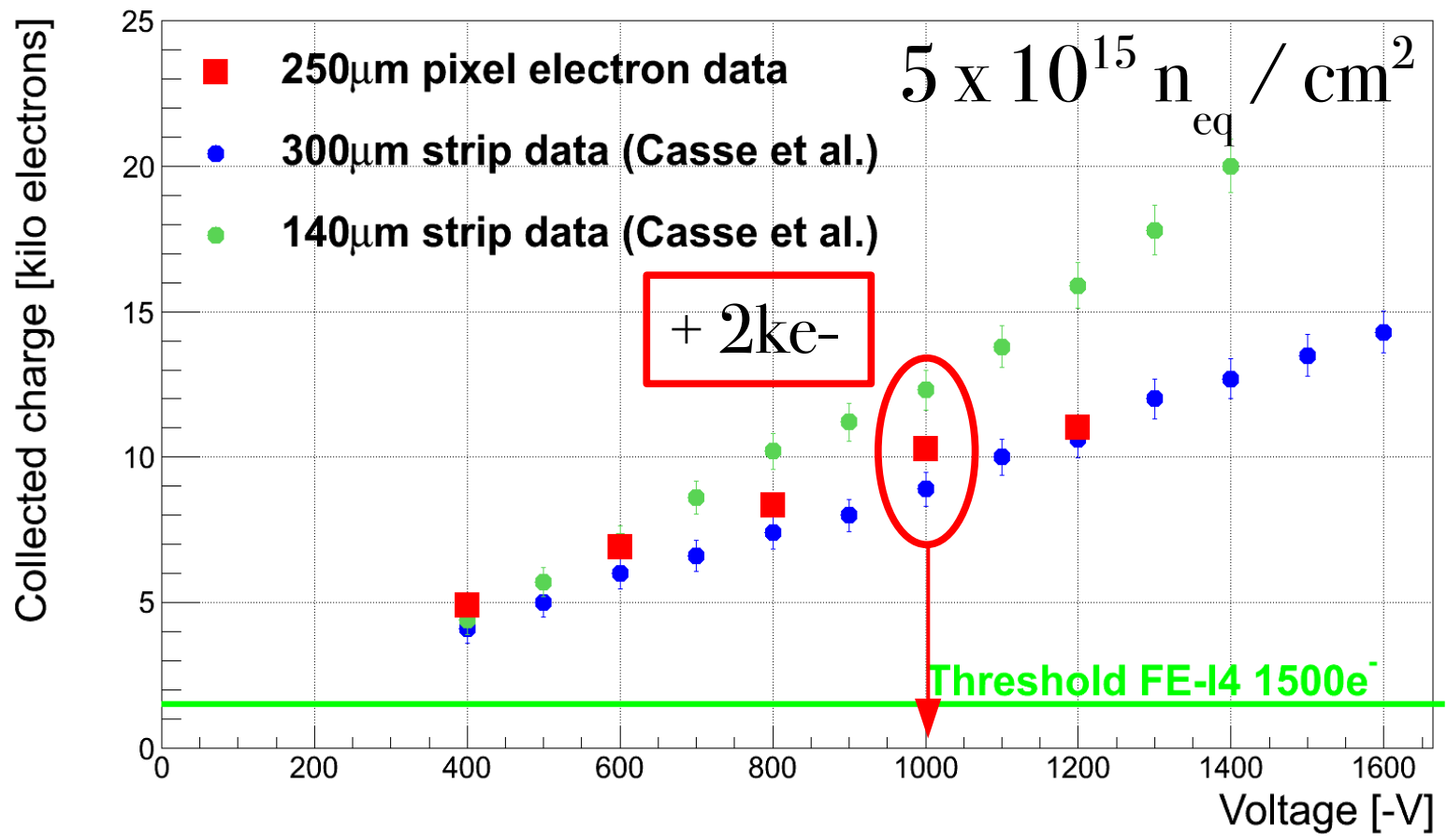


$5 \times 10^{15} \text{ n}_{\text{eq}} / \text{cm}^2 @ 1000 \text{ V}$   
 $\rightarrow 99.6 \%$  efficient

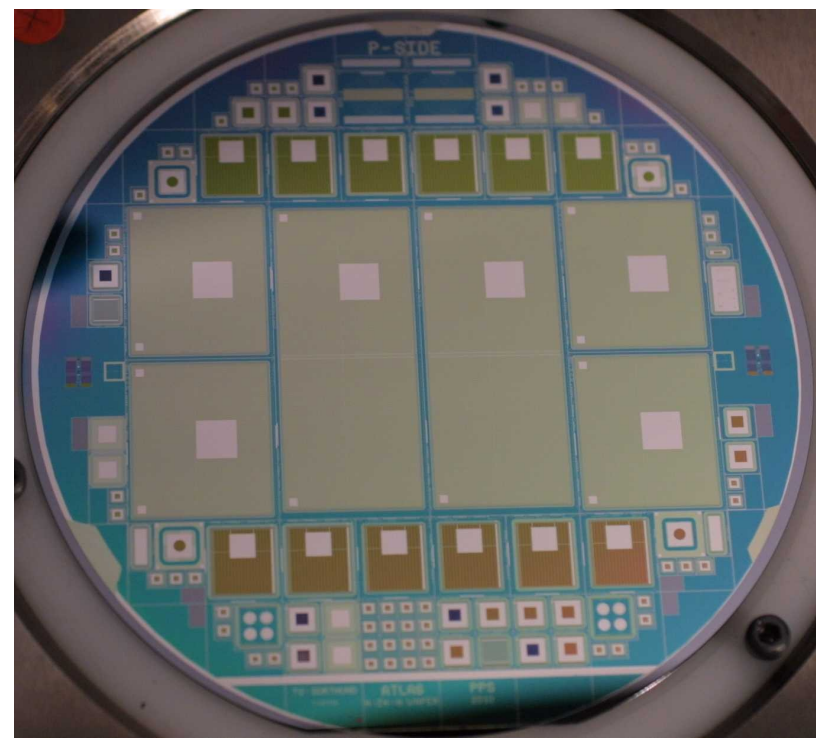
# Thin sensors



- **Thinner sensors**
  - With the same voltage → higher E field → **More charge amplification**  
→ **Velocity saturation**
  - Smaller radiation length
- n-CiS production: down to  $150\ \mu\text{m}$ , no support wafer



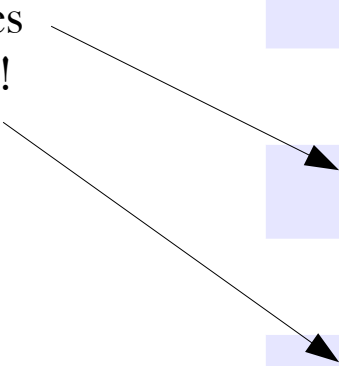
# Thin production



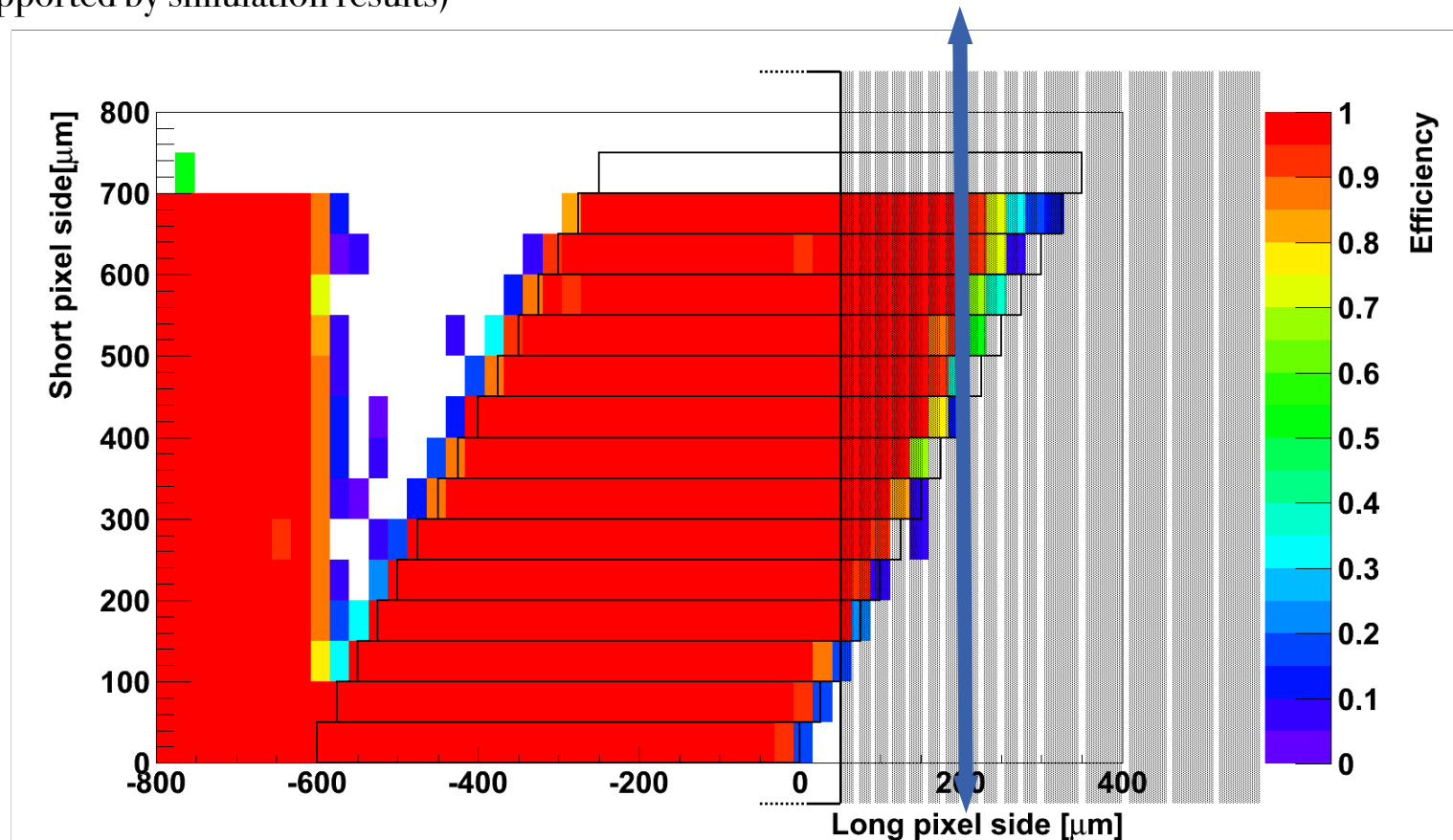
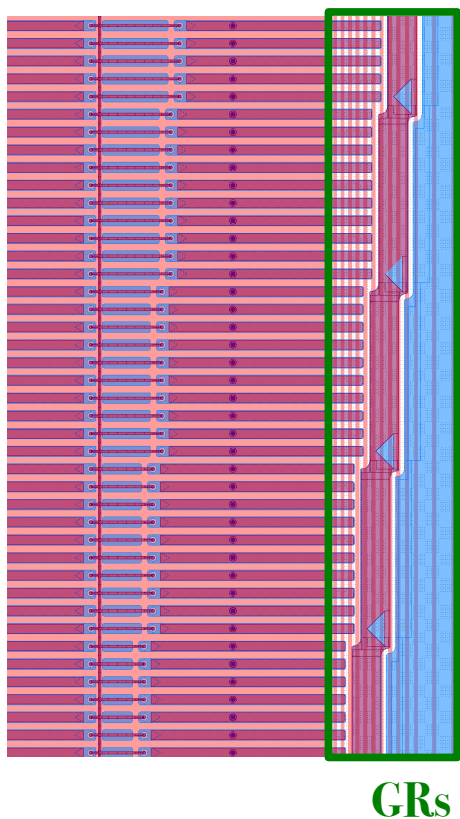
- 5 different thickness
- Detailed studies of
  - Charge collection
  - Charge amplification

thickness	wafers ordered	wafers received
250um	12	18
225um	6	11
200um	6	10
175um	6	11
150um	6	8

Irradiation studies  
already started!!!



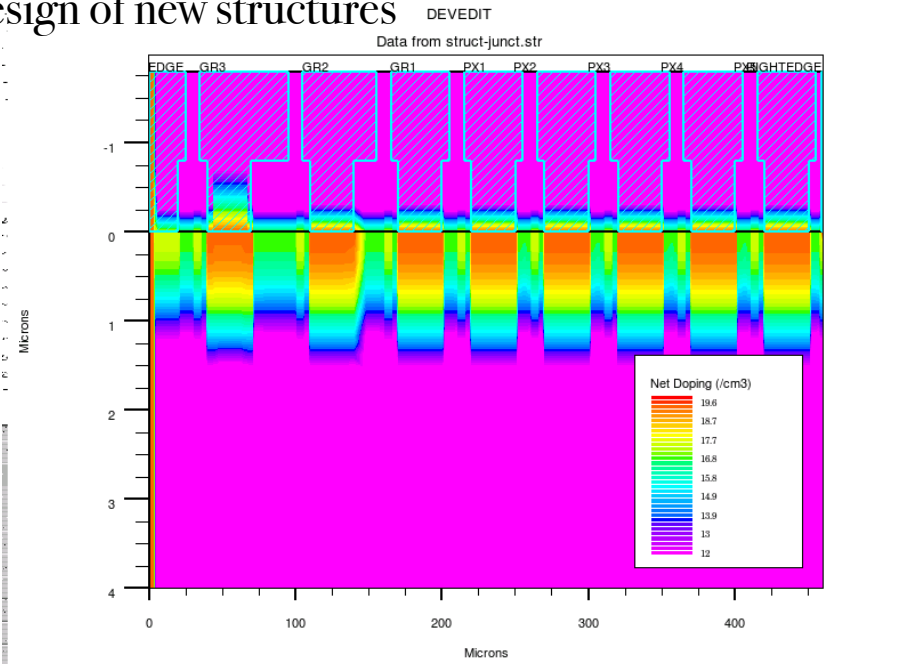
- **Inactive area** should be kept at minimum
  - *e.g.* Inner layers: no shingling in z
- dedicated test structure ('pixel shifted stepwise') confirms that charge is collected opposite of the guard rings
- estimated region of high (>99%) efficiency before irradiation: up to  $\sim 200 \mu\text{m}$  from the HV implant (i.e.  $\sim 250 \mu\text{m}$  inefficient edge)
- looks promising (strongly supported by simulation results)



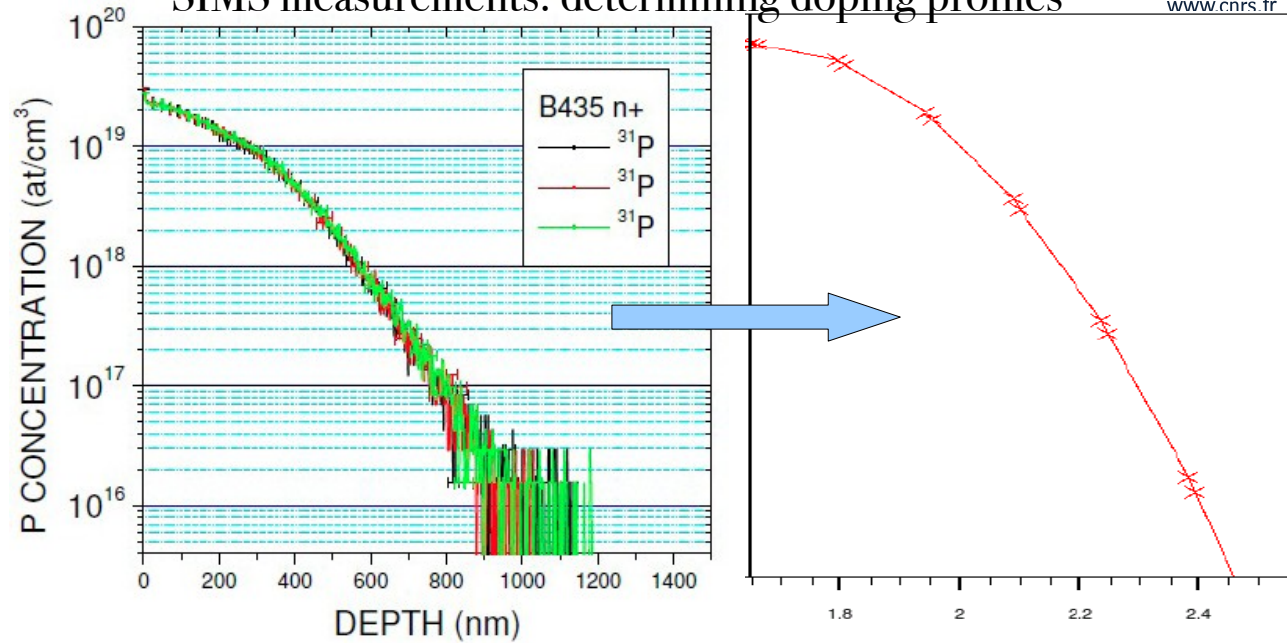


- TCAD simulations allows to test in advance several possible sensor designs
- It helps in keeping costs down
- Precise input is needed!!!
- Whole set of “experimental” conditions available
  - Temperature
  - Light
  - Irradiation
  - ...

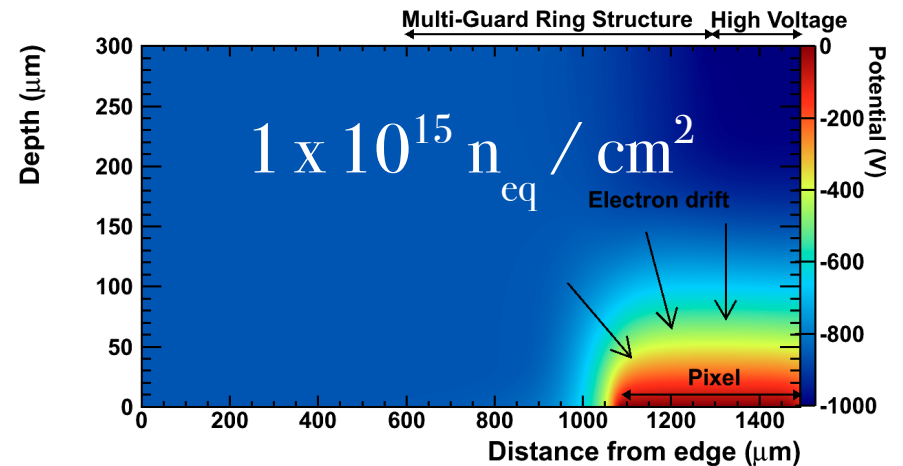
## Design of new structures



## SIMS measurements: determining doping profiles



## Potential after irradiation for a slim edge structure



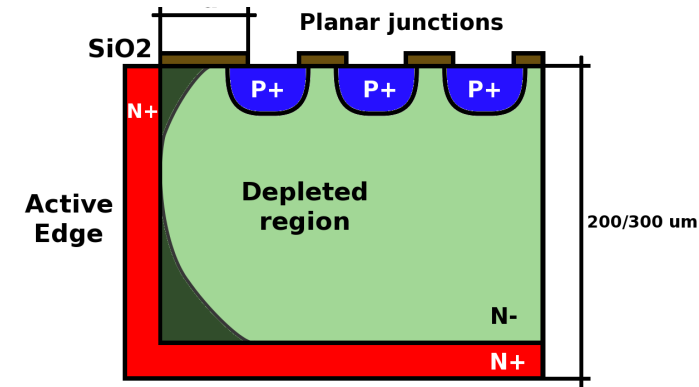
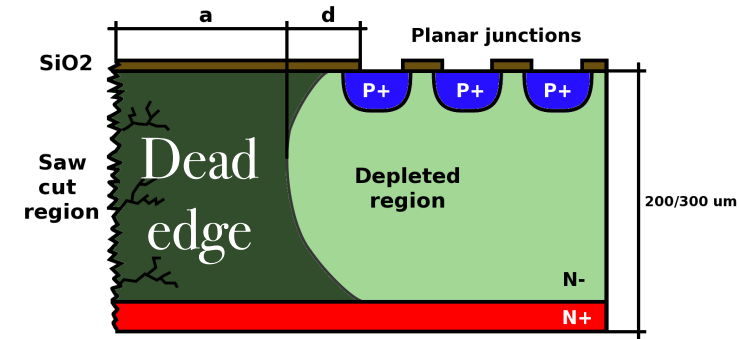
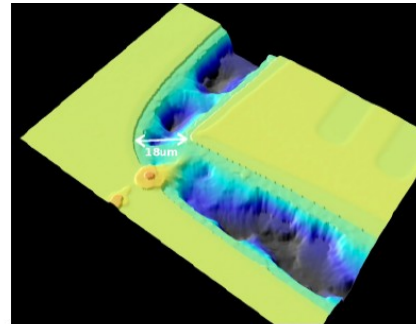
# Active edge

- Another approach to reduce dead area

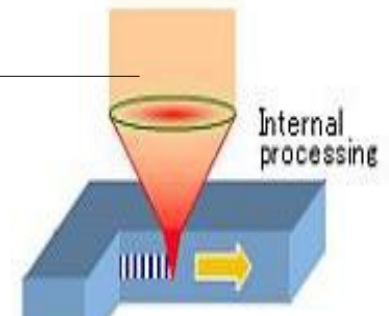
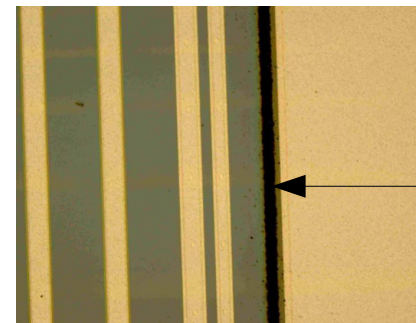
- Several ways to do that

- **Drie-etching approaches**

- ✓ CNM/IFAE
- ✓ FBK/LPNHE
- ✓ VTT/Munich



Stealth Dicing



- **Scribe + cleave + edge – passivation**

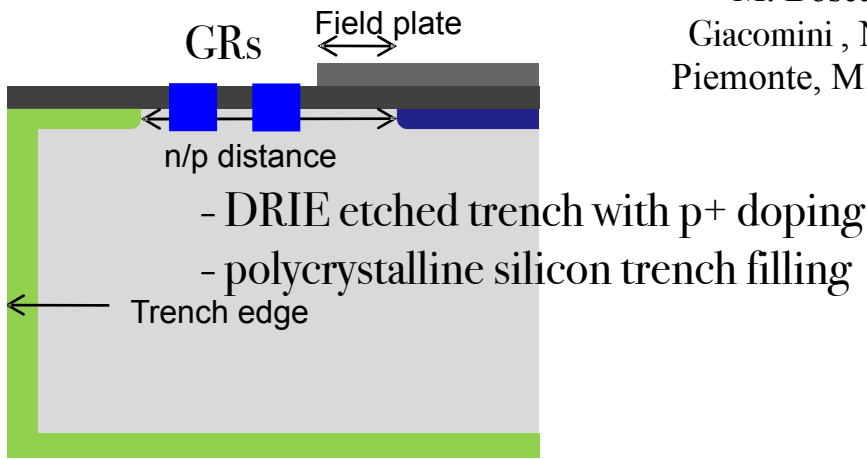
- ✓ UCSC
- ✓ Dortmund

- Post-processing → outer layers?

# LPNHE – FBK active edge

M. Boscardin, A. Baglioni, G. Giacomini, N. Zorzi, E. Vianello, C. Piemonte, M. Povoli, G.F. Dalla Betta

Design – **work in progress** [www.cnrs.fr](http://www.cnrs.fr)



Trench definition and etching

- Aspect Ratio **1/20**
- Deep etching (**200-230  $\mu\text{m}$** )

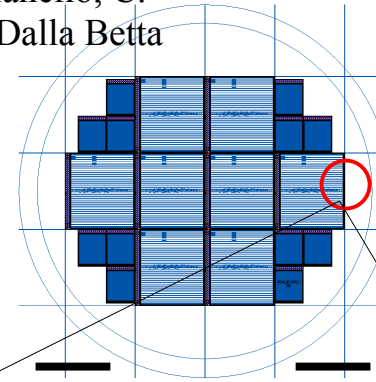
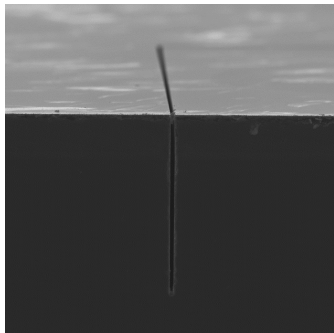
Trench filling

- Trench **width 8-12  $\mu\text{m}$**

Further trench optimization

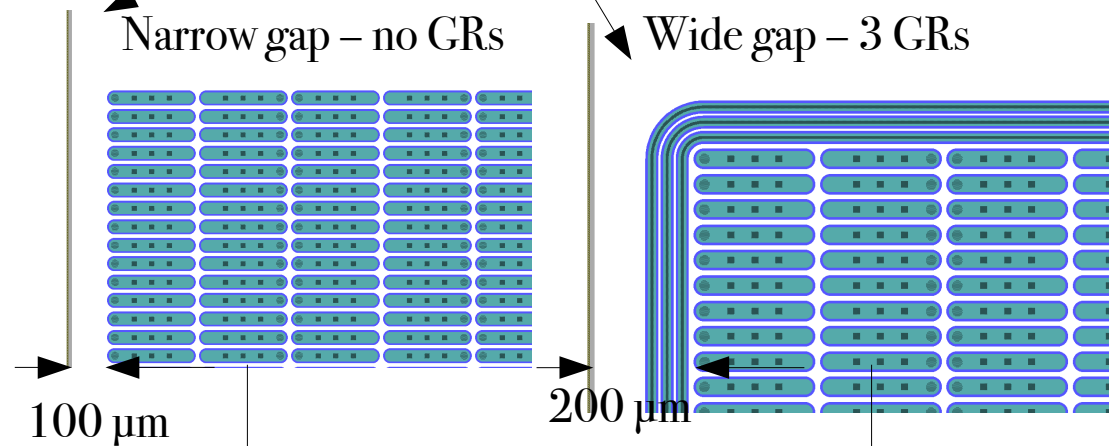
- Trying to reduce trench to **less than 10  $\mu\text{m}$**
- **Easier to fill the trench**

4.5  $\mu\text{m}$  wide  
220  $\mu\text{m}$  deep

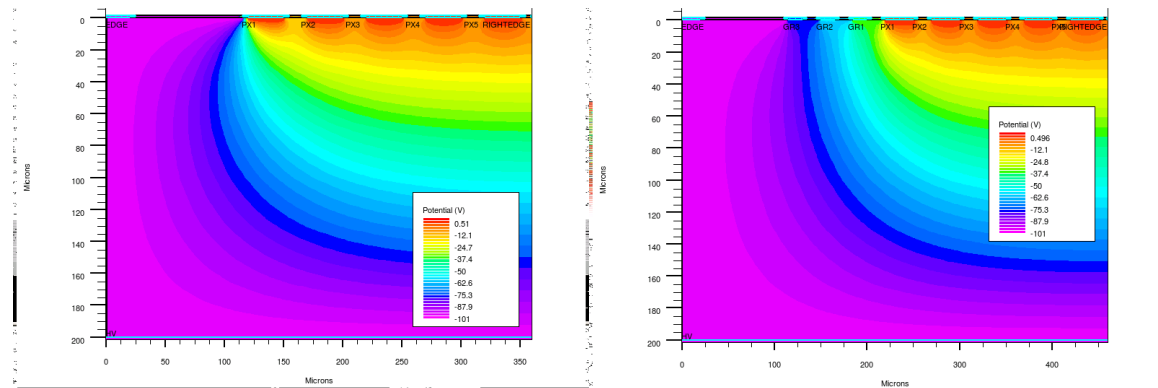


On 4 inch wafer:

- 8 FEI4
- 12 FEI3
- Test structures (diodes, ...)

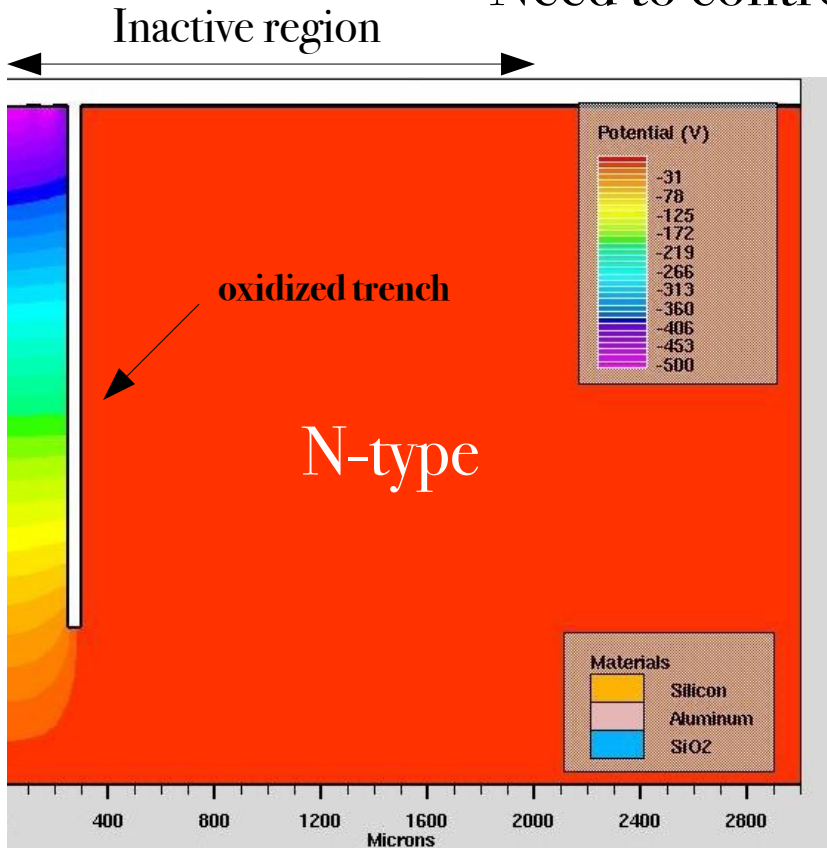


Potential maps @ 100 V



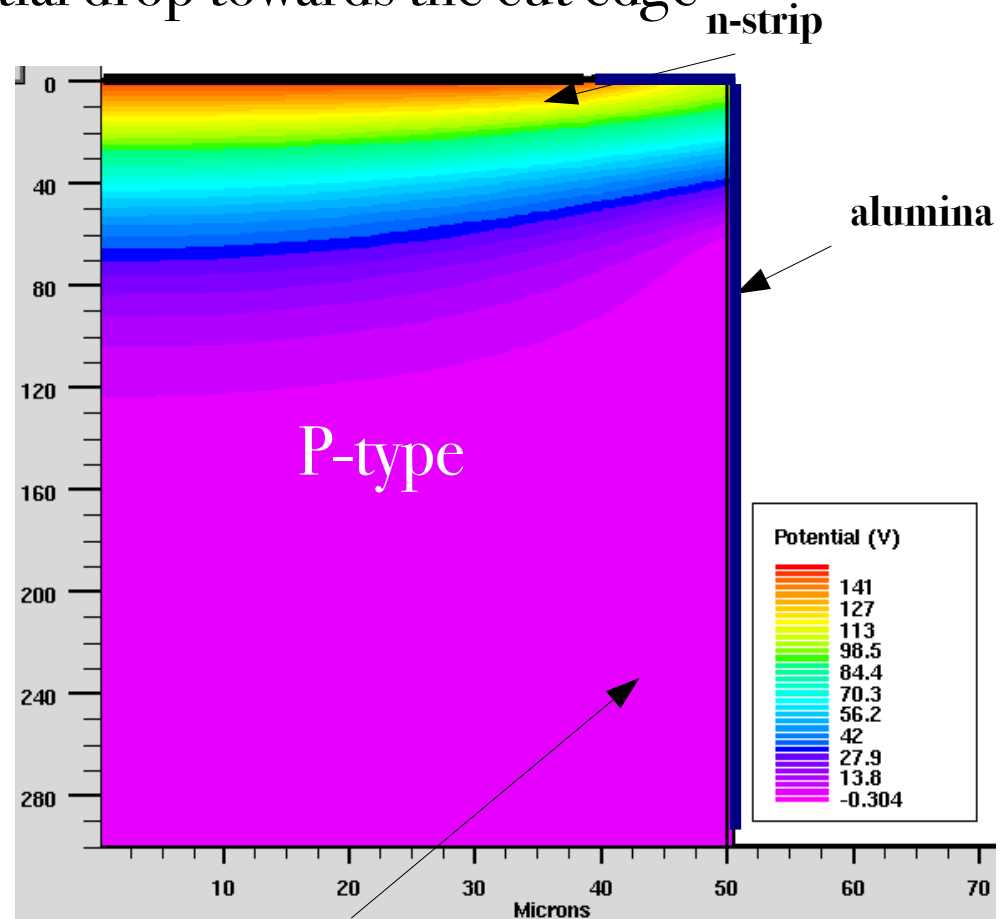
# Passivated trench

→ Need to control potential drop towards the cut edge



A passivated trench with a thermally grown oxide (**positive** charge density  $10^{11} \text{ cm}^{-2}$ ) trench will lead to:

- ✓ control potential drop toward the cut edge,
  - ✓ protection from saw cut edge.
- Scribe + nitride/oxide deposit approach too

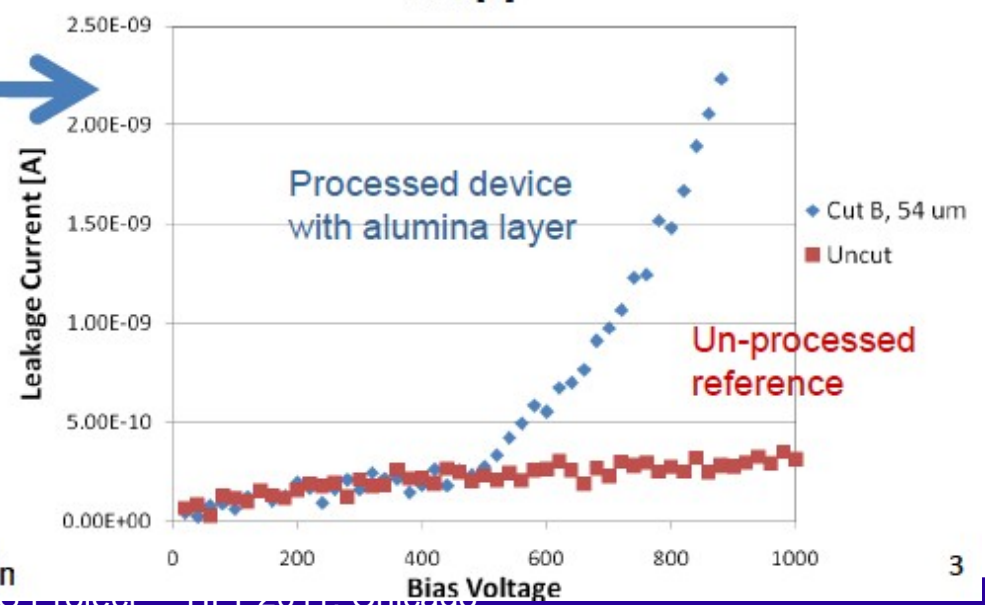
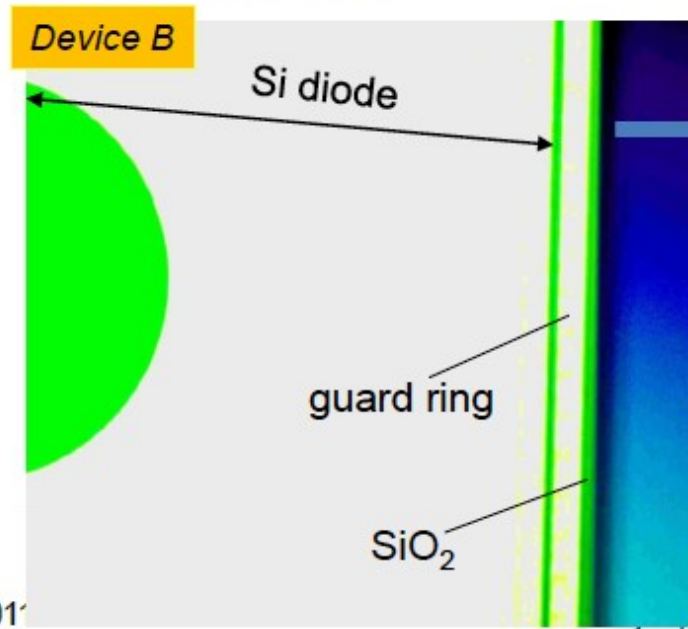
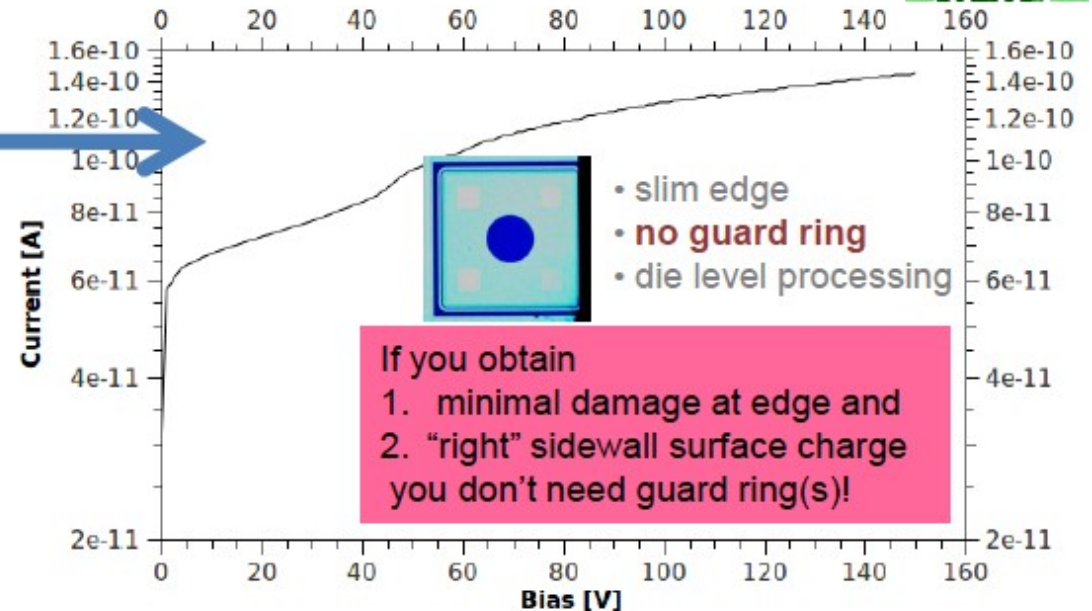
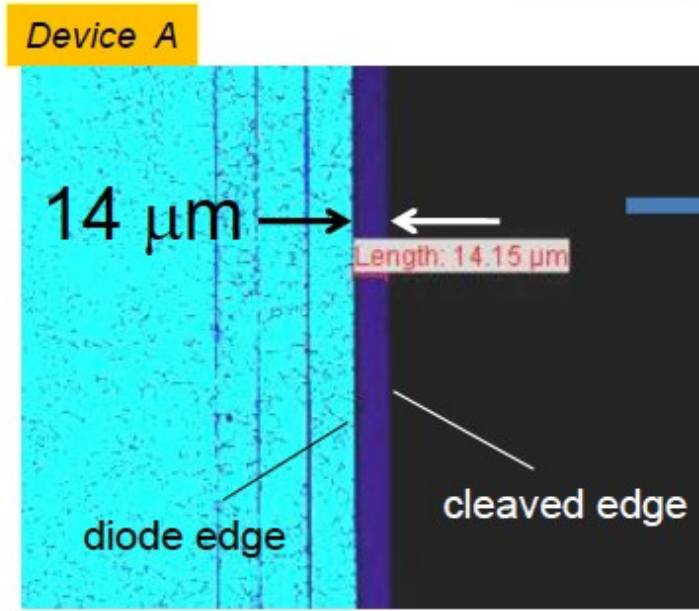


Negative charge ( $-1E11 \text{ cm}^{-2}$ )

- Alumina deposition by ALD
  - ✓ Partially controlled potential drop towards the cut edge
- The more charge, the better

# P-type passivated trench

## Examples of Processed Devices



- **Planar Pixel** is a **proven technology**
- **N-in-n** modules are fully efficient at  $5 \times 10^{15}$ 
  - Hit **efficiency** at **99.6%**
  - ... and still **collect charge** at  $2 \times 10^{16}$
- Many **on-going n-in-p** productions (target: **post-IBL upgrades**)
- Optimization of the geometry is crucial to **maximize active area**
  - **Slim edge**: encouraging **results** from **test-beam**
  - **Active edge**: several activities with **brand new ideas** too
- **Next**: more **test-beams**, **irradiation** campaigns with current & new **geometries**

Thank you!

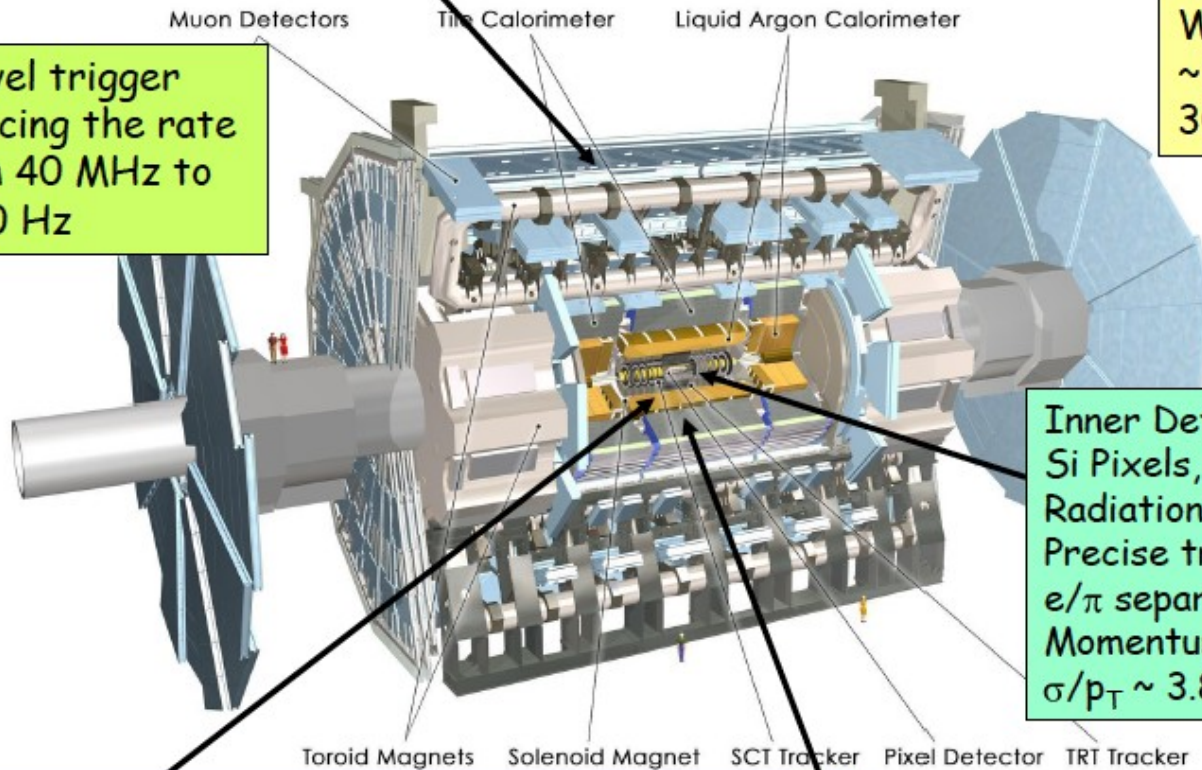
# Backup



Muon Spectrometer ( $|\eta| < 2.7$ ) : air-core toroids with gas-based muon chambers  
 Muon trigger and measurement with momentum resolution  $< 10\%$  up to  $E_\mu \sim 1$  TeV

Length :  $\sim 46$  m  
 Radius :  $\sim 12$  m  
 Weight :  $\sim 7000$  tons  
 $\sim 10^8$  electronic channels  
 3000 km of cables

3-level trigger  
 reducing the rate  
 from 40 MHz to  
 $\sim 200$  Hz

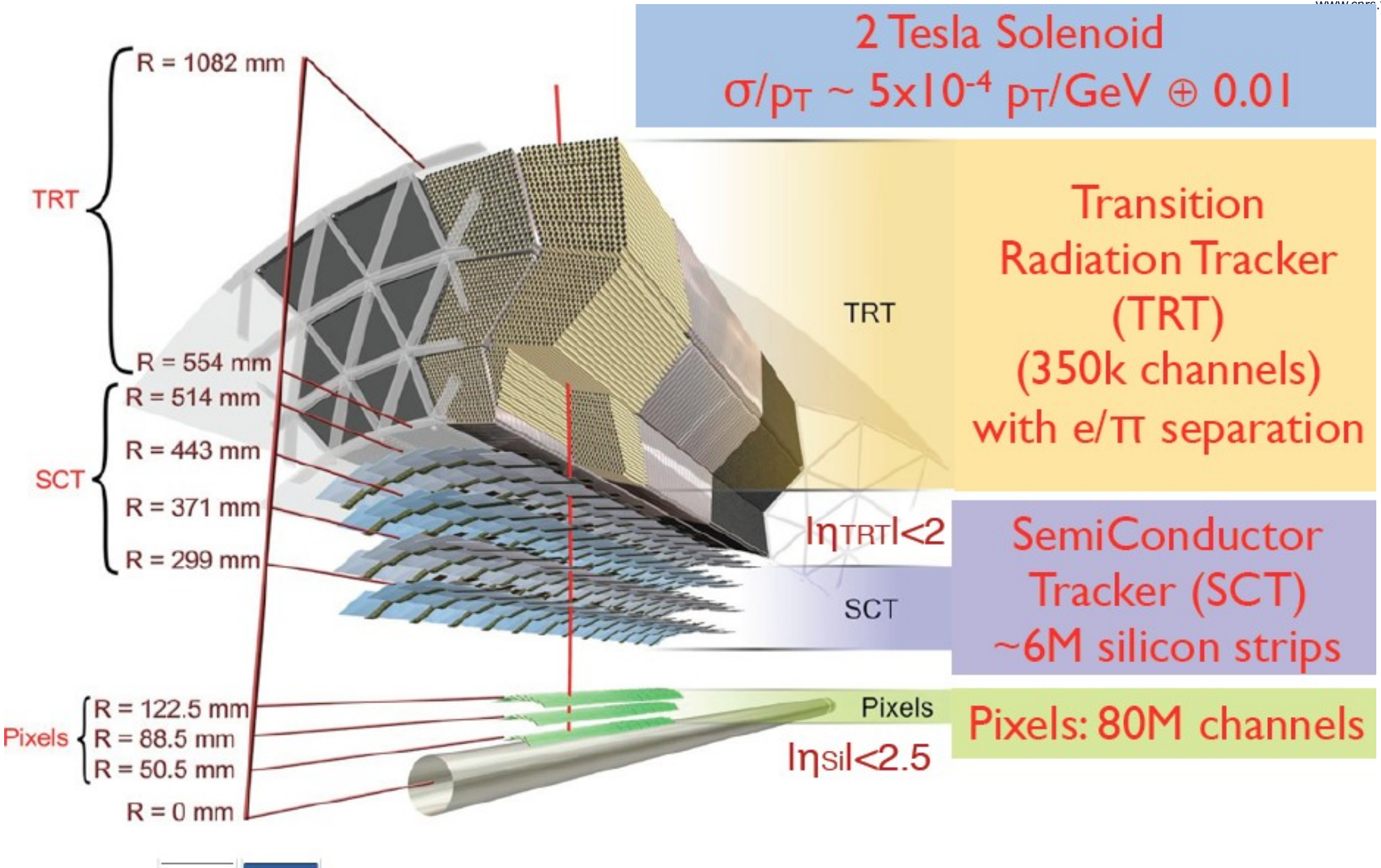


Inner Detector ( $|\eta| < 2.5, B=2T$ ):  
 Si Pixels, Si strips, Transition  
 Radiation detector (straws)  
 Precise tracking and vertexing,  
 $e/\pi$  separation  
 Momentum resolution:  
 $\sigma/p_T \sim 3.8 \times 10^{-4} p_T (\text{GeV}) \oplus 0.015$

EM calorimeter: Pb-LAr Accordion  
 $e/\gamma$  trigger, identification and measurement  
 E-resolution:  $\sigma/E \sim 10\%/\sqrt{E}$

HAD calorimetry ( $|\eta| < 5$ ): segmentation, hermeticity  
 Fe/scintillator Tiles (central), Cu/W-LAr (fwd)  
 Trigger and measurement of jets and missing  $E_T$   
 E-resolution:  $\sigma/E \sim 50\%/\sqrt{E} \oplus 0.03$

# Atlas Inner Detector



- **Inactive area** should be kept at minimum
  - e.g. Inner layers: no shingling in z

- **Two designs** for n-bulk sensors

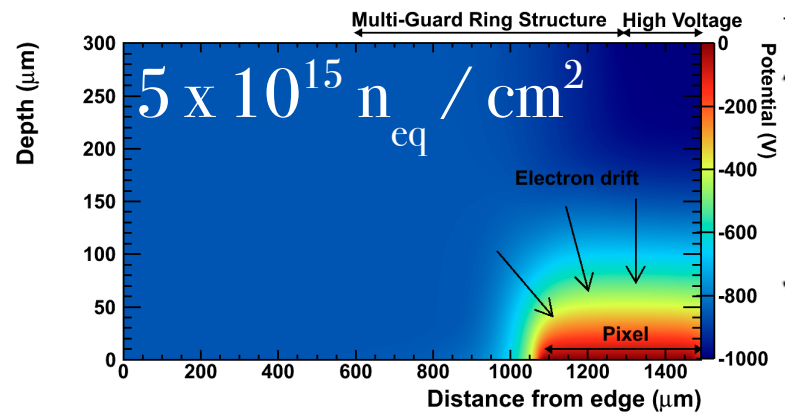
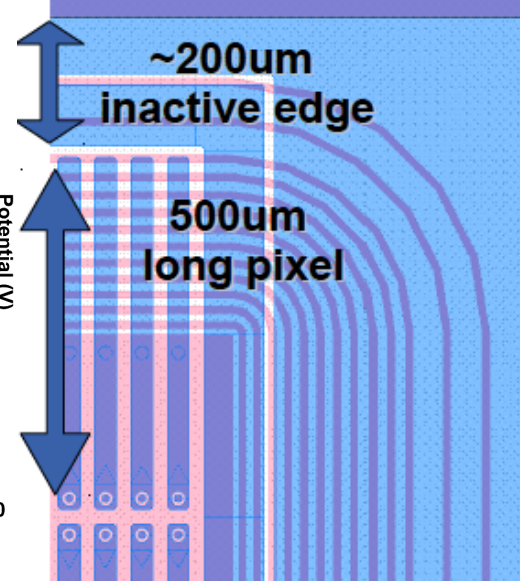
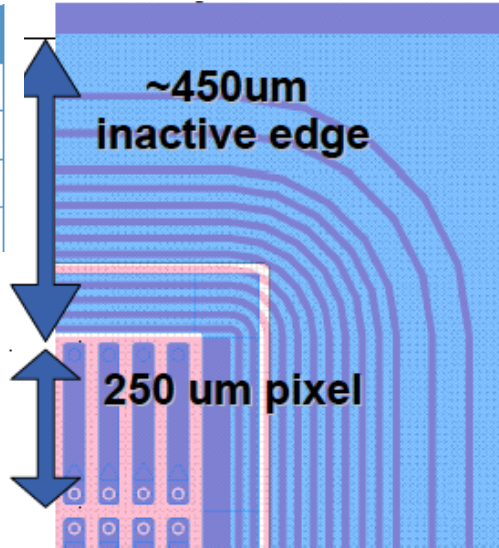
- **Conservative design**

- Similar to current ATLAS pixels
- $\sim 450 \mu\text{m}$  of inactive edge width
- Electrical field at edges homogeneous

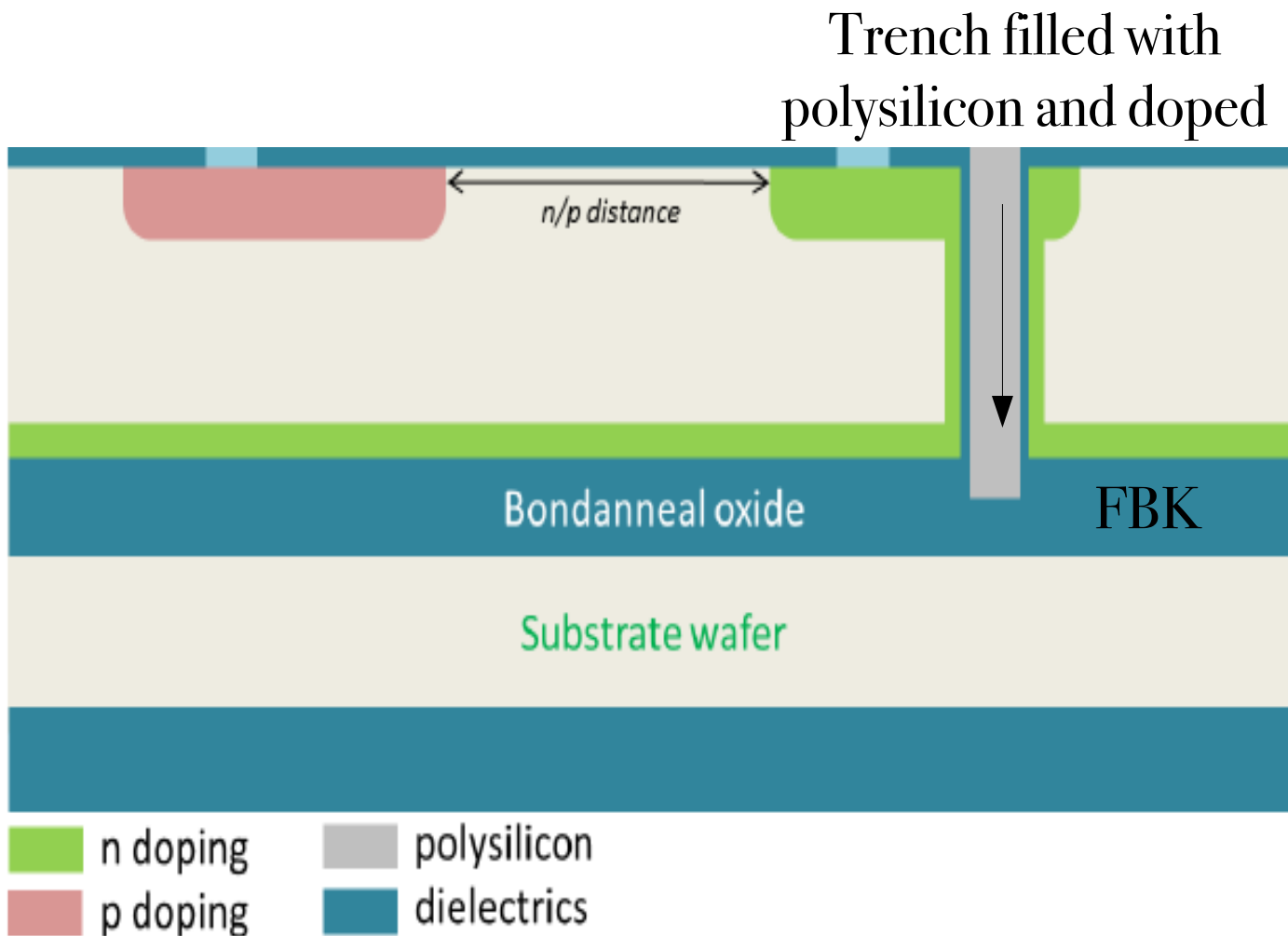
- **Slim edge design**

- **Guard rings on p-side shifted beneath the outermost pixels**  $\rightarrow$  least possible inactive edge
- Less homogeneous field
- But ok at large fluences thanks to space charge inversion

	FE-I3	FE-I4
Pixel size [ $\mu\text{m}^2$ ]	50x400	50x250
Pixel array	18x160	80x336
Chip size [ $\text{mm}^2$ ]	7.6x10.8	<b>20.2x19.0</b>
Active fraction	74%	89%



# Drie etching + trench fill



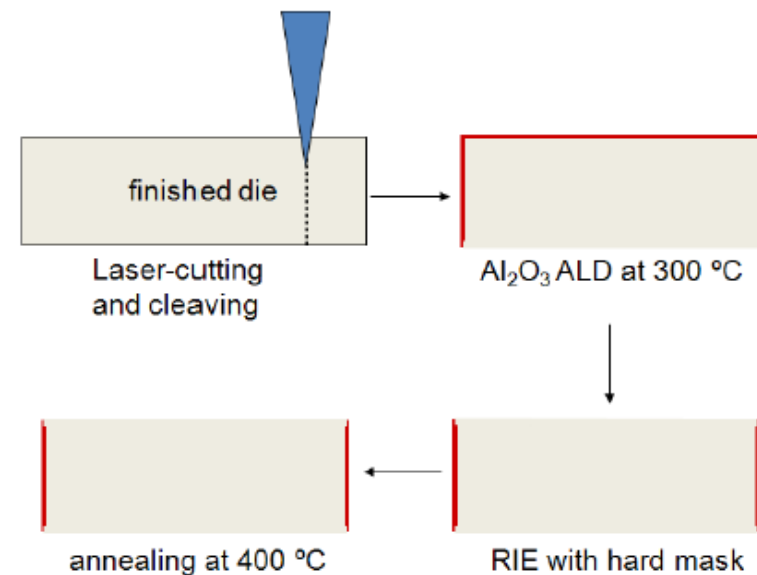
## ALD Processing on p-type Sensors



For p-type sensors the critical step is formation of proper passivation on the surface. The quickly forming Si oxide has a detrimental effect. Alumina deposition by ALD (left) leads to the desirable properties.

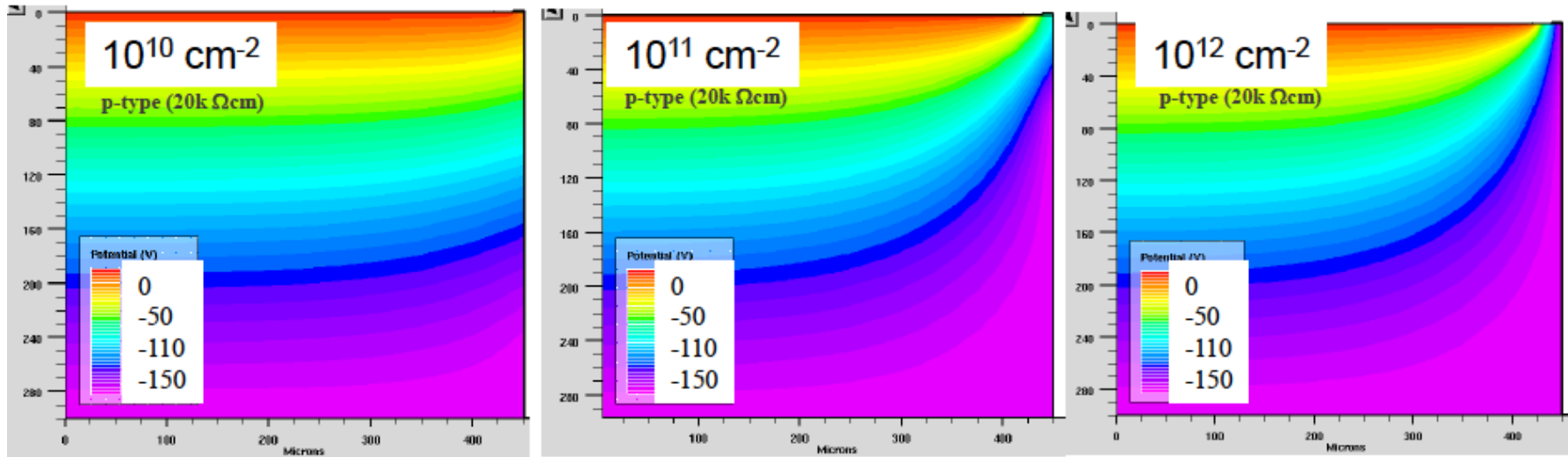
- So far worked with diodes from ATLAS07 batch from HPK (next slide) and strip sensors made by HLL.
- Processed the total of 5 diodes and 2 strip sensors.
- Also need to investigate radiation effects.

### Fabrication Sequence





## Influence of Surface Charge Concentration: P-Si/Al<sub>2</sub>O<sub>3</sub>



*increasing negative surface charge*

Typical literature values for alumina are ~  $10^{11} - 10^{13} \text{ cm}^{-2}$  depending on deposition conditions. BUT most research is focused on increasing (*not decreasing*) surface charge.

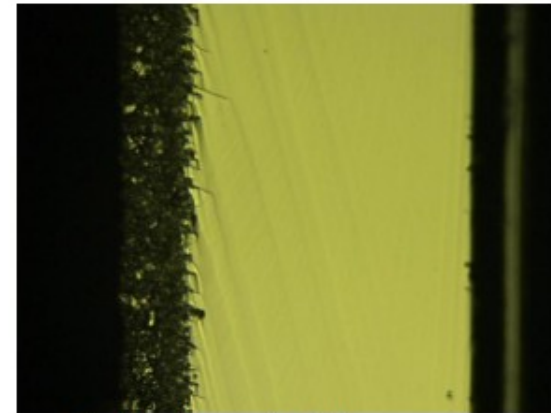
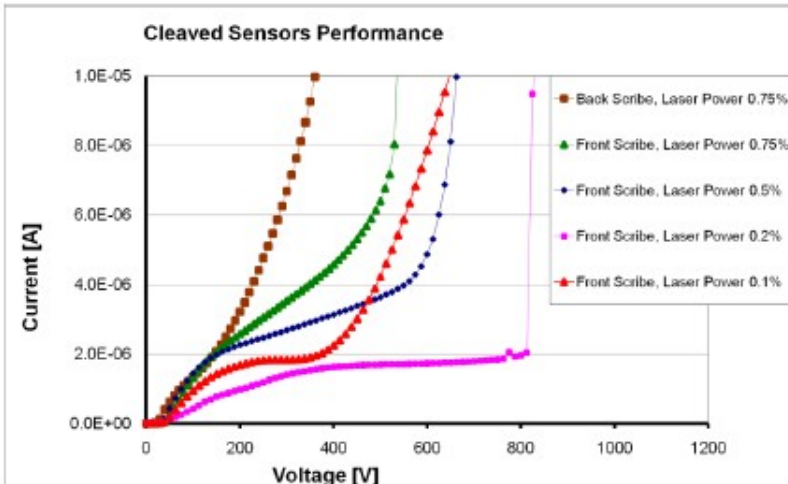
**The potential drop at edge depends strongly on surface charge density.**

# Passivated trench

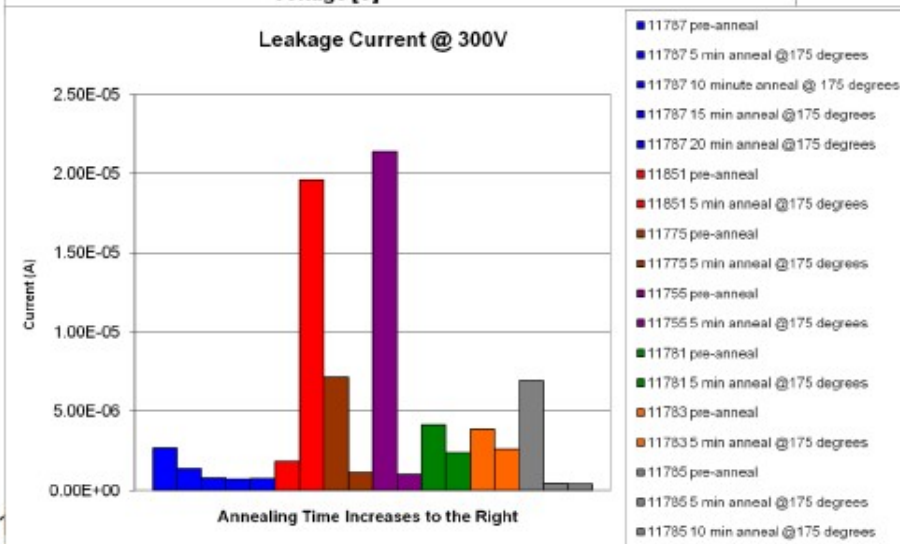
## N-bulk sensors



- Processing of n-bulk sensors is easier, since formation of  $\text{SiO}_2$  passivates the sidewall. Prototyped with p-on-n HPK sensors from GLAST/Fermi production.



Edge illumination



These sensors were breaking down at relatively high voltages, 100s of volts. Performance improves with high-temperature exposure which facilitates formation of  $\text{SiO}_2$  on the sidewall surface.

20

y post-processing

6



## The FE-I4 front-end

- Reason for a new FE design:
  - Increased rad hard
  - New architecture to reduce inefficiencies ( $L=3 \times \text{LHC}$ )
- Biggest chip in HEP to date
- Greater fraction of footprint devoted to pixel array
- Lower power: *don't move the hits around unless triggered*
- Able to take higher hit rate: *store the hits locally in each pixel and distribute the trigger*
- No need for extra module control chip: *significant digital logic block on array periphery*
- Present status: *Submission end of June 2010*

### Design collaboration (15 IC designers):

Bonn, CPPM, INFN-Genova, LBNL, NIKHEF

### Specification & test setup development:

Bonn, CERN, Goettingen, LBNL

IPRD10, Siena 9.6.2010 - Alessandro La Rosa (CERN)

- FE-I3 → FE-I4

	FE-I3	FE-I4
Pixel size [ $\mu\text{m}^2$ ]	50x400	50x250
Pixel array	18x160	80x336
Chip size [ $\text{mm}^2$ ]	7.6x10.8	<b>20.2x19.0</b>
Active fraction	74%	89%
Analog current [ $\mu\text{A}/\text{pix}$ ]	26	<b>10</b>
Digital current [ $\mu\text{A}/\text{pix}$ ]	17	<b>10</b>
Analog voltage [V]	1.6	<b>1.5</b>
Digital voltage [V]	2.0	<b>1.2</b>
Pseudo-LVDS out [Mb/s]	40	<b>160</b>

