



In2p3

LIR



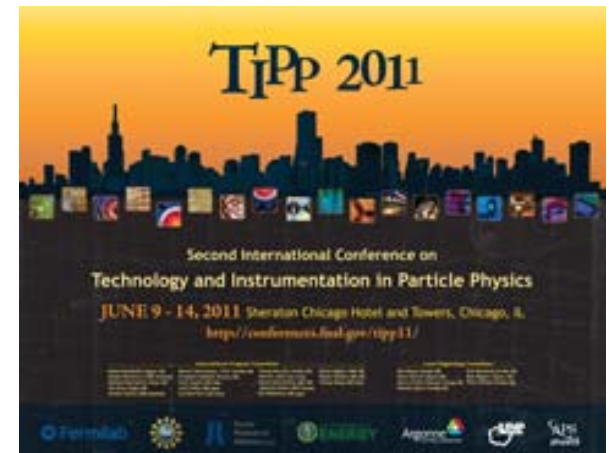
Data Acquisition system and detector interface for power pulsed detectors

Rémi Cornat

Laboratoire Leprince-Ringuet

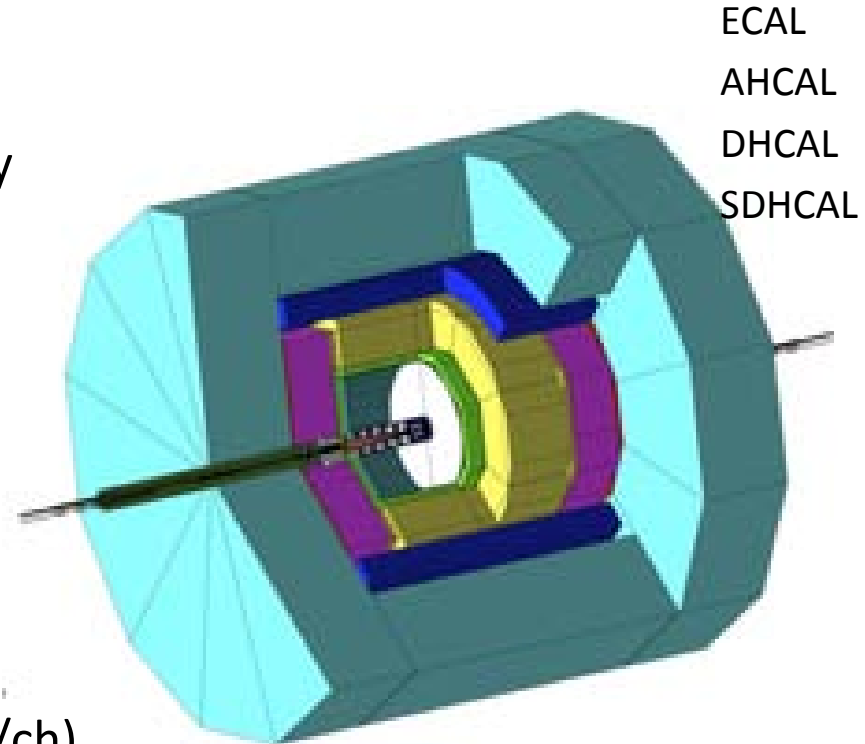
Ecole Polytechnique – IN2P3/CNRS

On behalf of the CALICE collaboration



CALICE collaboration looking at detectors for ILC

- Particle flow method: imaging calorimetry
10-100 10^6 channels / detectors
- Issues:
Integration
Power consumption
- Ideas:
Detectors prototypes
Power pulsing (1% duty cycle = $\sim 25 \mu\text{W}/\text{ch}$)
allowed due to the beam structure (5 Hz spills)
Data acquisition and control
A Single cable for everything
Scalable architecture inspired from computing network
Reliable protocols & simplicity



Expectations for a DAQ system

- **Scalable**
 - Computing network architecture
- **Standard**
 - Giga-Ethernet
 - Serial 8b10B
 - Cables and connectors
 - Hdmi : 5 pairs + supplies
 - CAT5 or fibre
 - Backplane-less
 - **Detector interface (DIF) unified among the detectors (CALICE standard)**
- **Compact**
 - “one cable for everything” : Data Acquisition, Timing, Slow control
- Flexible (prototypes)
 - (re)programmable parts (fpga)
- Cheap : Off the Shelf components

R&D from Univ. College London, Manchester Univ., Cambridge Univ., Royal Holloway ; continued at LLR-Ecole Polytechnique / IN2P3-CNRS



Limitations

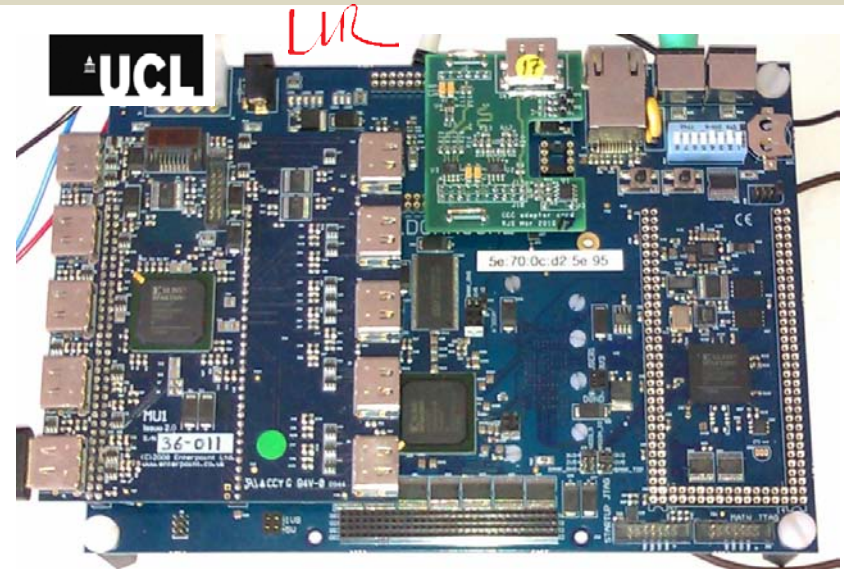
- Low speed access to a chain of 10-100 very front end chips (1k-10k channels) : 1-5 Mbit/s
 - daisy chain and reduced number of connections for compactness,
 - up to 2 m PCB traces,
 - low power consumption at VFE chip level : open collector bus
- Therefore assume : auto trigger, zero suppression at VFE level
- TFC interleaved with SC, DAQ using 8b/10b protocol : limited timing precision (>10 ns)
- Events build at VFE level, read out during inter-spill train : limited buffering capacity (10-100 evt)

Low occupancy of the detectors is assumed (<0.5%/cell/bunch)

Prototypes of LDA & DCC

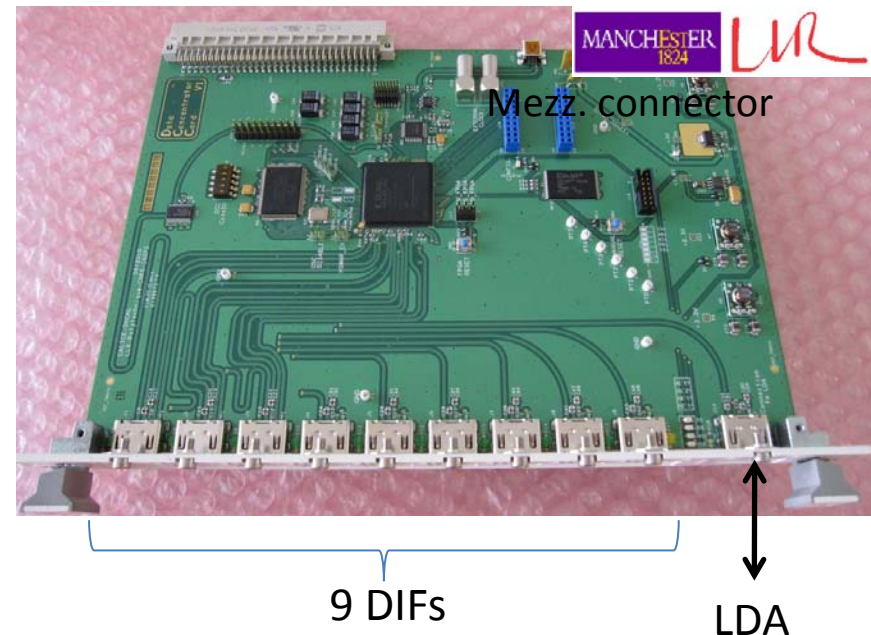
Local Data Aggregator

- 1:10 switch
- Giga-Ethernet upstream
- Custom serial link downstream
- CCC link



Data Concentrator Card

- 1:9 switch, multiplexed buffers
- Custom serial link upstream
- Custom serial link downstream



Custom serial link

3 twisted pairs + 2 optional :

- **reference clock** (50 - 100 MHz), fan-out from CCC
 - **data in** (fast control, slow control, data)
 - **data out** (slow control, data, det. Read-out)
 - trigger (used for test beams if not ILC structure)
 - busy (used for test beams if not ILC structure)
-
- HDMI connector & cable

custom PHY layer, similar to Fast-Ethernet

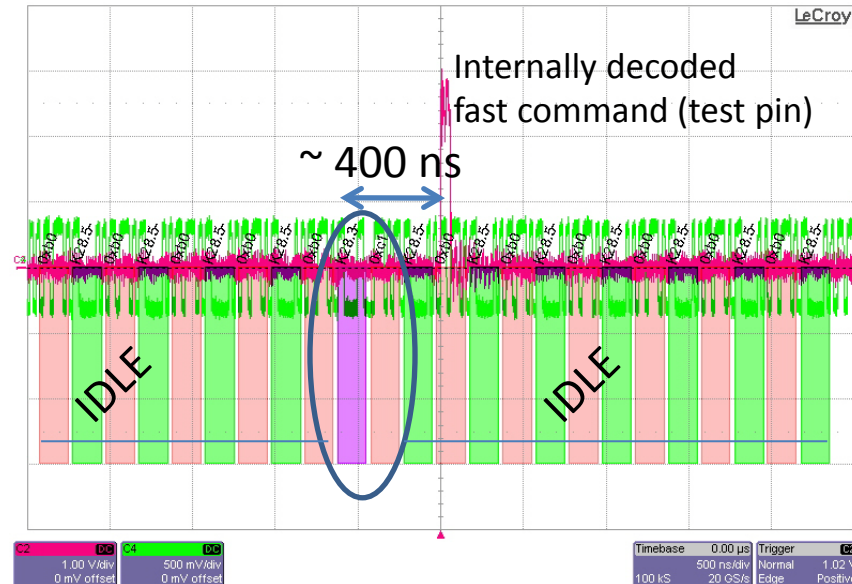
- PMD : 3 LVDS pairs (clk, din, dout)
- PMA : Word size extended to 16b same 8b/10b characters as for ethernet
- PCS : 16b/20b for data

Simple MAC layer for synchronization

- IDLE detection (carrier)
- Word clock alignment

FAST control commands sent from a central CCC board

broadcasted Control + Data characters interleaved with data flow

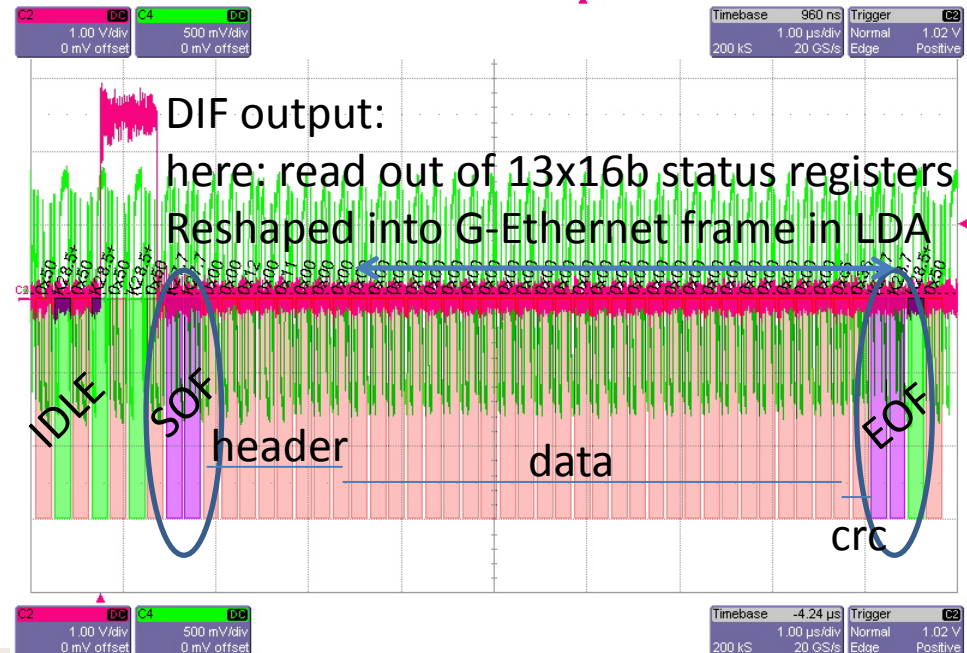
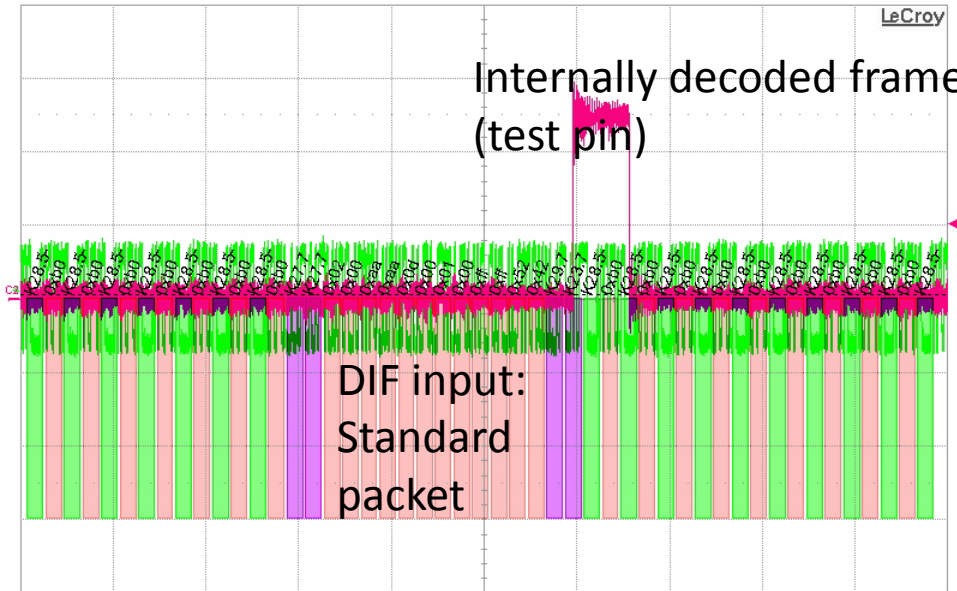


Slow control and read-out

Sent from the DAQ/Control PC as a normal ethernet frame passed to/from the DIF via LDA / DCC

Packets have a simple structure

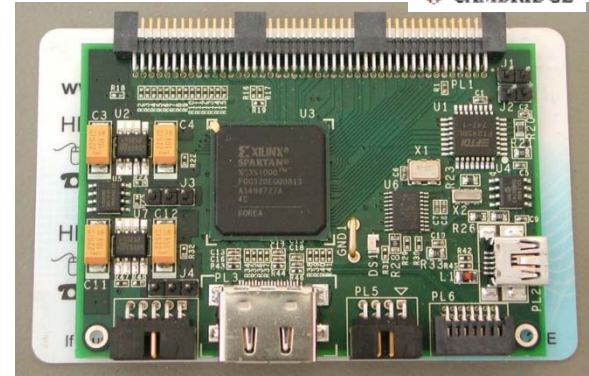
header	Type ID Sub type Size
...	
Data	506 words max.
...	
CRC	16b



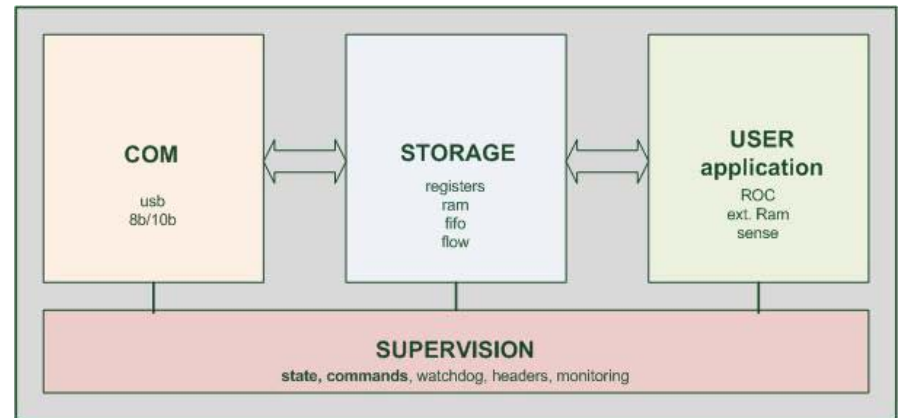
Detector InterFace (DIF) board



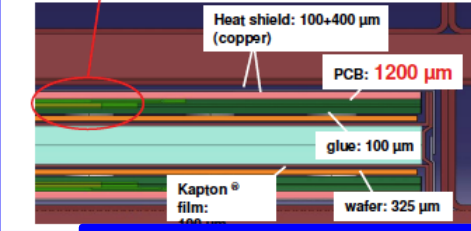
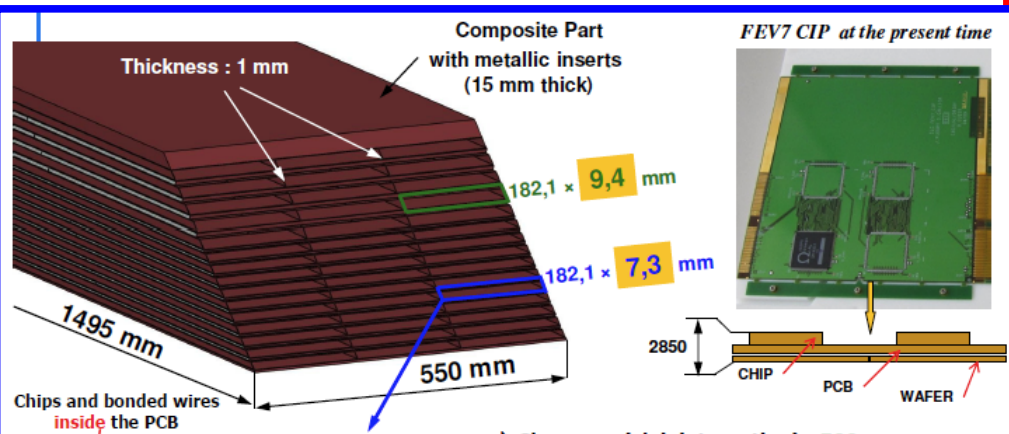
ECAL version



- Can use the same hardware for every detector
 - Based on low cost fpga
 - Compact : credit card size and below
 - 7 mm thick (integration)
 - Drive 1 to 10 k channels
- Functionalities are simple
 - VFE chip management (power pulsing, SC, DAQ) with a common interface
 - Local storage of SC data (Flash ram)
 - Processor like architecture
- DIF task force (4 people)
 - LLR, DESY, LAPP, Cambridge
 - Specifications
 - **Common firmware (LLR & LAPP)**

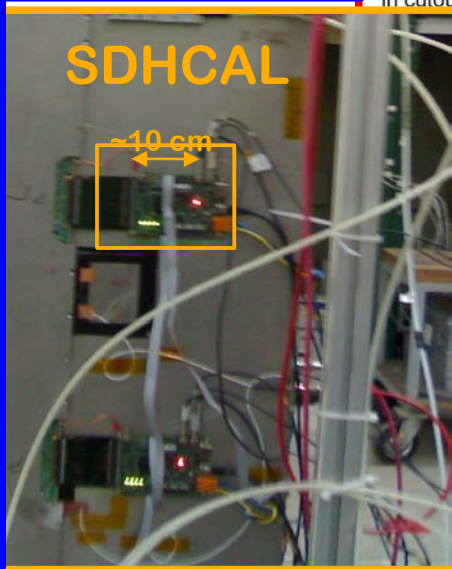
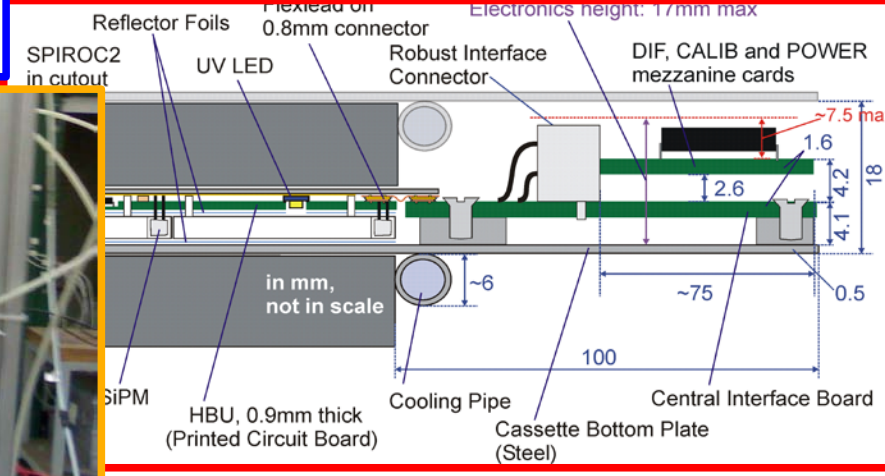
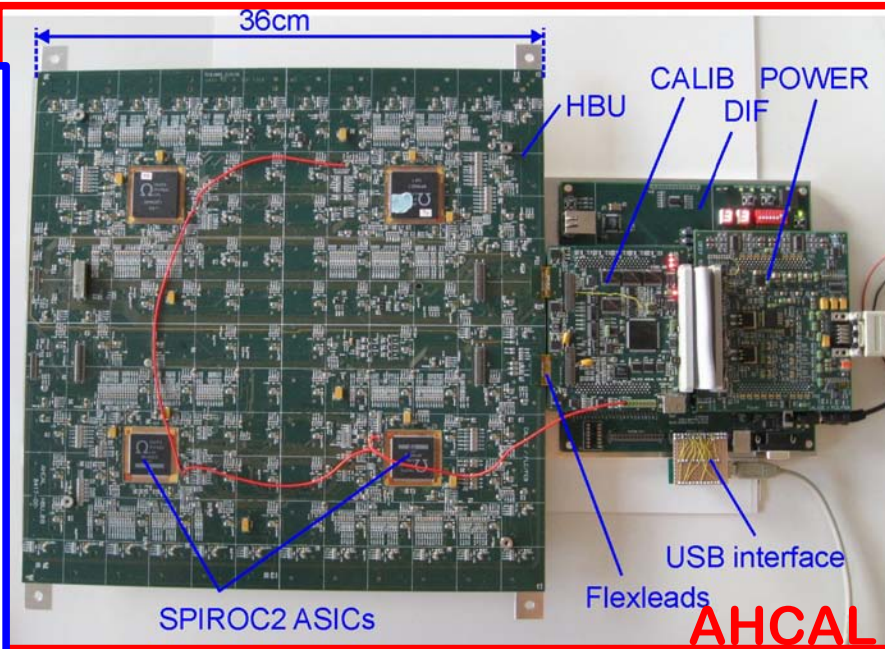


Detector interfaces



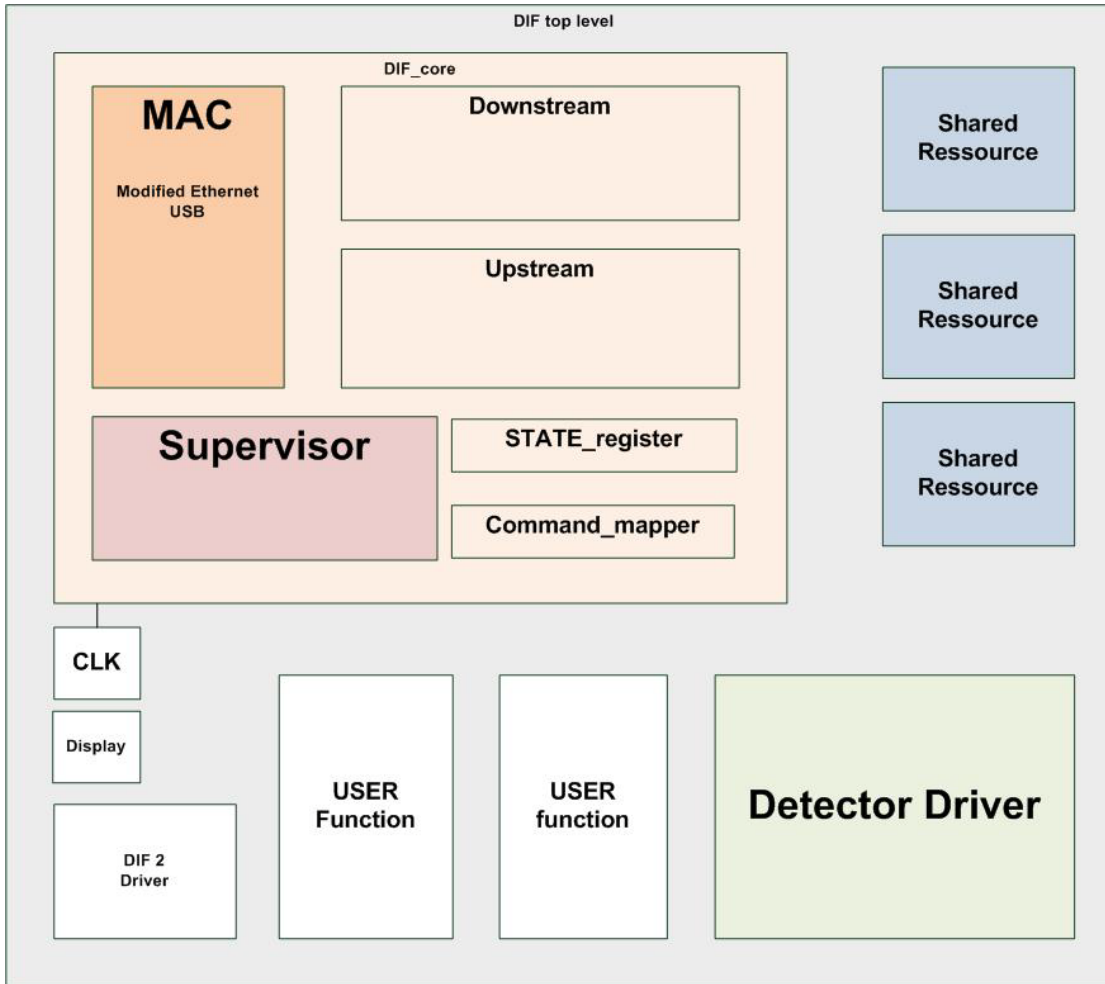
- ⇒ Clearance (slab integration) : 500 μm
- ⇒ Heat shield : 500 μm → Thermal demonstrator
- ⇒ PCB : 1200 μm → but 1100 μm used
- ⇒ Thickness of glue : 100 μm
- ⇒ Thickness of wafer : 325 μm
- ⇒ Kapton® film HV : 100 μm ? → tests
- ⇒ Thickness of W : 2100/4200 μm (± 80 μm)

ECAL



Overall architecture

Core includes MAC interface to UBS port and custom serial link and a supervisor (control of data path, ...)



RAMs, register banks, FIFO are shared at top level
DMA access allowed to/from functions

User functions to drive external devices including detectors

Upstream data path

Allow any configuration of data sources, buffers and queues interconnected thanks to switches and muxes according to detector needs

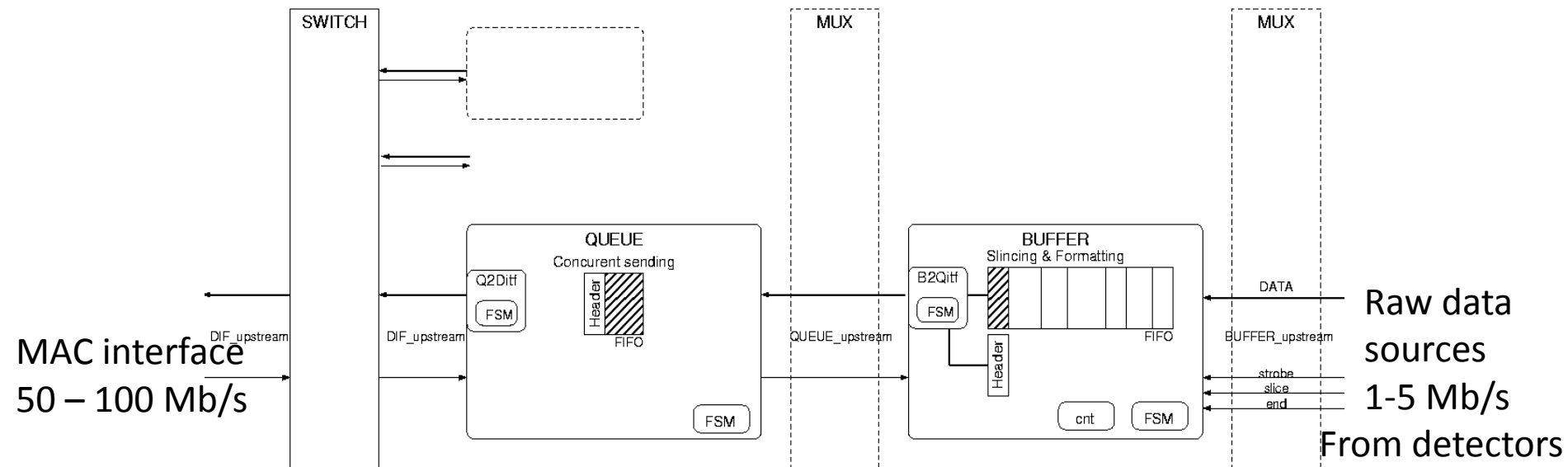
Tested with up to 15 DIFs at max. rate
Equivalent of 100 k channel detector
 10^{-13} BER

Outgoing data : 2 levels of buffering

Buffer : store raw data slices from data sources

Queue : queue single packet at the input

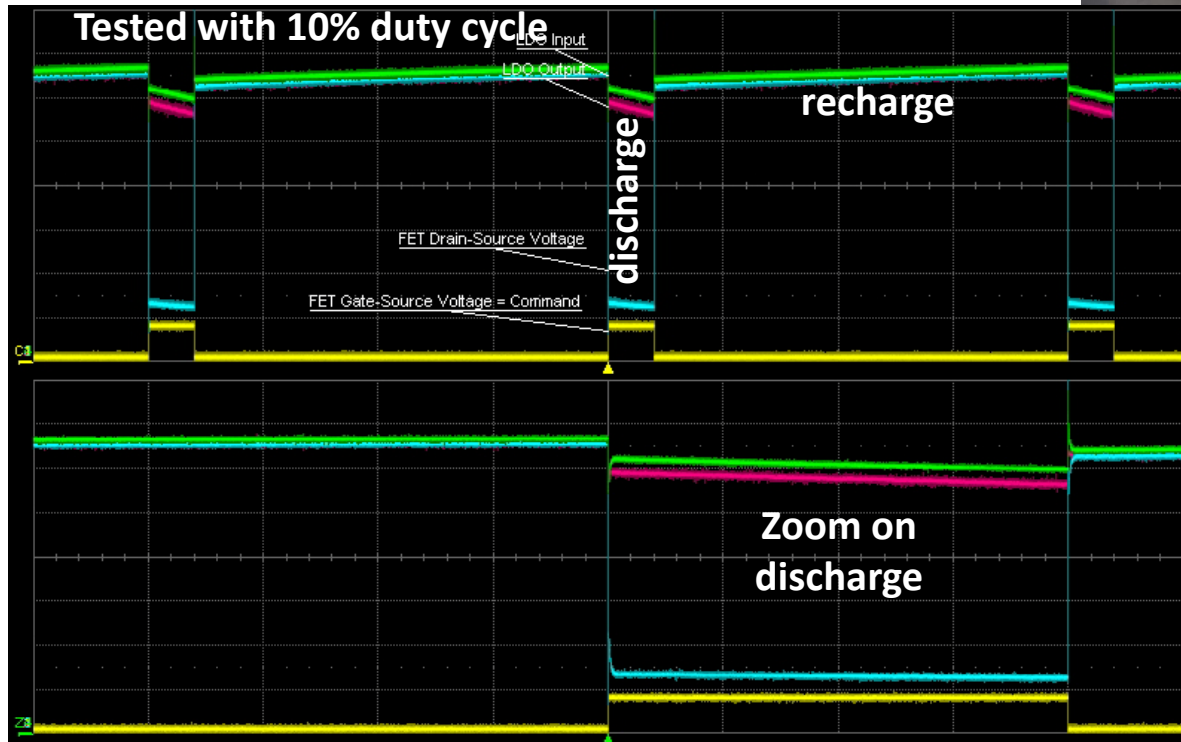
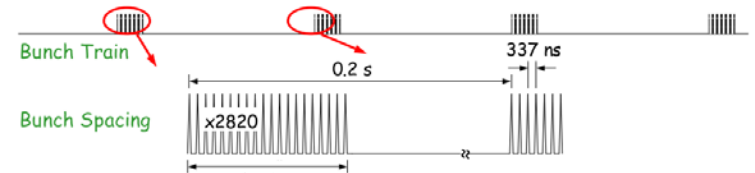
Headers can be added dynamically



Pulsed power supply

Detectors seen as variable load
Consumption from 100 mA to 10 A at 5 Hz
Duty cycle : 1% (1 ms)

Strategy : 10 to 1000 mF capacitance used
as batteries continuously recharged
with low current source (~100 mA)



Output stability :
20 mV / ms

30 μ W / channel !
+ DIF

Vout : serial resistor drop +
capacitance discharge

Drain Voltage => 6A

FET gate command (load)

Software: XDAQ framework

dev^{ts} started @IN2P3/IPNL for electronics test using XDAQ in 2008

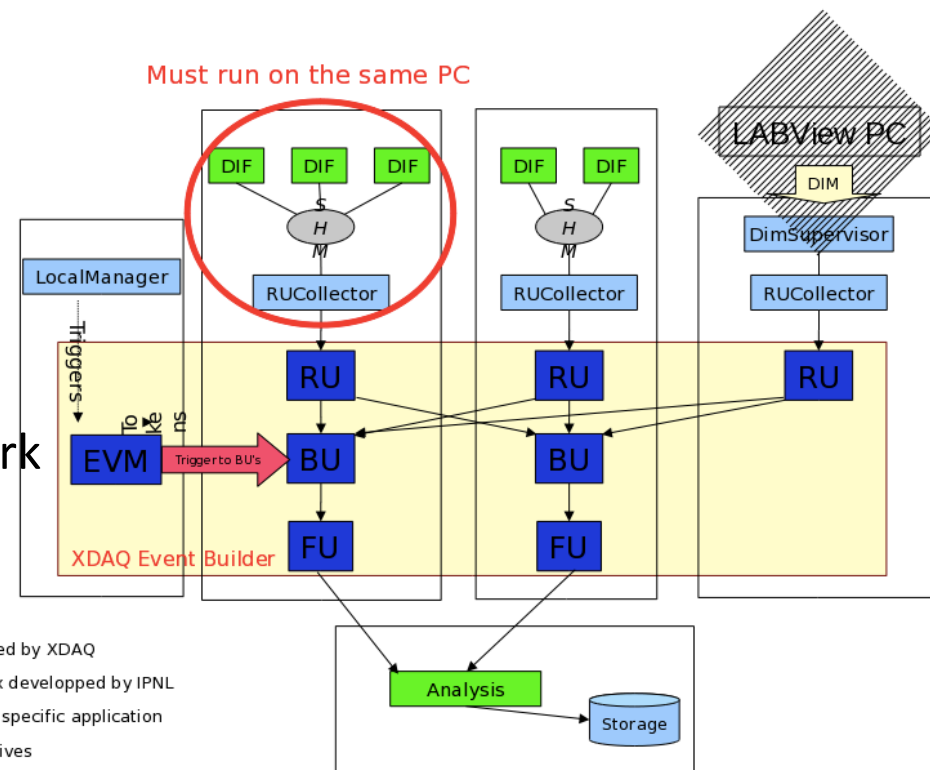
- Same architecture than for CMS tracker
- PC farm

Ran for ≥ 1 year in TB, Cosmics & Electronics test

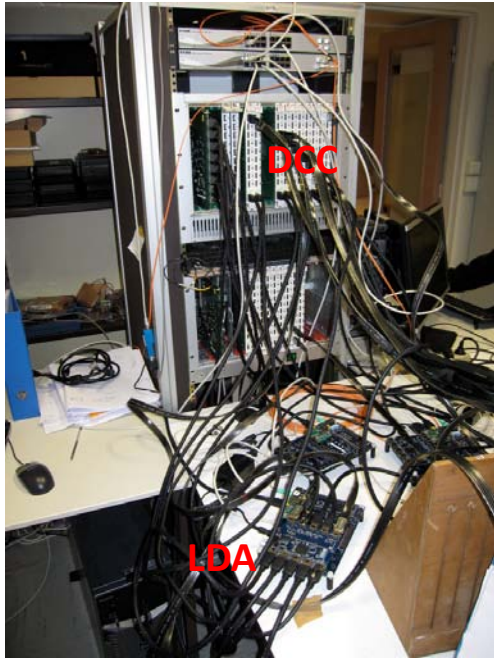
- USB readout
- Interface to old LabView (tests)

Recent development

- Interfaced to CALICE DAQ
- Configuration data base
- Writing of LCIO data
- Versatile online analysis framework (root histos) \rightarrow Marlin Based



Integration tests



Qualification tests at LLR

(Cabling procedure to be optimized)

Integration together with 400 k channels DHCAL
at IPNL, Lyon, France

Test beam at CERN next week



Conclusion

Credit card size DIF manage 1 det module $\sim 10^5$ channels

- Lightweight design, resource sharing
- Same HDL code for 3..5 detectors with common repository

Running prototype of CALICE DAQ system

- Design constraints of a detector for ILC

Next prototyping steps will allow

- Higher frequency at leaf level (x2)
- Look at 10 Geth (VTX det, ...)
- Low power mode of DAQ to be investigated

Prototype of the DAQ System deployed
for DHCAL test beam at CERN

- **400 000 channels** in 1 m³
- 120 DIF, 17 DCC, 3 LDA, **1 fibre**
- Computing network architecture

