3D IC for Real Chips

Bob Patti, CTO

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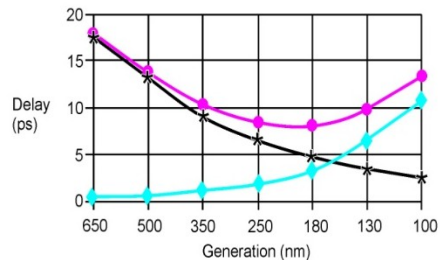
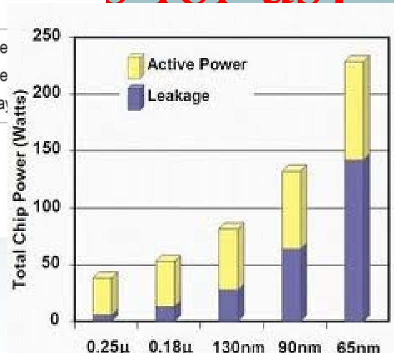
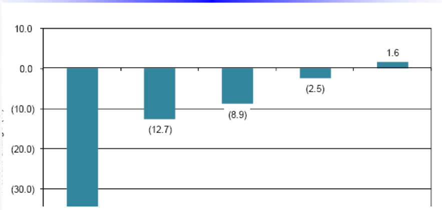
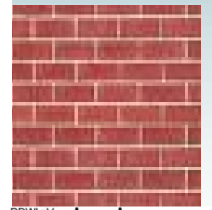
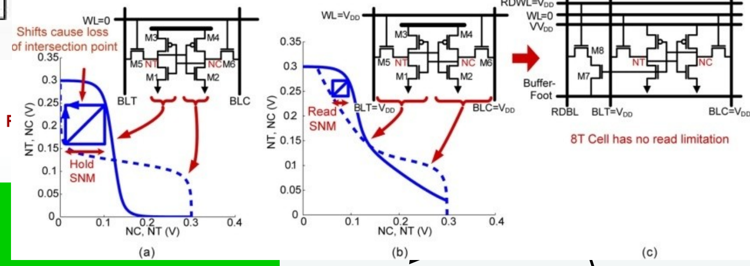
Why We Scale?











o for us?

Advantages

Speed

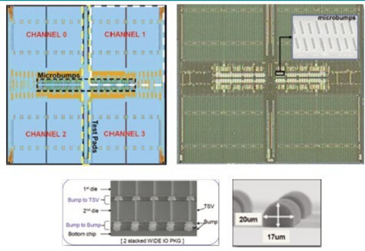
Power

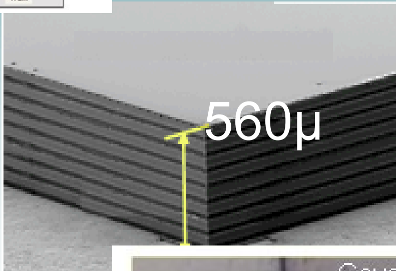
Cost

Size

>180nm 130nm 90nm 65nm 45nm 28nm 22nm 16nm

How Real is 3D???

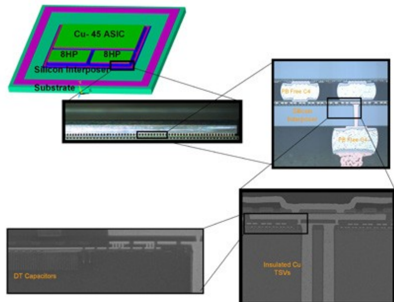


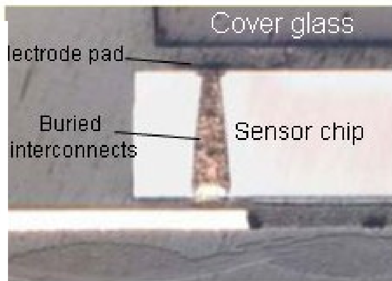


Samsung
16Gb NAND flash (2Gx8 chips), Wide Bus DRAM

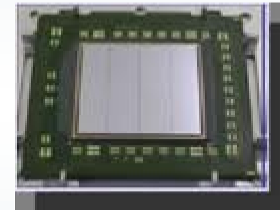
Micron
Wide Bus DRAM

Intel
CPU + memory

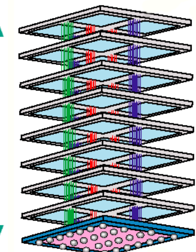


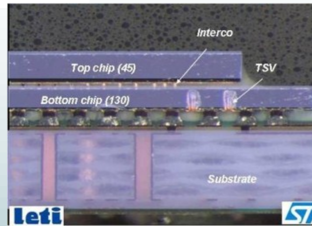


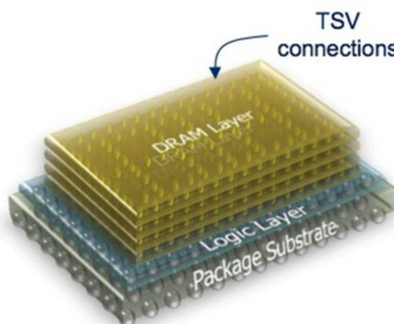
OKI
CMOS Sensor



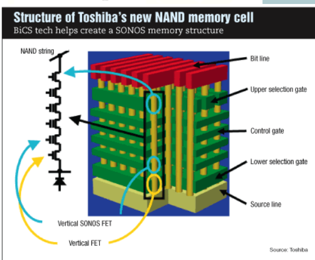
Xilinx
4 die 65nm interposer

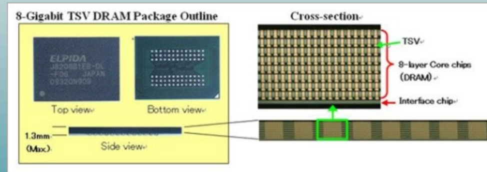






Raytheon/Ziptronix
PIN Detector Device



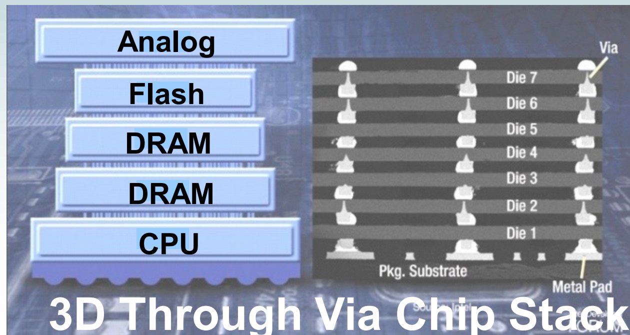


IBM
RF Silicon Circuit Board / TSV
Logic & Analog

Toshiba
3D NAND

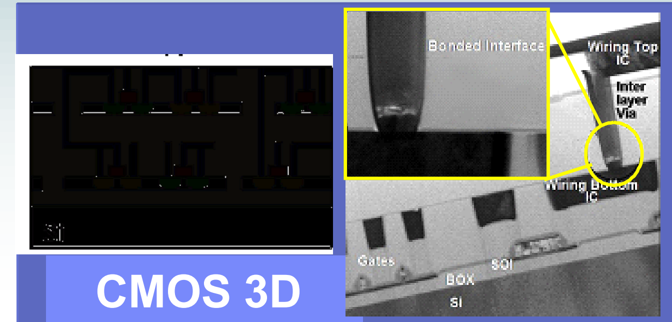
Span of 3D Integration

Packaging



IBM/Samsung

Wafer Fab



IBM

3D-ICs

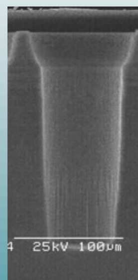
100-1,000,000/sqmm

1000-10M Interconnects/device

1s/sqmm

Peripheral I/O

- Flash, DRAM
- CMOS Sensors

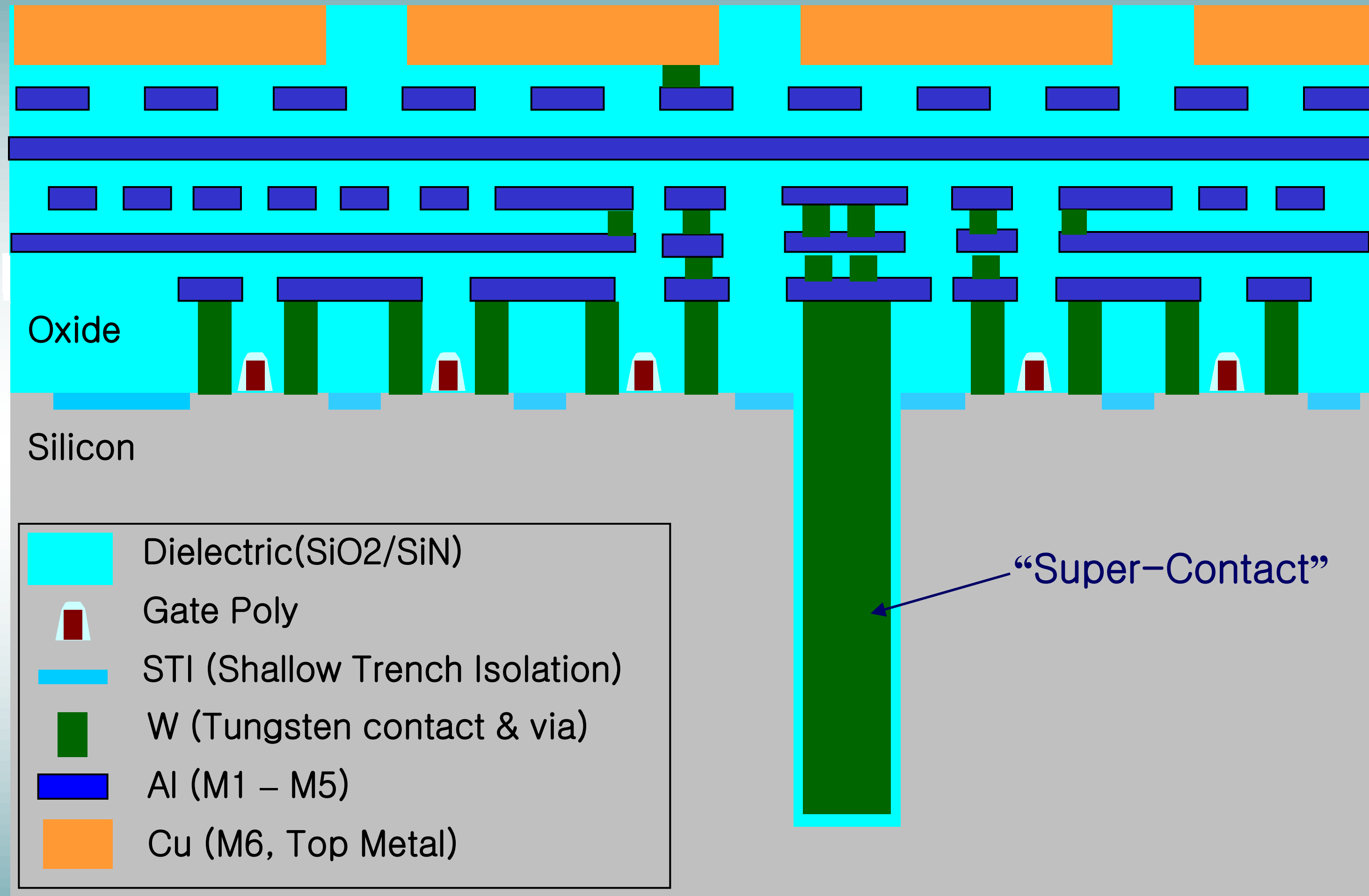


100,000,000s/sqmm

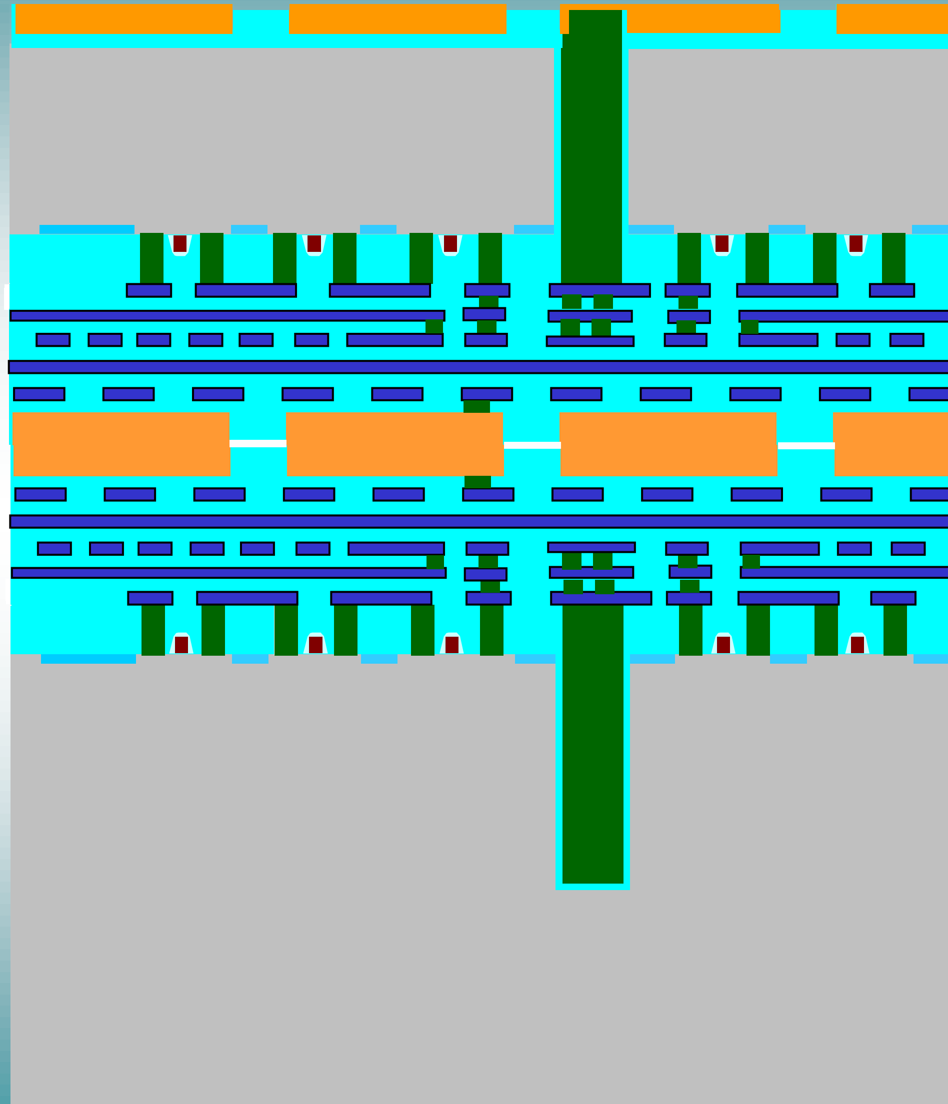
Transistor to Transistor

- Ultimate goal

A Closer Look at Wafer-Level Stacking



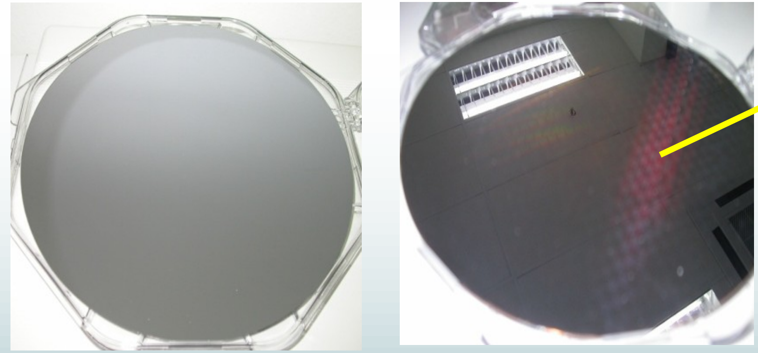
Next, Stack a Second Wafer & Thin:

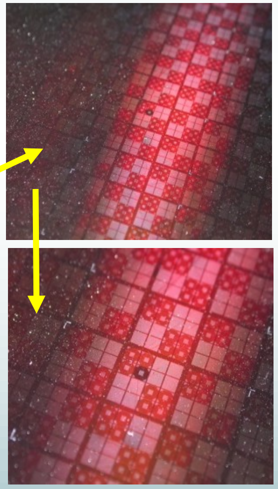


Stacking Process Sequential Picture

Two wafer Align & Bond → Course Grinded → Fine Grinded

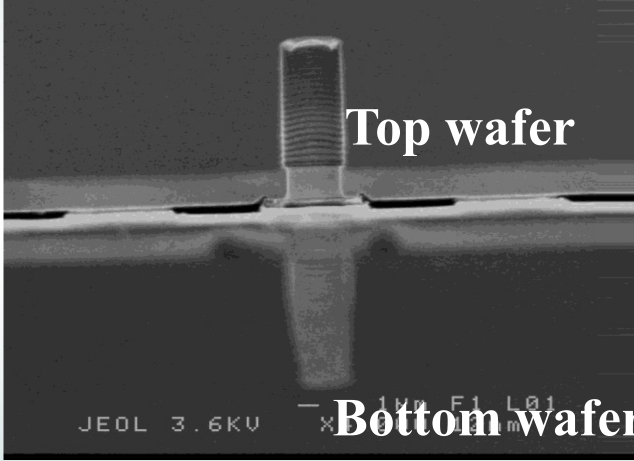
→ After CMP → Si Recessed



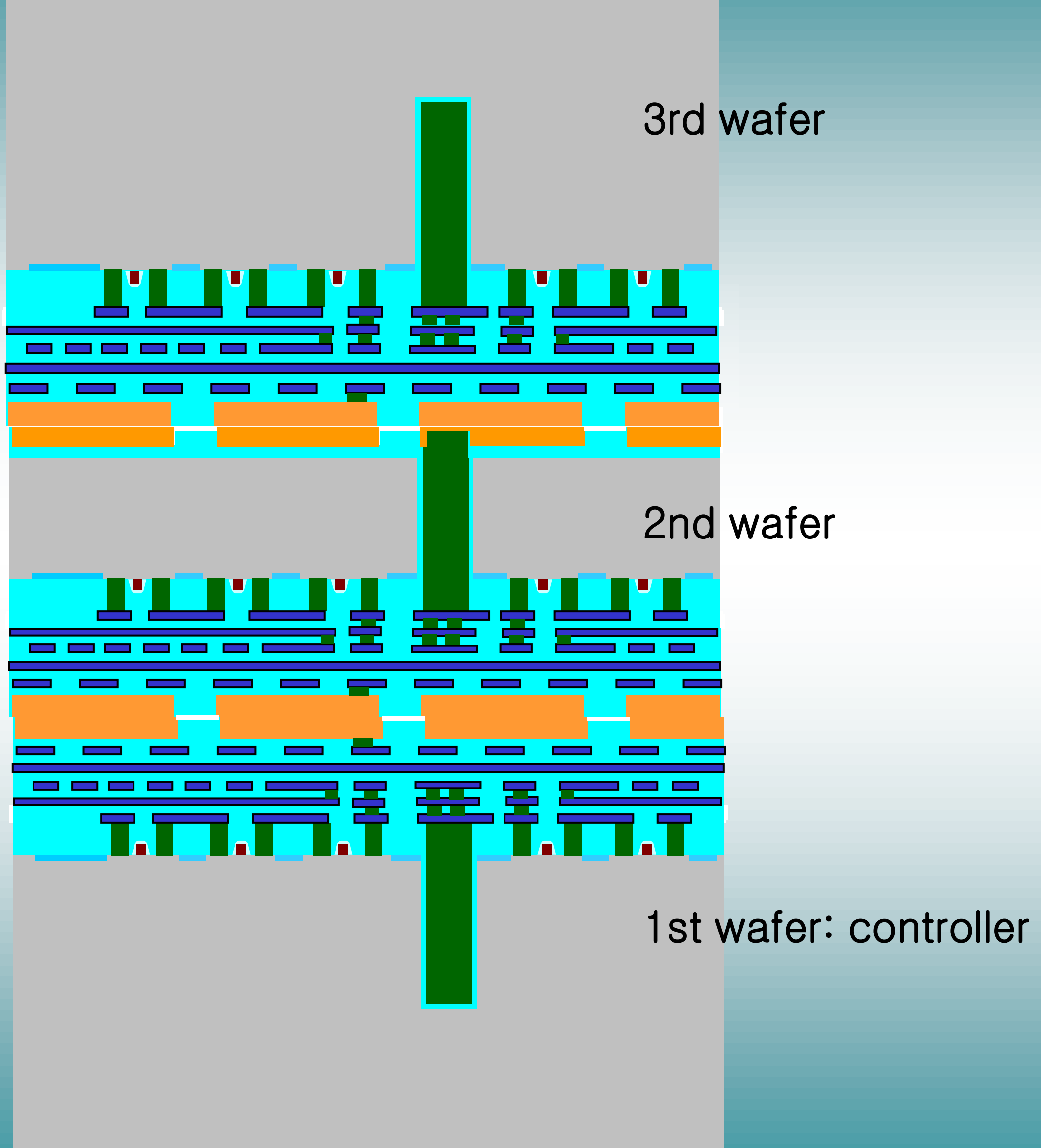


High Precision Alignment

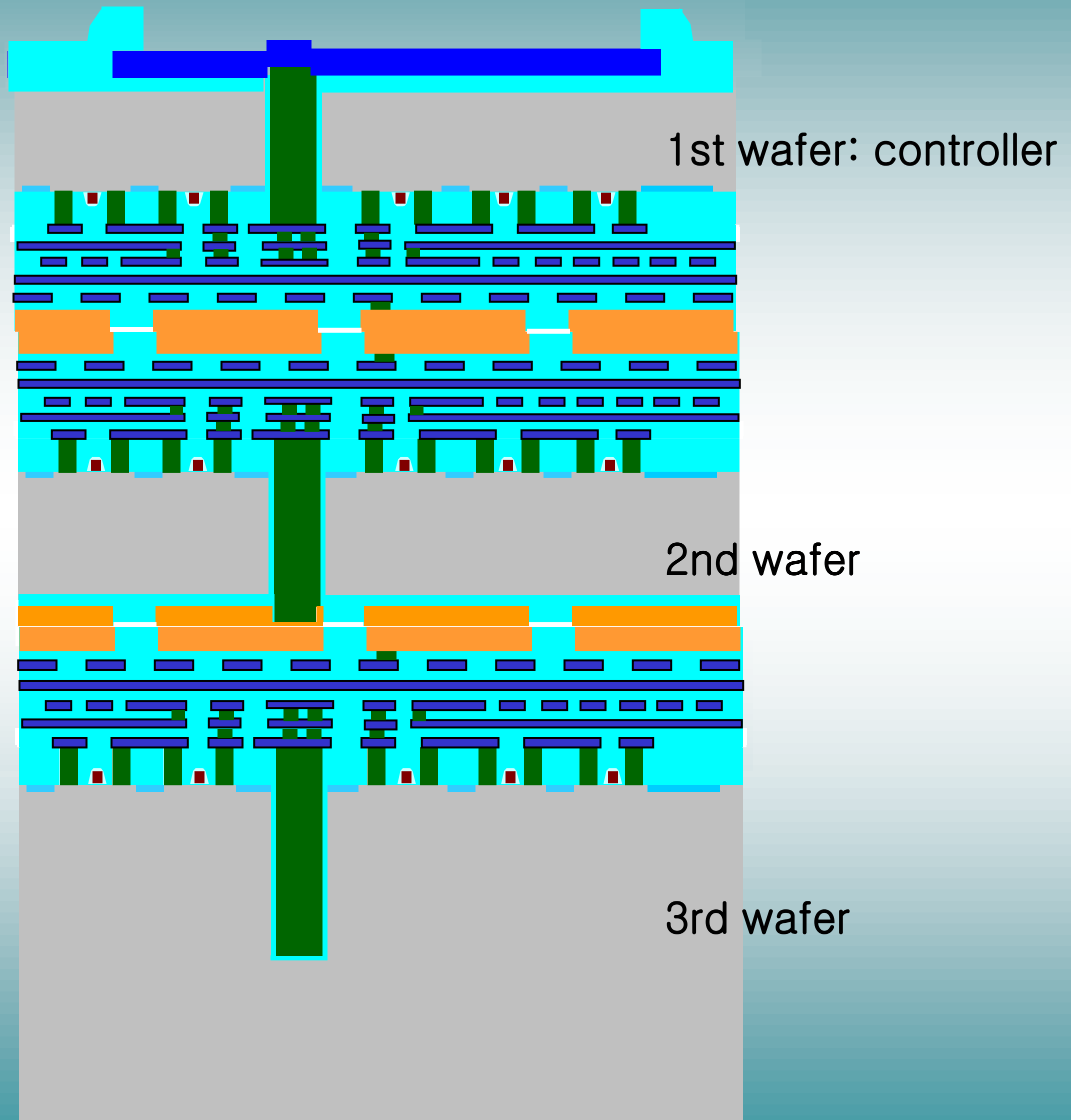
Misalign=0.3um



Then, Stack a Third Wafer:

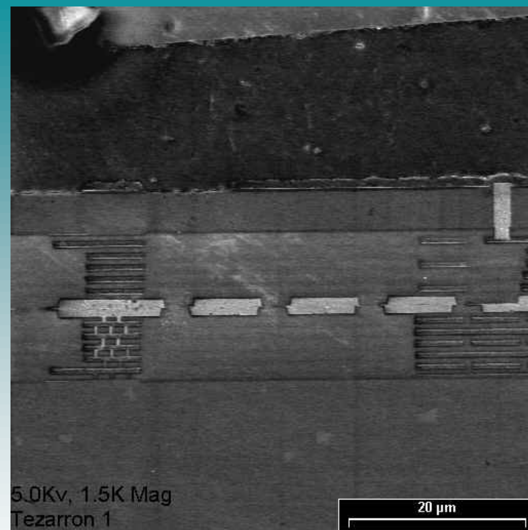


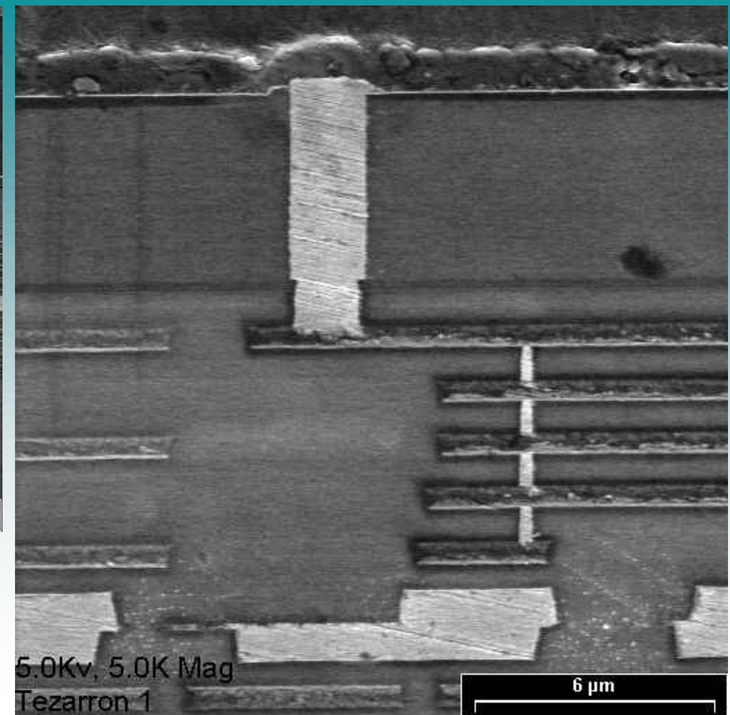
Finally, Flip, Thin & Pad Out:

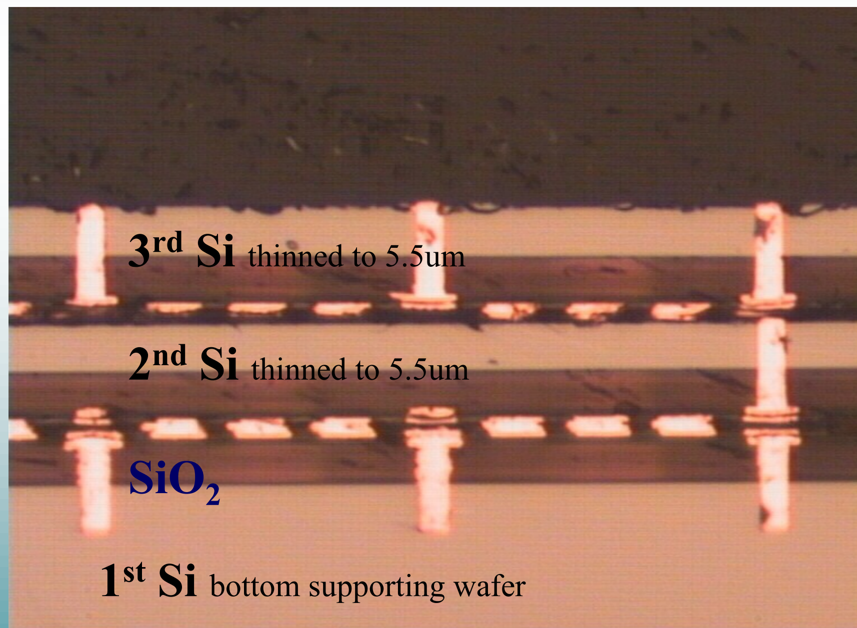


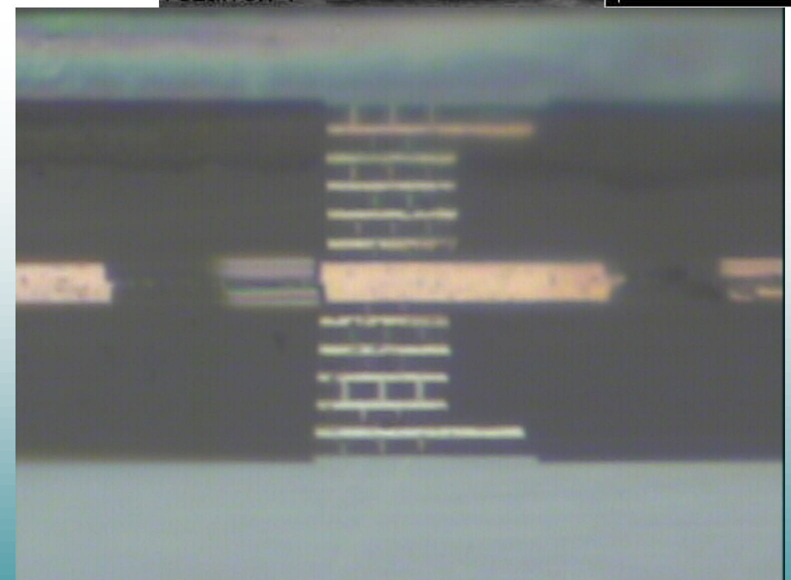
This is the completed stack!

5kV, 800X, Tezzaron
37.5 µm


5.0Kv, 1.5K Mag
Tezarron 1
20 µm


5.0Kv, 5.0K Mag
Tezarron 1
6 µm

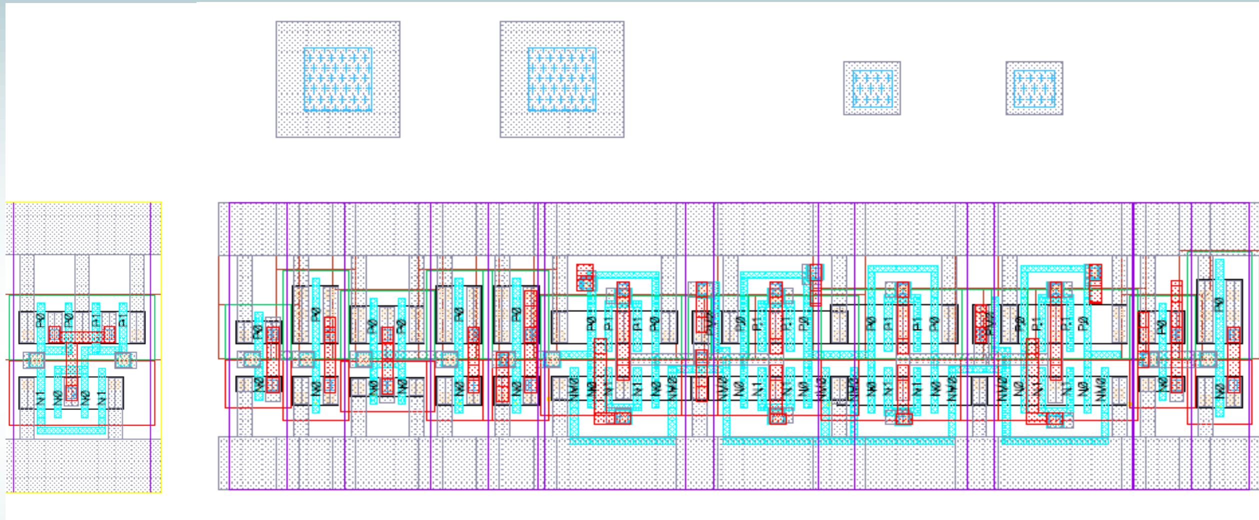

3rd Si thinned to 5.5um
2nd Si thinned to 5.5um
SiO2
1st Si bottom supporting wafer



3D Interconnect Characteristics

	SuperContact™ I 200mm Via First, FEOL	SuperContact™ II 300mm Via First, FEOL	SuperContact™ III 200mm Via First, FEOL	SuperContact™ 4 200mm Via First, FEOL	Bond Points
Size L X W X D Material	1.2 μ X 1.2 μ X 6.0μ W in Bulk	1.6 μ X 1.6 μ X 10.0μ W in Bulk	0.85 μ X 0.85 μ X 10μ W in Bulk	0.40 μ X 0.40 μ X 2μ W in SOI	1.7 μ X 1.7 μ Cu
Minimum Pitch	<2.5 μ	<3.2 μ	1.75 μ	0.8 μ	2.4 μ (1.1 μ)
Feedthrough Capacitance	2-3fF	6fF	3fF	0.2fF	<<
Series Resistance	<1.5 Ω	<1.8 Ω	<3 Ω	<1.5 Ω	<

Relative TSV Size



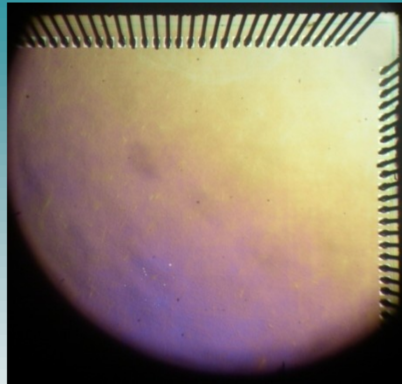
Pitch and Interconnect

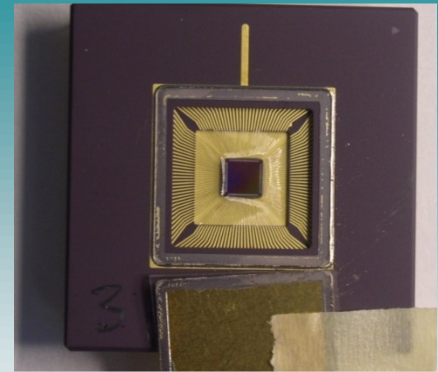
- SuperContact™ is $500f^2$ (including spacing)
- Face to face is $350f^2$ (including spacing)
- Chip on wafer I/O pitch is $35{,}000f^2$
- Standard cell gate is 200 to $1000f^2$
  - 3 connections
- Standard cell flip-flop is $5000f^2$
  - 5 connections
- 16 bit sync-counter is $125{,}000f^2$
  - 20 connections
- Opamp is $300{,}000f^2$
  - 4 connections

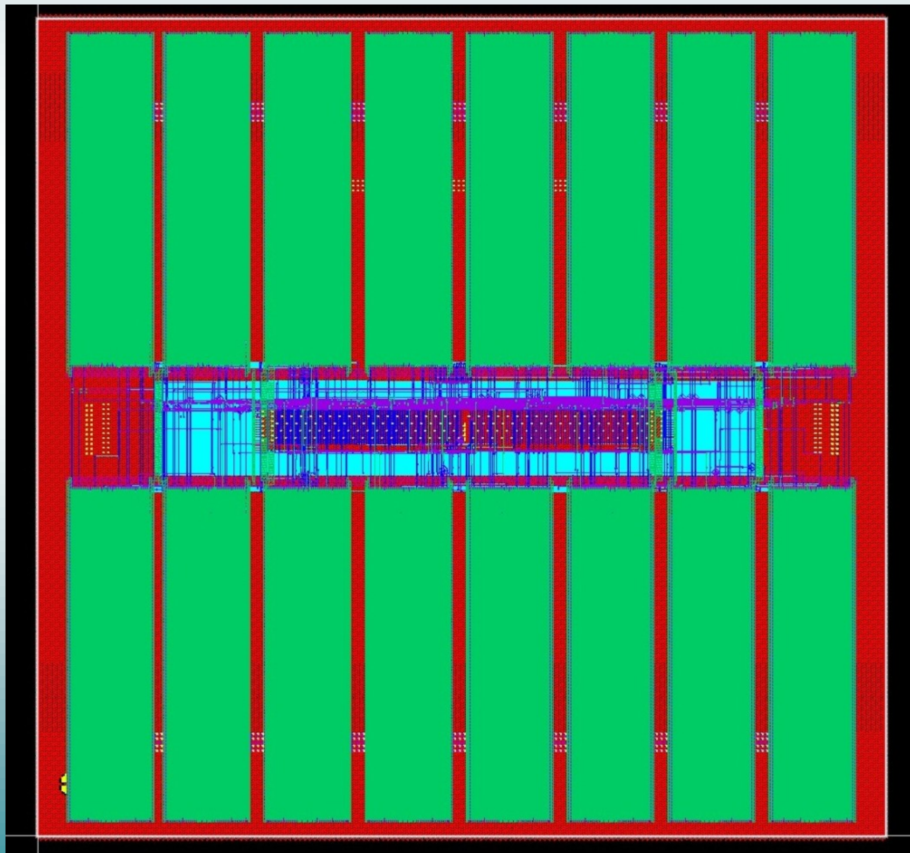
f^2 is minimum feature squared

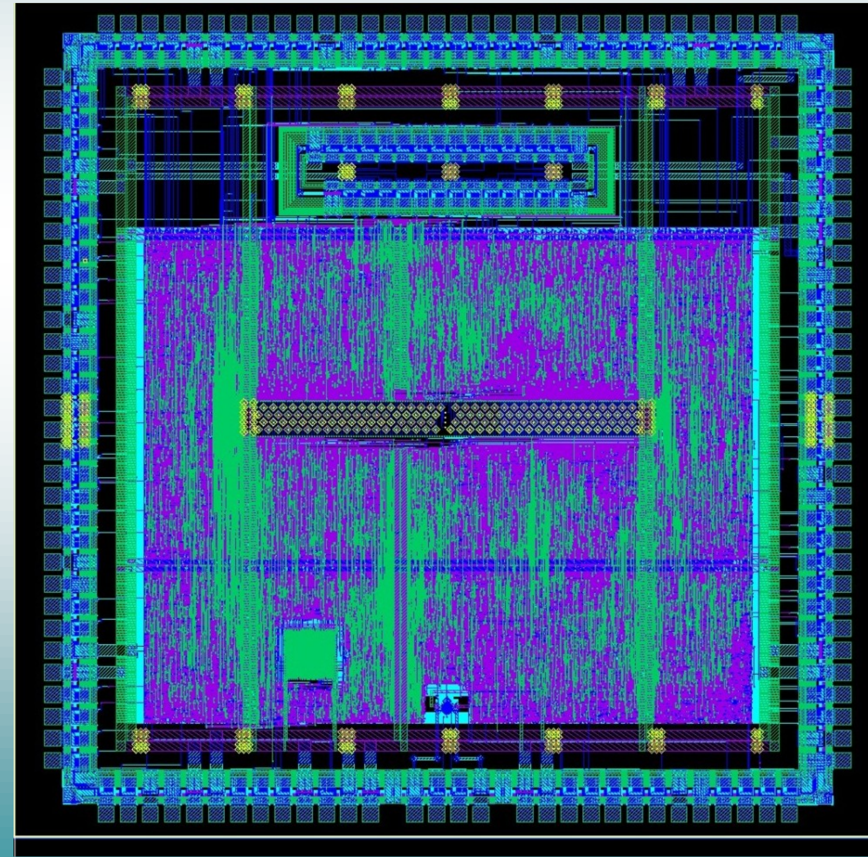
R8051/Memory

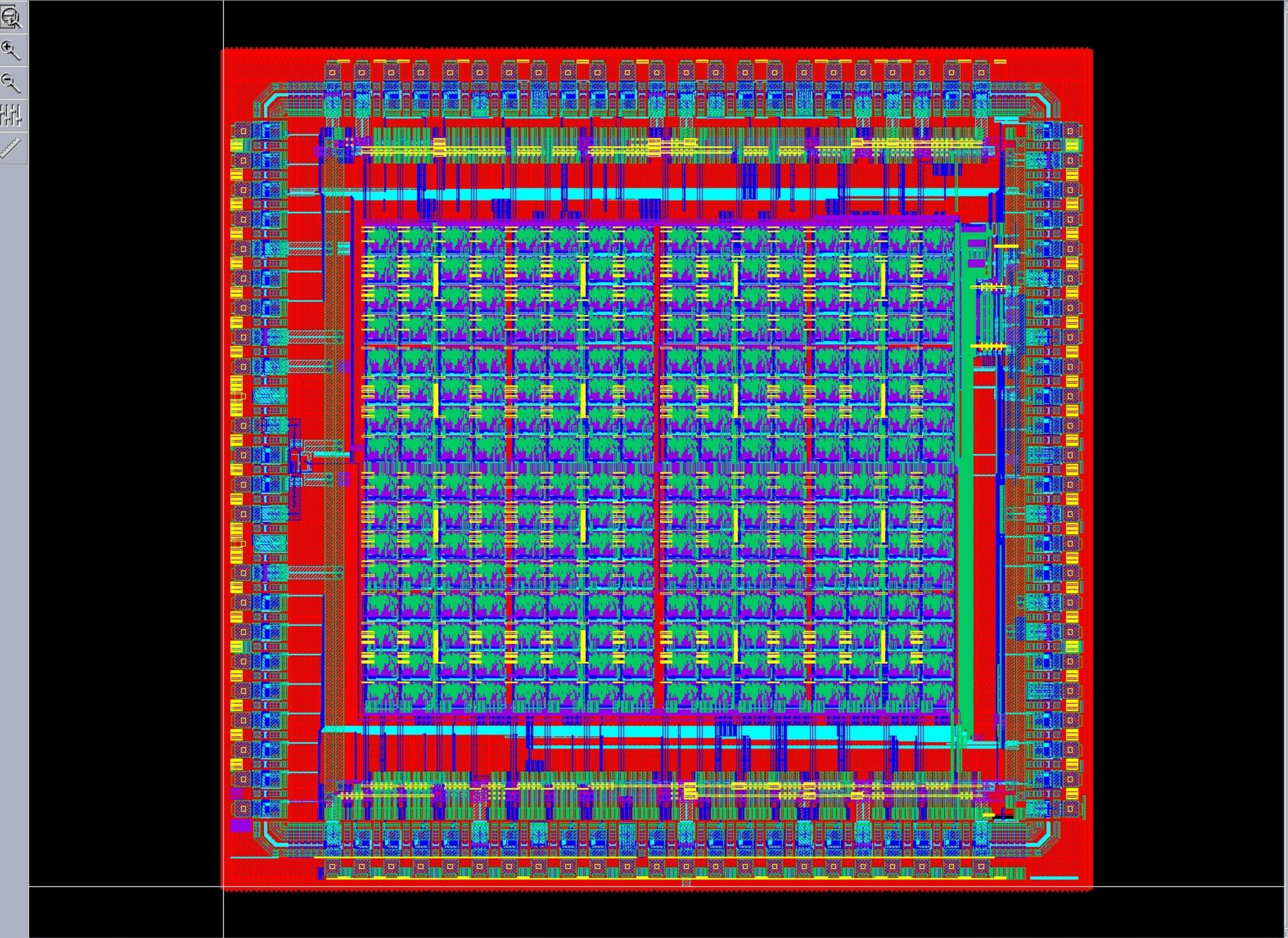
5X Performance
$1/10^{th}$ Power



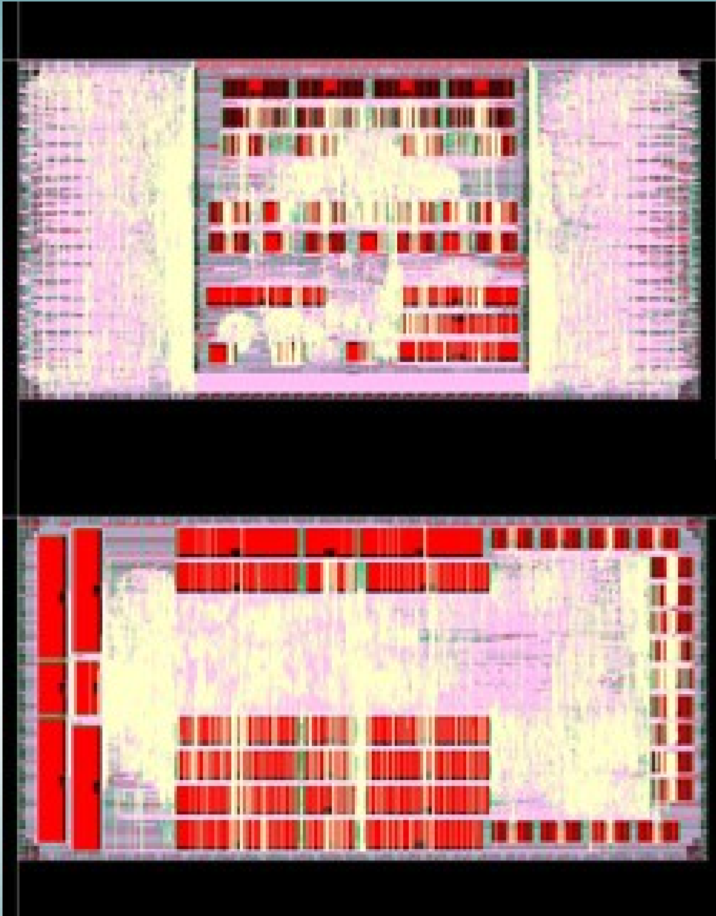


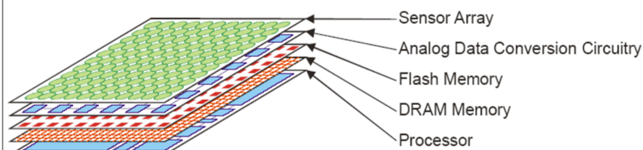


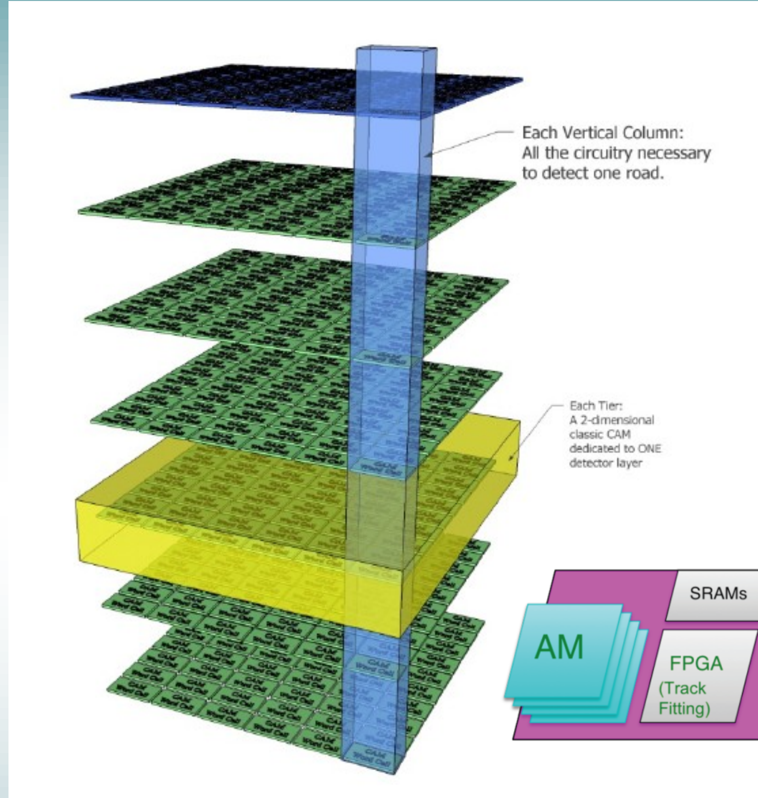


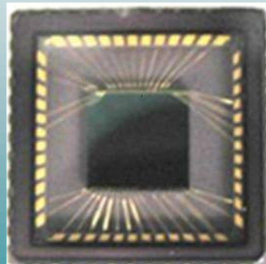

X: 3755.305
Y: 3622.500
(F) Select: 0
dX:
dY:
Dist:
Cmd:
Tools Design Window Create Edit Verify Connectivity Options Route Calibre
Help
mouse L: mouseSingleSelectPt
M: mousePopUp()
R: hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9)

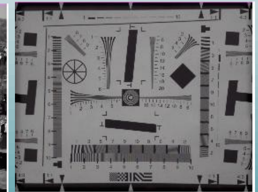
New Apps – New Architectures



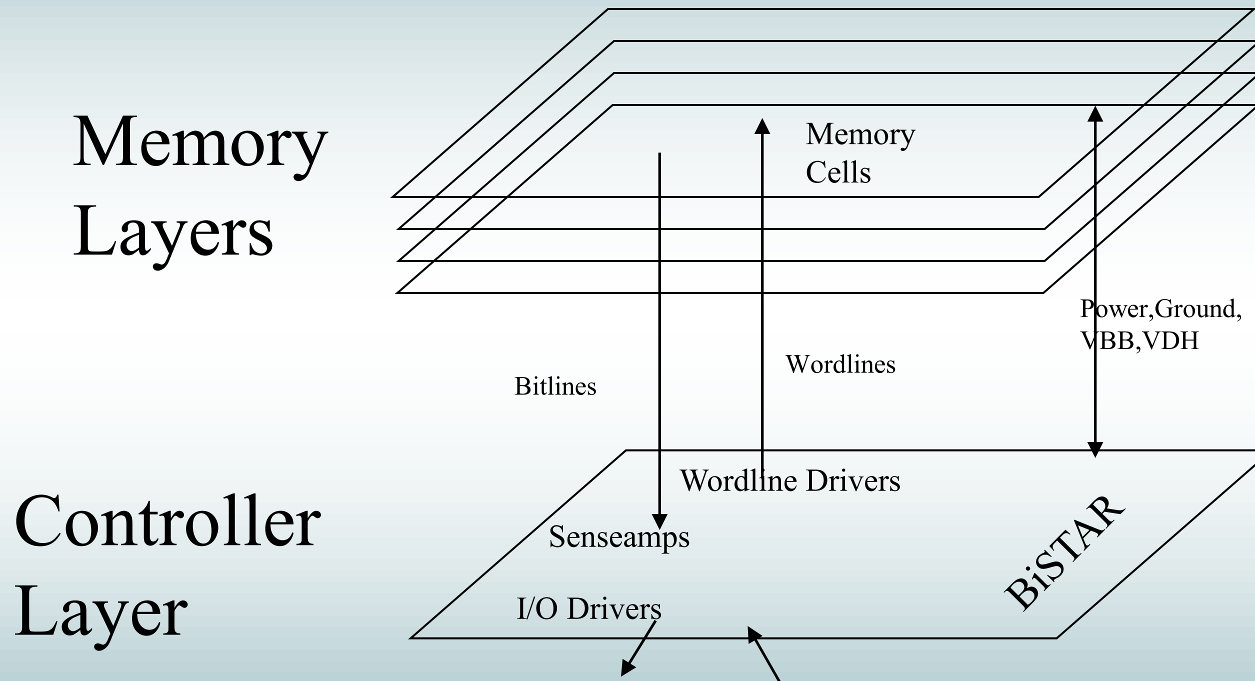








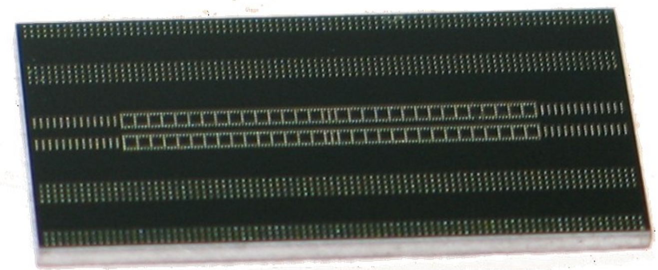
“Dis-Integrated” 3D Memory



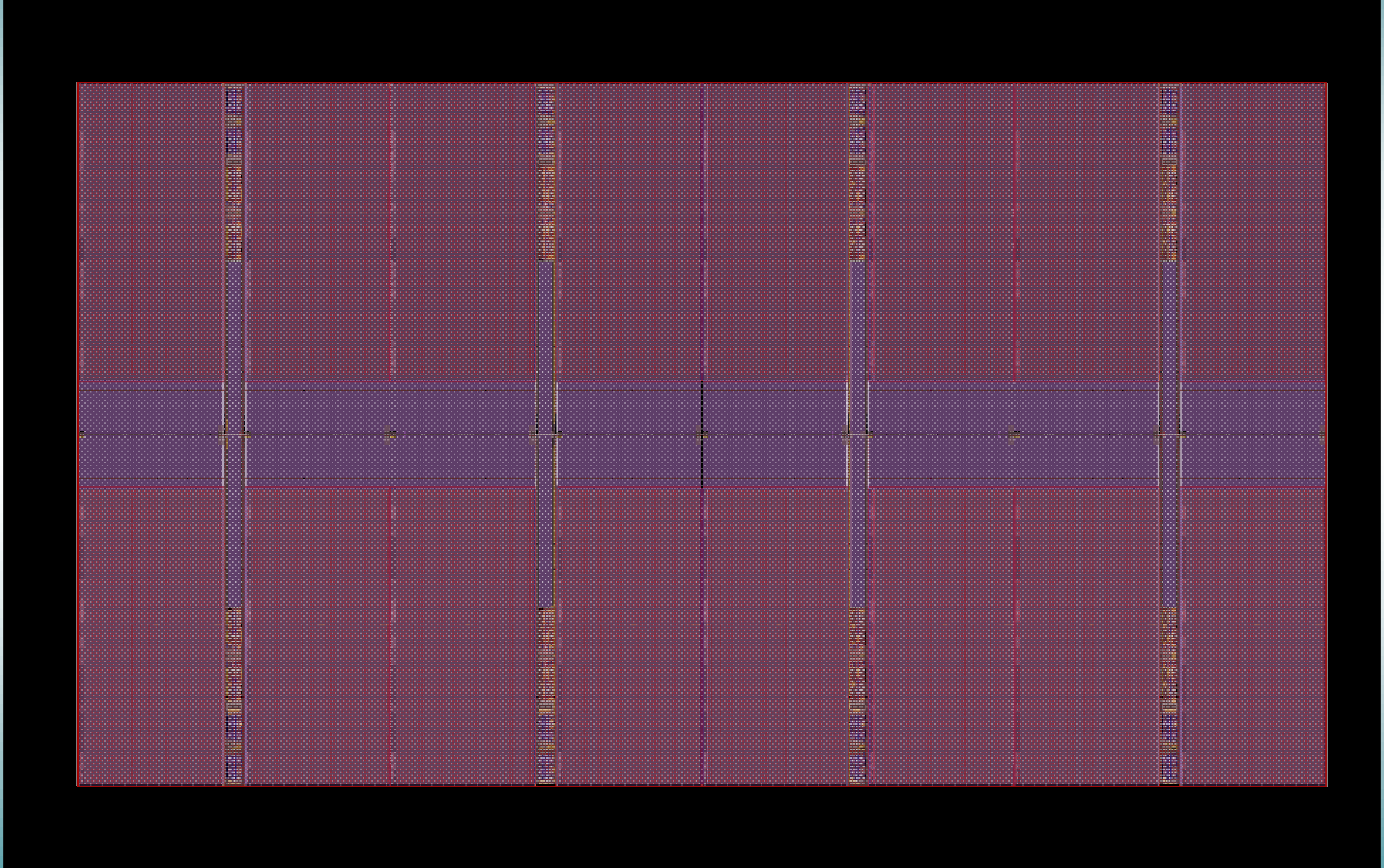
Octopus DRAM

- 1-4Gb
- 16 Ports x 128bits (each way)
- @1GHz
  - CWL=0 CRL=2 SDR format
  - 7ns closed page access to first data (aligned)
  - <20ns full cycle memory time
  - 288GB/s data transfer rate
- Max clk=1.6GHz
- Internally ECC protected, Dynamic self-repair, Post attach repair
- 115C die full function operating temperature
- JTAG/Mailbox test&configuration

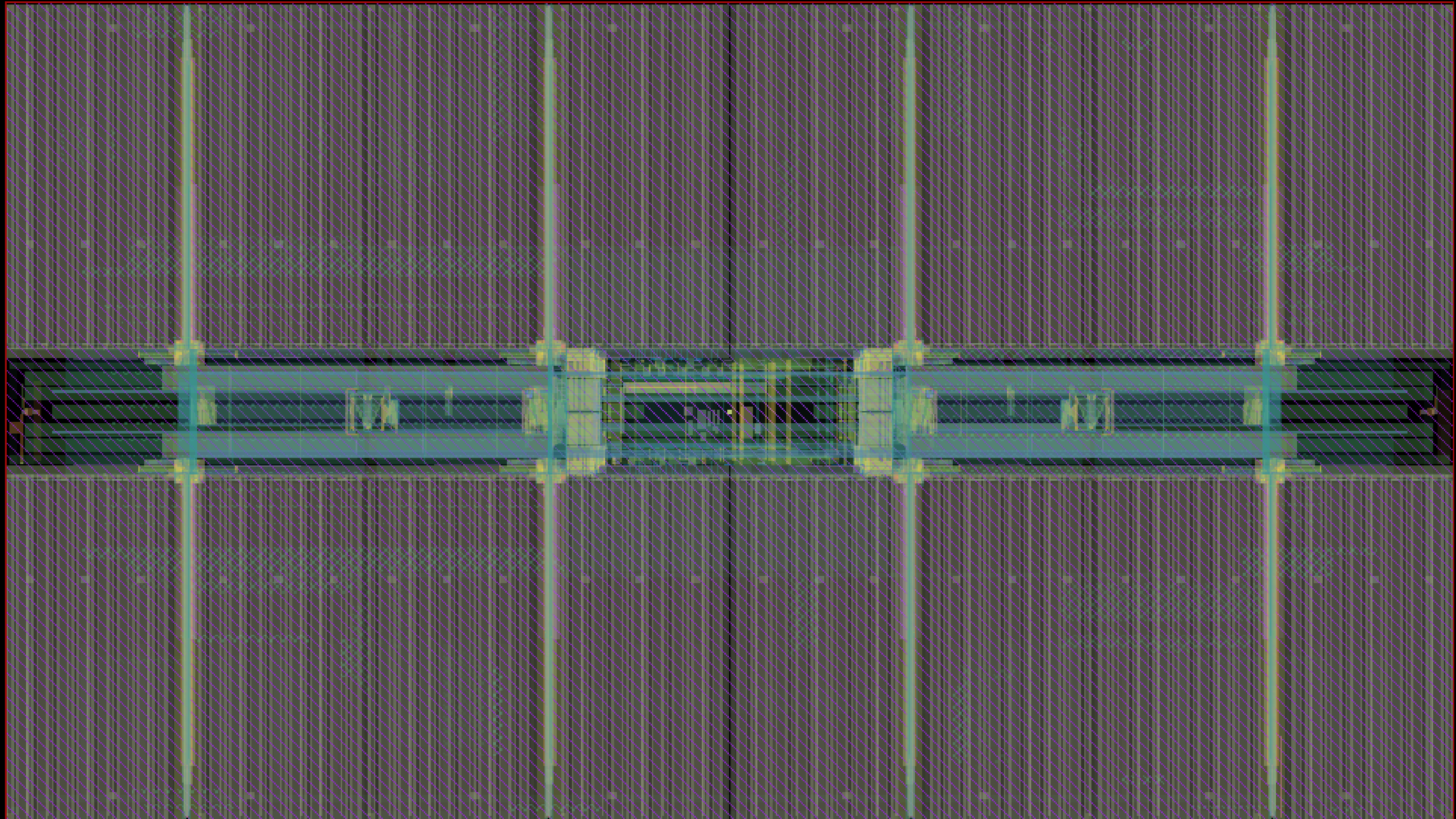
- Power -40%
- Density x4++
- Performance +300%
- Cost -50%



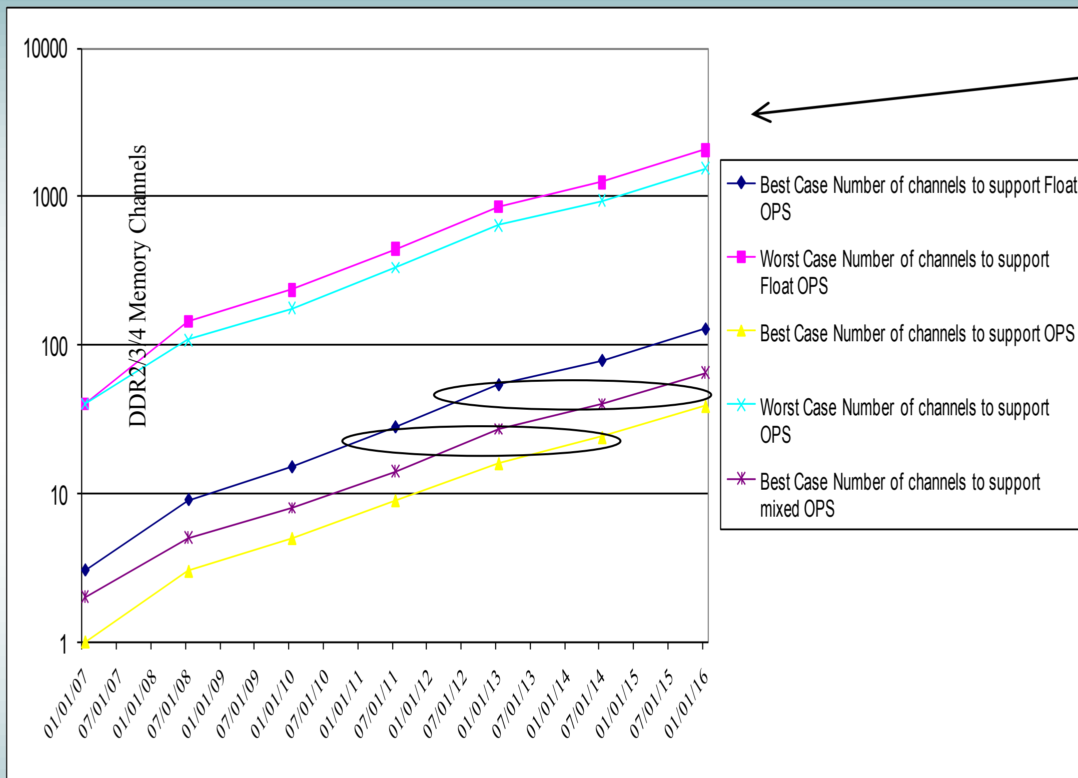
Octopus DRAM Layer



Octopus Controller



The Industry Issue



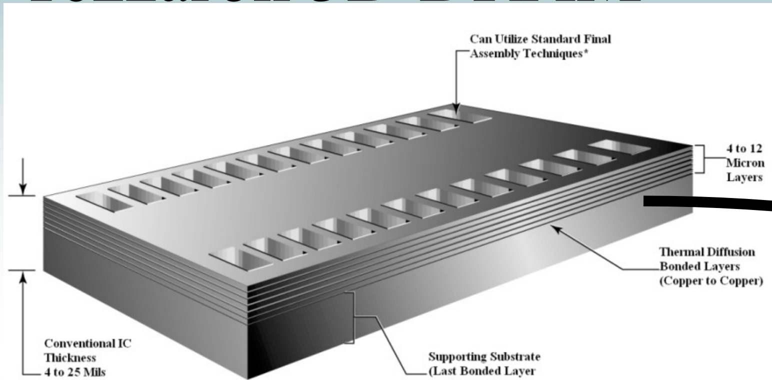
- To continue to increase CPU performance, exponential bandwidth growth required.
- More than 200 CPU cycles of delay to memory results in cycle for cycle CPU stalls.
- 16 to 64 Mbytes per thread required to hide CPU memory system accesses.
- No current extension of existing IC technology can address requirements.
- Memory I/O power is running away.

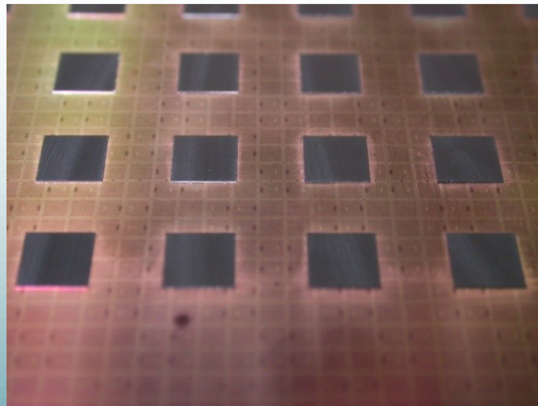
Need 50x bandwidth improvement.

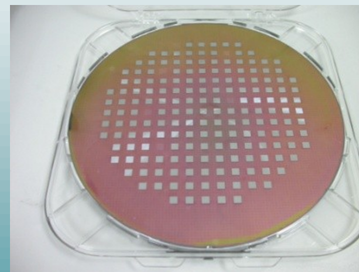
Need 10x better cost model than embedded memory.

The "Killer" App: Split-Die

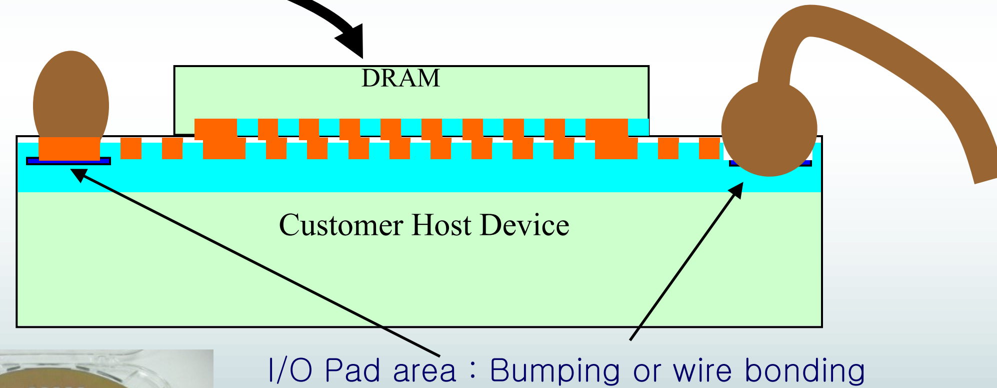
Tezzaron 3D DRAM



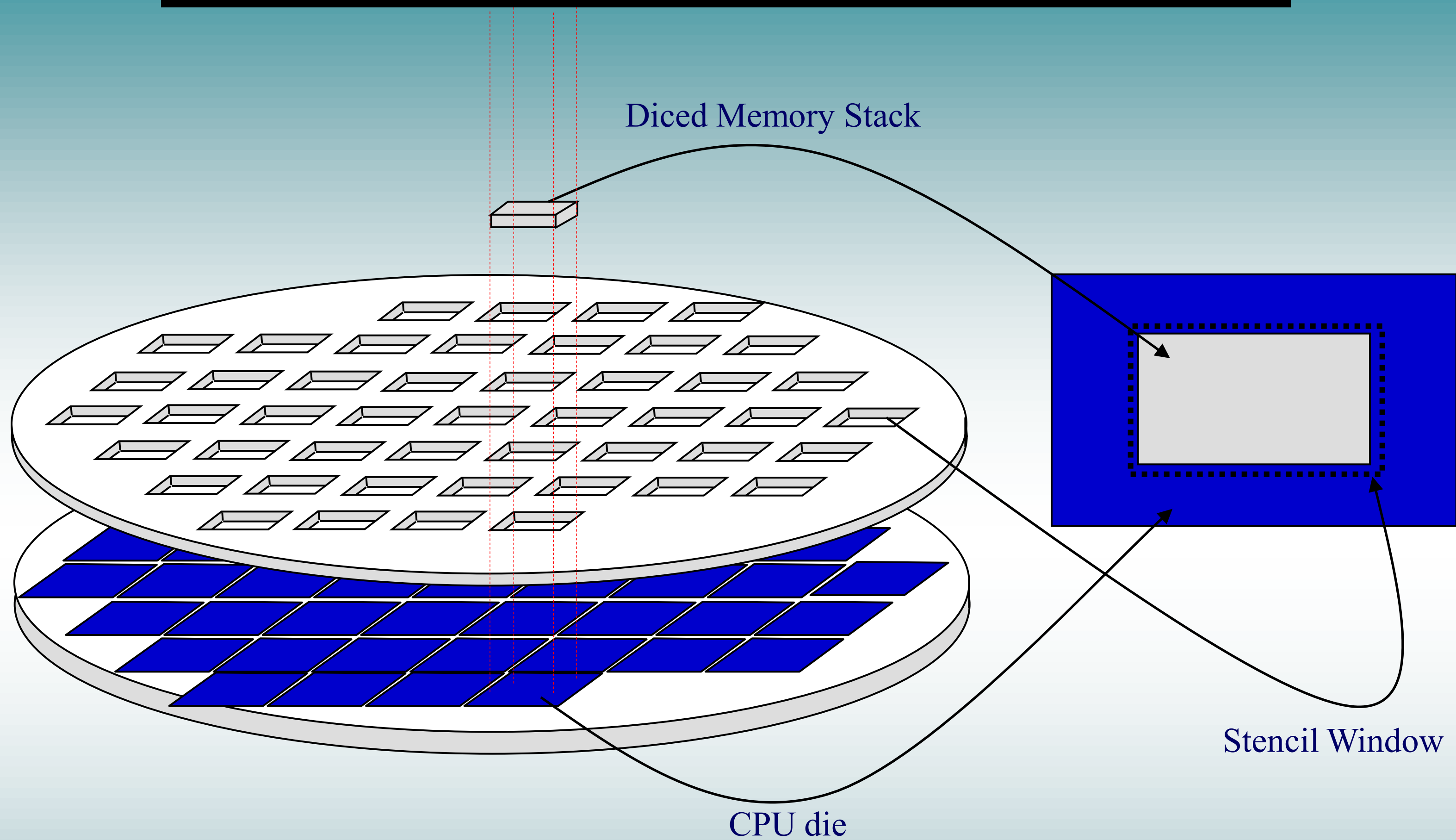




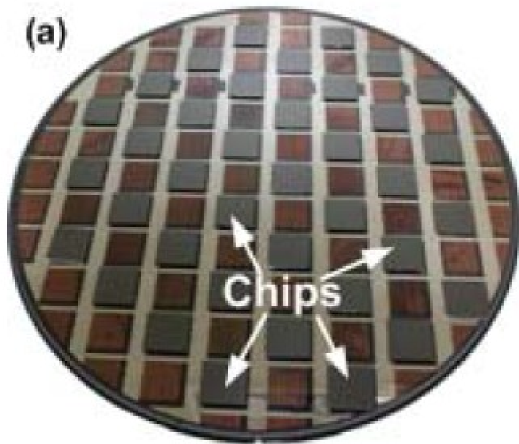
- Embedded Performance with far superior cost/density.
- 110nm DRAM node has better density than 45nm embedded DRAM.
- 1000x reduction in I/O power.

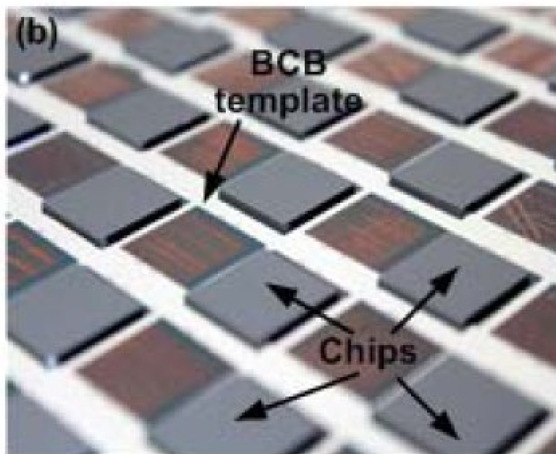


Die to Wafer With Stencils

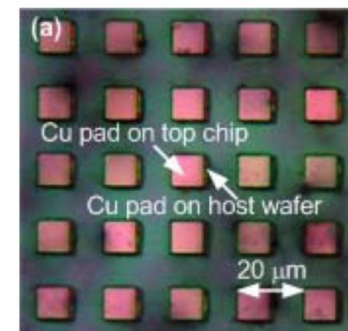


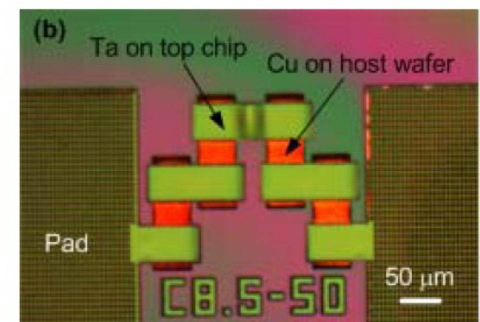
Die to Wafer With BCB Template





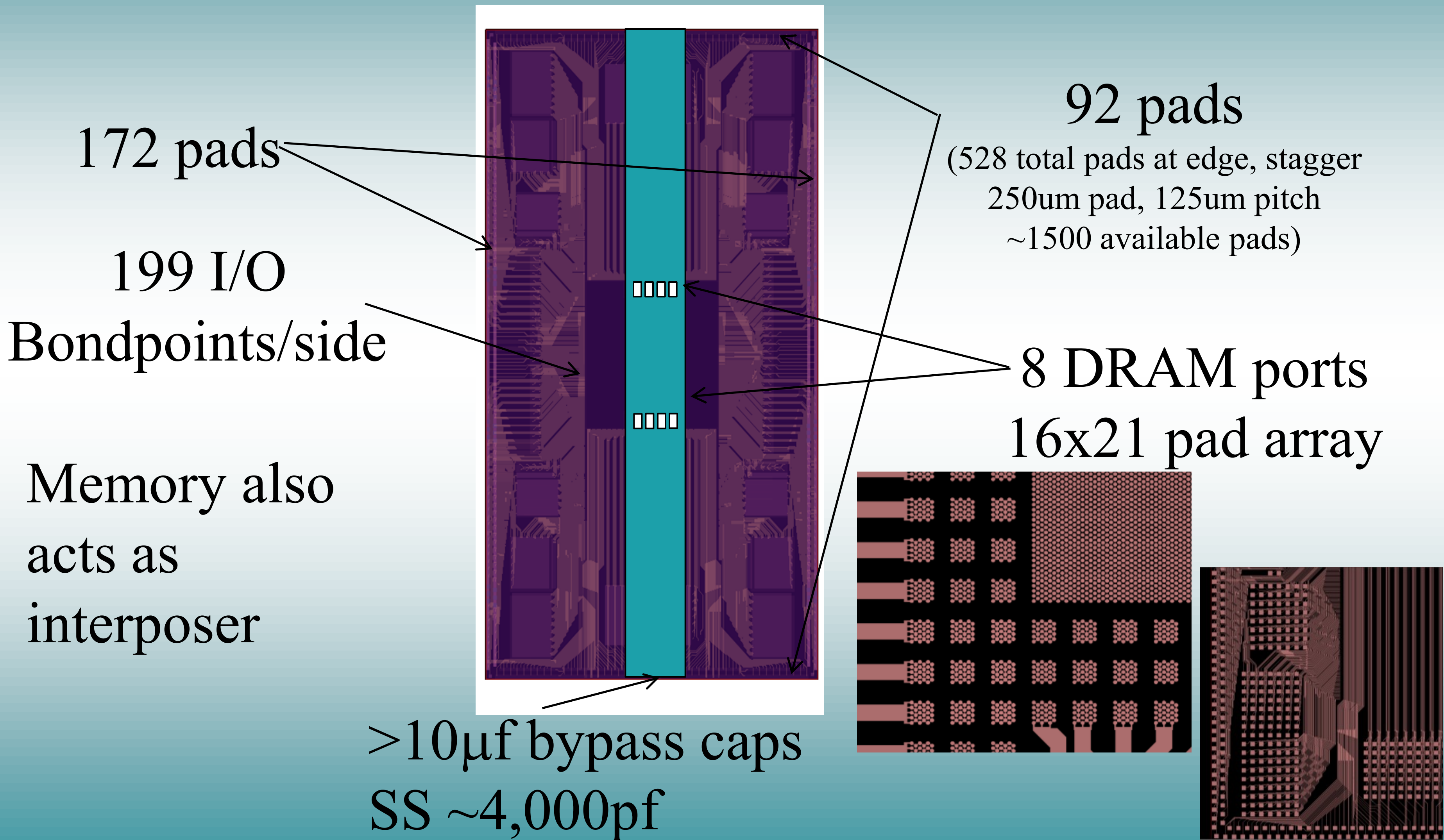
RPI Effort under Dr. James Lu



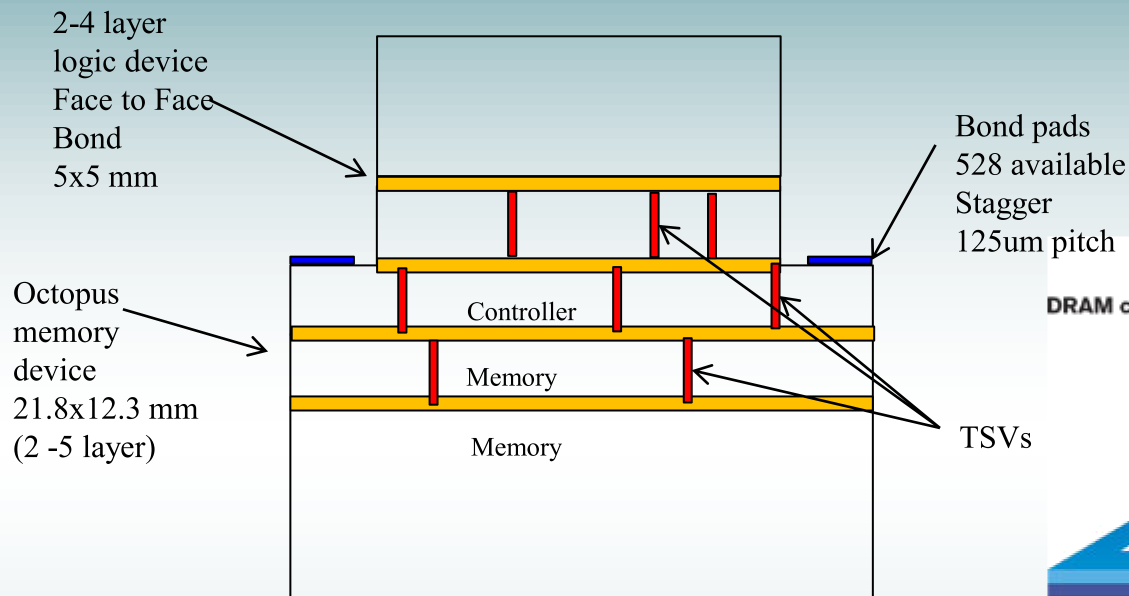


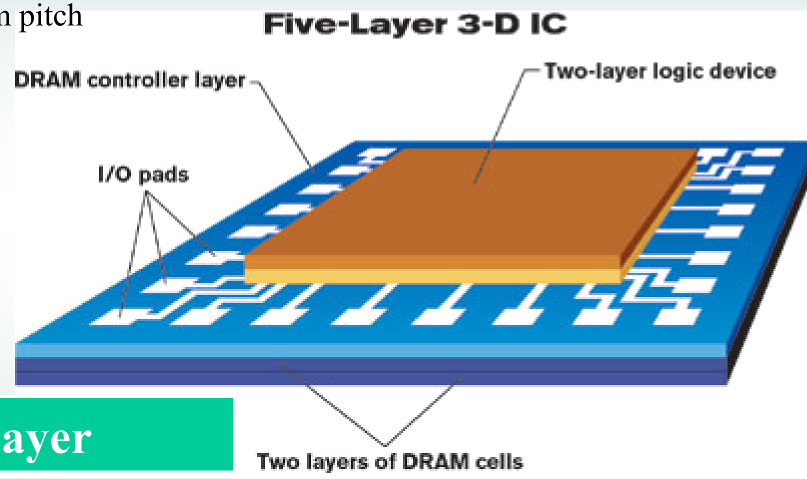
- KGD
- 2um alignment / 5um pitch limit
- Cu-Cu thermo compression bonding
- Multilayer capability

Logic on Memory



Hyper-Integration 5-9 layer stacks

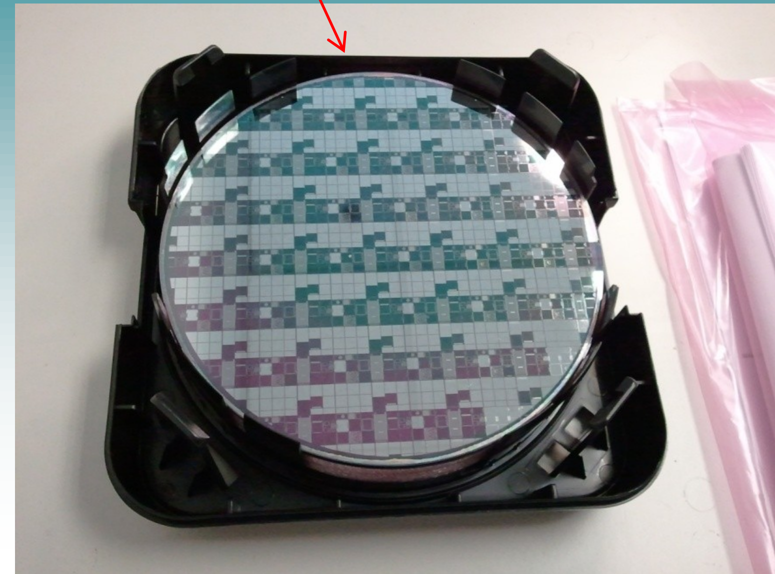


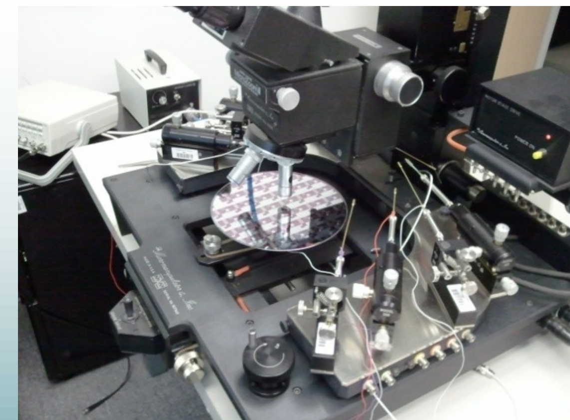


Layer	5 Layer	7 Layer	9 Layer
Poly	9	11	17
Copper Wire	21 (25)	32 (38)	34 (42)
Al/W Wire	7	7	13
Trans. Count	3B	3.1B	5.5B

Challenges

23 customer designs.

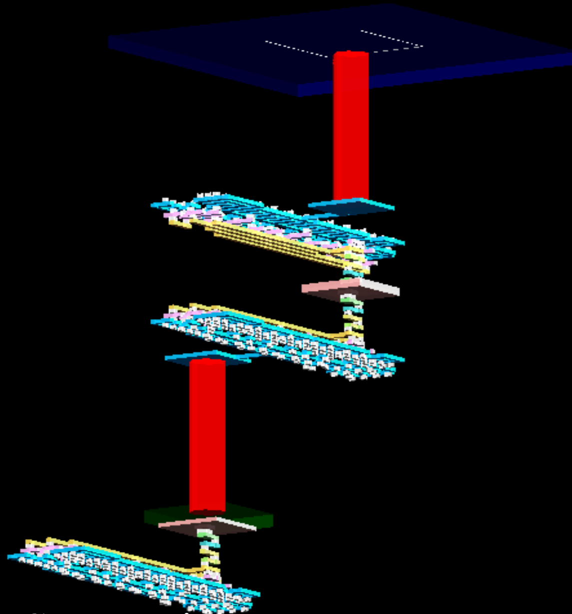


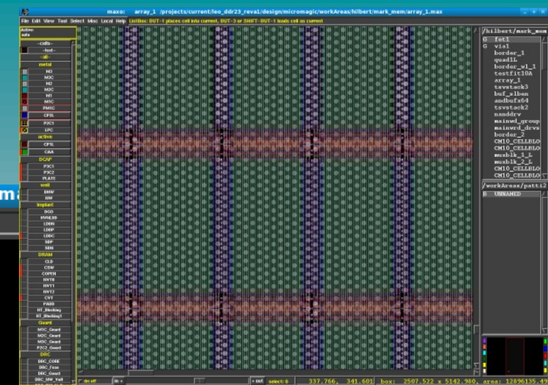


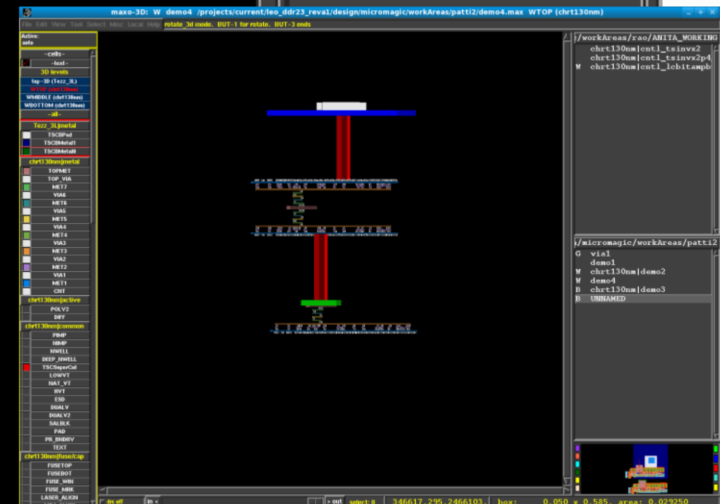
- Tools
  - Partitioning tools
  - 3D P&R
- Access
- Testing
  - IEEE 1500
  - IEEE 1149
- Standards
  - Die level
    - JEDEC JC-11 Wide bus memory
  - Foundry interface

MAX-3D by Micro Magic, Inc.
Fully functional 3D layout editor.

- Independent tech files for each tier.
- Saves GDSII as flipped or rotated.
- Custom output streams for 3D DRC / LVS.

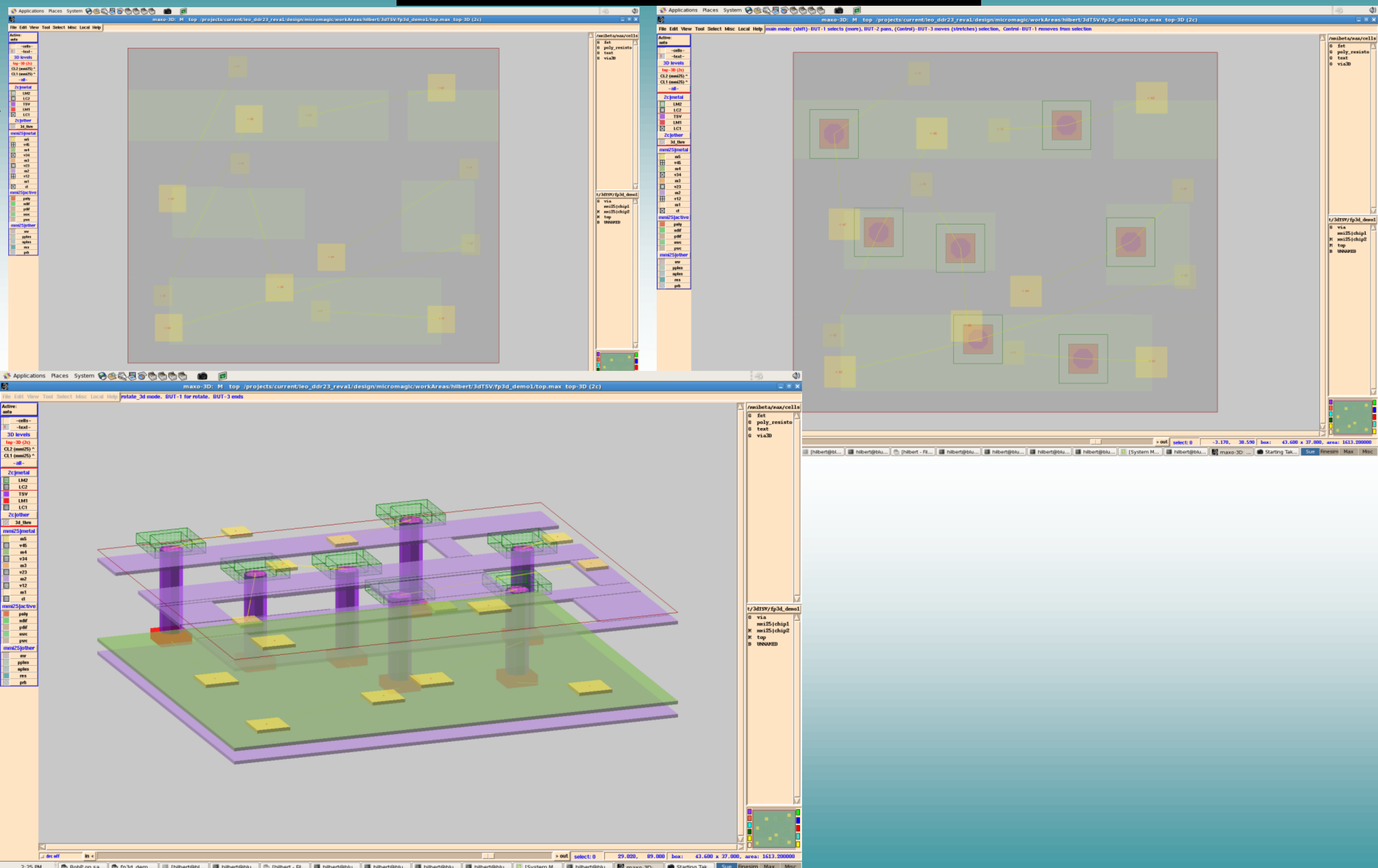






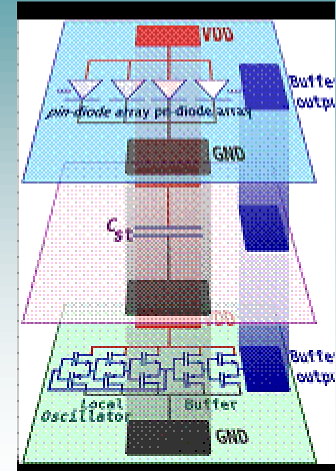
DRC, LVS, Transistor synthesis, Crossprobing.
Multiple tapeouts,
0.35um-45nm
>20GB, ~10B devices

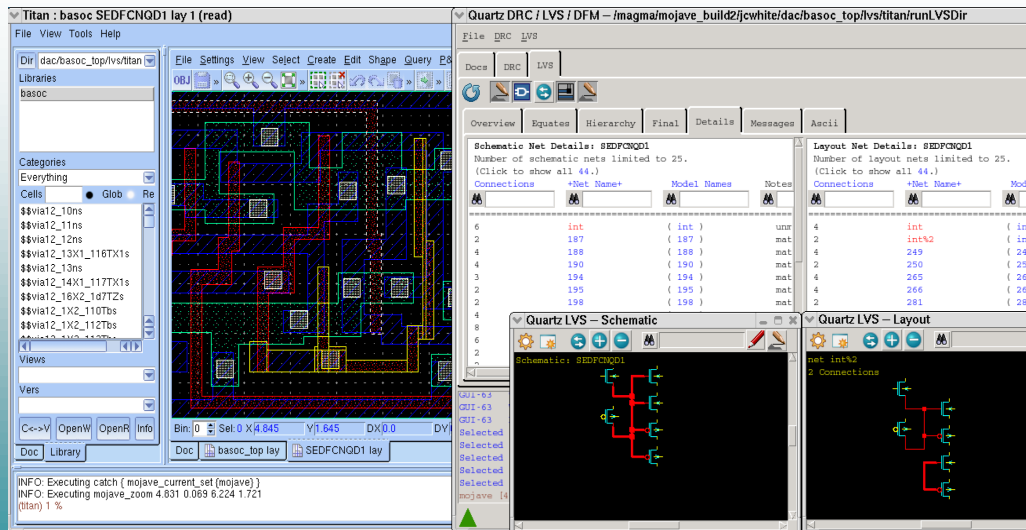
3D Place & Route



3D LVS using QuartzLVS from Magma

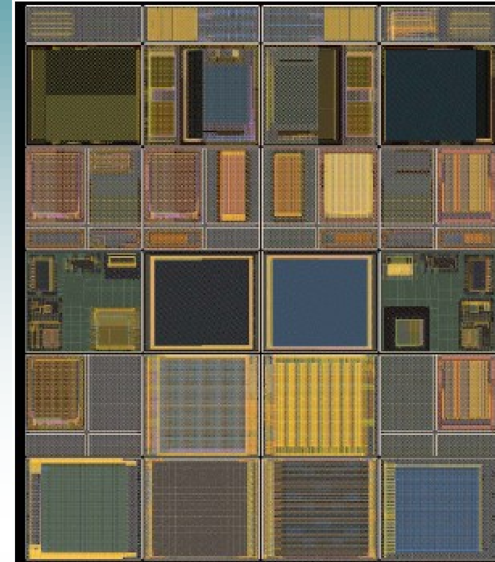
- Key features
  - LVS each of the 2D designs as well as the 3D interconnections between them in a single run
  - Driven by a 3D "tech file" that specifies the number and order of layers, interconnect material, etc
  - TSV aware LVS extraction
  - Full debug environment to analyze any LVS mismatch





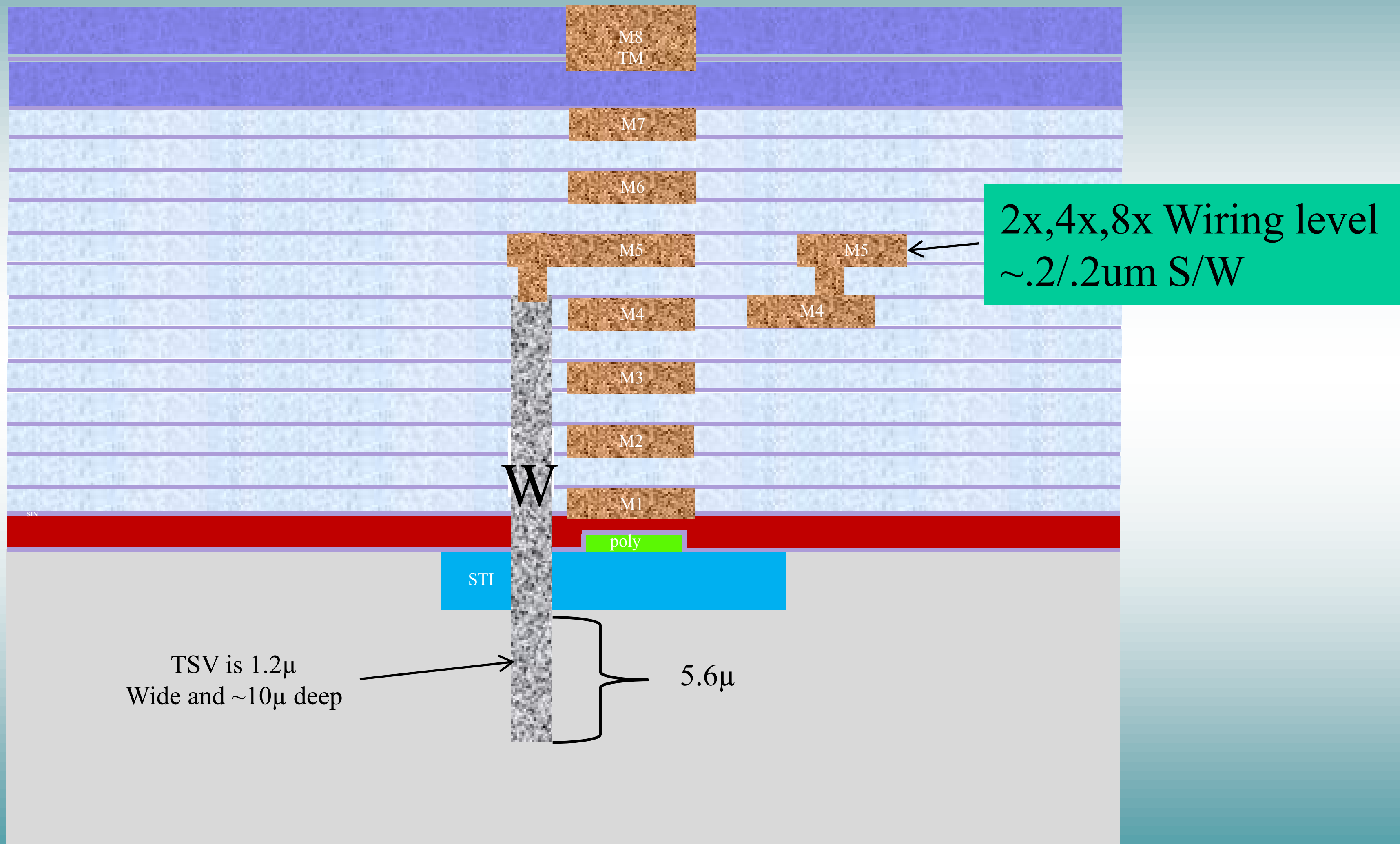

```
# 3D LVS Tech file
WAFER: 1
   LAYOUT TOP BLOCK: lvslayer1_1
   SCHEMATIC TOP BLOCK: lvslayer1
   GDSII FILE: lvslayer1_1.gds
   SCHEMATIC NETLIST: lvslayer1.sp
   INTERFACE UP METAL: 1;0
   INTERFACE UP TEXT: 1;101
...
INTERFACE:
   LAYOUT TOP BLOCK: lvstop
   SCHEMATIC TOP BLOCK: lvstop
   GDSII FILE: lvstop_ALL.gds
   SCHEMATIC NETLIST: lvstop.sp
   BOND OUT METAL: 5;0
   BOND OUT TEXT: 5;101
```

3D MPW



- Complete 3D PDK 7th Release
  - GF 130nm
  - Calibre, Synopsis, Hspice, Cadence
  - MicroMagic 3D physical editor
  - Magma 3D DRC/LVS
  - Artisan standard cell libraries
  - Release 8 up coming
- MOSIS, CMP, and CMC MPW support
  - July 1st MPW Tapeout
  - 90nm, 150nm SOI
  - Silicon Workbench
- >70 in process
- >400 users

Near End-of-Line



Summery

- 3D has numerous and vast opportunities!!
  - New design approaches
  - New ways of thinking
  - New tools
  - Poised for explosive growth

Sensors

Computing

MEMS

Communications