3D IC for Real Chips

Bob Patti, CTO

rpatti@tezzaron.com
Why We Scale?

What can 3D do for us?

Advantages

Speed  Power  Cost  Size

>180nm  130nm  90nm  65nm  45nm  28nm  22nm  16nm
How Real is 3D???

Samsung
16Gb NAND flash (2Gx8 chips), Wide Bus DRAM

Micron
Wide Bus DRAM

Intel
CPU + memory

OKI
CMOS Sensor

Xilinx
4 die 65nm interposer

Raytheon/Ziptronix
PIN Detector Device

IBM
RF Silicon Circuit Board / TSV
Logic & Analog

Toshiba
3D NAND
Span of 3D Integration

Packaging

3D-ICs
100-1,000,000/sqmm
1000-10M Interconnects/device

Peripheral I/O
- Flash, DRAM
- CMOS Sensors

1s/sqmm

Transistor to Transistor
- Ultimate goal

100,000,000s/sqmm

Wafer Fab

IBM/Samsung

IBM
A Closer Look at Wafer-Level Stacking

- **Dielectric (SiO₂/SiN)**
- **Gate Poly**
- **STI (Shallow Trench Isolation)**
- **W (Tungsten contact & via)**
- **Al (M1 – M5)**
- **Cu (M6, Top Metal)**

“Super-Contact”
Next, Stack a Second Wafer & Thin:
Stacking Process Sequential Picture

Two wafer Align & Bond → Course Grinded → Fine Grinded

→ After CMP → Si Recessed

High Precision Alignment
Misalign=0.3um

Top wafer
Bottom wafer
Then, Stack a Third Wafer:

1st wafer: controller

2nd wafer

3rd wafer
Finally, Flip, Thin & Pad Out:

This is the completed stack!
3rd Si thinned to 5.5um

2nd Si thinned to 5.5um

SiO₂

1st Si bottom supporting wafer

5KV, 800X, Tezzaron

5KV, 1.5K Mag
Tezzaron 1

5KV, 5K Mag
Tezzaron 1
## 3D Interconnect Characteristics

<table>
<thead>
<tr>
<th></th>
<th>SuperContact™ I 200mm Via First, FEOL</th>
<th>SuperContact™ II 300mm Via First, FEOL</th>
<th>SuperContact™ III 200mm Via First, FEOL</th>
<th>SuperContact™ IV 200mm Via First, FEOL</th>
<th>Bond Points</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Size</strong></td>
<td>1.2 µ X 1.2 µ X 6.0µ W in Bulk</td>
<td>1.6 µ X 1.6 µ X 10.0µ W in Bulk</td>
<td>0.85 µ X 0.85 µ X 10µ W in Bulk</td>
<td>0.40 µ X 0.40 µ X 2µ W in SOI</td>
<td>1.7 µ X 1.7 µ Cu</td>
</tr>
<tr>
<td><strong>Material</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Minimum Pitch</strong></td>
<td>&lt;2.5 µ</td>
<td>&lt;3.2 µ</td>
<td>1.75 µ</td>
<td>0.8 µ</td>
<td>2.4 µ (1.1 µ)</td>
</tr>
<tr>
<td><strong>Feedthrough</strong></td>
<td>2-3fF</td>
<td>6fF</td>
<td>3fF</td>
<td>0.2fF</td>
<td>&lt;&lt;</td>
</tr>
<tr>
<td><strong>Series Resistance</strong></td>
<td>&lt;1.5 Ω</td>
<td>&lt;1.8 Ω</td>
<td>&lt;3 Ω</td>
<td>&lt;1.5 Ω</td>
<td>&lt;</td>
</tr>
</tbody>
</table>
Relative TSV Size
Pitch and Interconnect

- SuperContact™ is 500f² (including spacing)
- Face to face is 350f² (including spacing)
- Chip on wafer I/O pitch is 35,000f²
- Standard cell gate is 200 to 1000f²
  - 3 connections
- Standard cell flip-flop is 5000f²
  - 5 connections
- 16 bit sync-counter is 125,000f²
  - 20 connections
- Opamp is 300,000f²
  - 4 connections

f² is minimum feature squared
R8051/Memory

5X Performance
1/10th Power
New Apps – New Architectures
“Dis-Integrated” 3D Memory

Memory Layers

Controller Layer

- Memory Cells
- Bitlines
- Wordlines
- Wordline Drivers
- Senseamps
- I/O Drivers
- Power, Ground, VBB, VDH

Tezzaron Semiconductor

06/14/2011
Octopus DRAM

- 1-4Gb
- 16 Ports x 128bits (each way)
- @1GHz
  - CWL=0 CRL=2 SDR format
  - 7ns closed page access to first data (aligned)
  - <20ns full cycle memory time
  - 288GB/s data transfer rate
- Max clk=1.6GHz
- Internally ECC protected, Dynamic self-repair, Post attach repair
- 115C die full function operating temperature
- JTAG/Mailbox test & configuration

- Power -40%
- Density x4++
- Performance +300%
- Cost -50%
Octopus DRAM Layer
Octopus Controller
The Industry Issue

To continue to increase CPU performance, exponential bandwidth growth required.

More than 200 CPU cycles of delay to memory results in cycle for cycle CPU stalls.

16 to 64 Mbytes per thread required to hide CPU memory system accesses.

No current extension of existing IC technology can address requirements.

Memory I/O power is running away.

Need 50x bandwidth improvement.
Need 10x better cost model than embedded memory.
The “Killer” App: Split-Die

- Embedded Performance with far superior cost/density.
- 110nm DRAM node has better density than 45nm embedded DRAM.
- 1000x reduction in I/O power.

Tezzaron 3D DRAM

Customer Host Device

DRAM

I/O Pad area: Bumping or wire bonding
Die to Wafer With Stencils

- Diced Memory Stack
- Stencil Window
- CPU die
Die to Wafer With BCB Template

RPI Effort under Dr. James Lu

- KGD
- 2um alignment / 5um pitch limit
- Cu-Cu thermo compression bonding
- Multilayer capability
Logic on Memory

172 pads

199 I/O Bondpoints/side

Memory also acts as interposer

>10μf bypass caps
SS ~4,000pf

92 pads
(528 total pads at edge, stagger 250um pad, 125um pitch ~1500 available pads)

8 DRAM ports
16x21 pad array

Tezzaron Semiconductor

06/14/2011
Hyper-Integration
5-9 layer stacks

2-4 layer logic device
Face to Face Bond
5x5 mm

Octopus memory device
21.8x12.3 mm (2-5 layer)

Layer | 5 Layer | 7 Layer | 9 Layer
--- | --- | --- | ---
Poly | 9 | 11 | 17
Copper Wire | 21 (25) | 32 (38) | 34 (42)
Al/W Wire | 7 | 7 | 13
Trans. Count | 3B | 3.1B | 5.5B
Challenges

• Tools
  – Partitioning tools
  – 3D P&R

• Access

• Testing
  – IEEE 1500
  – IEEE 1149

• Standards
  – Die level
    • JEDEC JC-11 Wide bus memory
  – Foundry interface

23 customer designs.
MAX-3D by Micro Magic, Inc.
Fully functional 3D layout editor.

- Independent tech files for each tier.
- Saves GDSII as flipped or rotated.
- Custom output streams for 3D DRC / LVS.

DRC, LVS, Transistor synthesis, Crossprobing. Multiple tapeouts, 0.35um-45nm >20GB, ~10B devices
3D Place & Route
3D LVS using QuartzLVS from Magma

- Key features
  - LVS each of the 2D designs as well as the 3D interconnections between them in a single run
  - Driven by a 3D “tech file” that specifies the number and order of layers, interconnect material, etc
  - TSV aware LVS extraction
  - Full debug environment to analyze any LVS mismatch

# 3D LVS Tech file

```
WAFER: 1

LAYOUT TOP BLOCK: lvslayer1_1
SCHEMATIC TOP BLOCK: lvslayer1
GDSII FILE: lvslayer1_1.gds
SCHEMATIC NETLIST: lvslayer1.sp

INTERFACE UP METAL: 1;0
INTERFACE UP TEXT: 1;101

... INTERFACE:
LAYOUT TOP BLOCK: lvstop
SCHEMATIC TOP BLOCK: lvstop
GDSII FILE: lvstop_ALL.gds
SCHEMATIC NETLIST: lvstop.sp
BOND OUT METAL: 5;0
BOND OUT TEXT: 5;101
```
3D MPW

• Complete 3D PDK 7th Release
  – GF 130nm
  – Calibre, Synopsis, Hspice, Cadence
  – MicroMagic 3D physical editor
  – Magma 3D DRC/LVS
  – Artisan standard cell libraries
  – Release 8 up coming

• MOSIS, CMP, and CMC MPW support
  – July 1st MPW Tapeout
  – 90nm, 150nm SOI
  – Silicon Workbench

• >70 in process
• >400 users
Near End-of-Line

TSV is 1.2µ Wide and ~10µ deep

2x, 4x, 8x Wiring level ~.2/.2um S/W
Summery

• 3D has numerous and vast opportunities!!
  – New design approaches
  – New ways of thinking
  – New tools
  – Poised for explosive growth

Sensors
  Computing
    MEMS
  Communications