Laboratoire d'Annecy-le-Vieux de Physique des Particules

Calorimeter for ILC

Large area MICROMEGAS chambers with embedded front-end electronics for hadron calorimetry

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on behalf of the LAPP LC Detector Group

TIPP 2011, 8 – 15 June, Chicago, USA

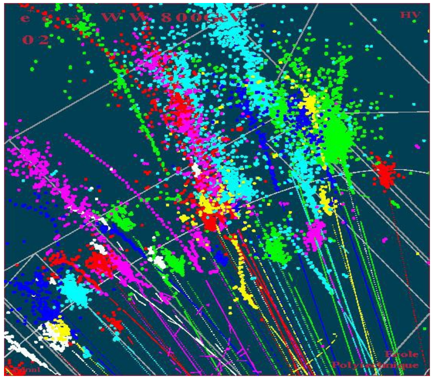
Outline

1. Introduction
2. MICROMEGAS for DHCAL
3. First large scale prototype – $1x1m^2$ chamber
   - Design, read-out electronics, test beam
4. New $1x1m^2$ chamber
   - Design improvements, new read-out electronics, X-ray test
5. Simulation activities
6. Summary and conclusions

Calorimetry at future e+e- colliders

Detectors at a future linear collider will be optimized for Particle Flow to reach an excellent jet energy resolution $\sigma E_j/E < 3\text{-}4\%$ over whole jet energy range

→ Calorimeters must have very fine lateral and longitudinal segmentation



Several technologies are under intensive R&D for hadron calorimeter:

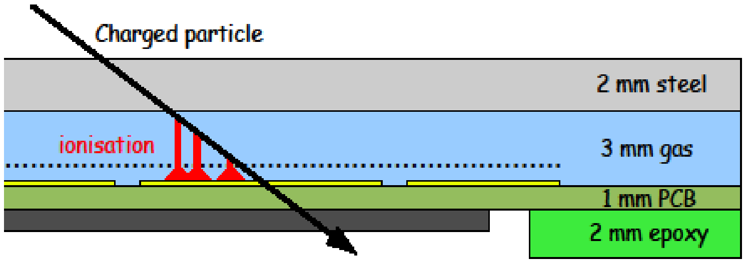
- Scintillator with analogue readout
- Gaseous detectors with digital (1 or 2-bit) readout:
  - RPC (Resistive Plate Chamber)
  - GEM (Gas Electron Multiplier)
  - MICROMEGAS (MICROmesh GAseous Structure)

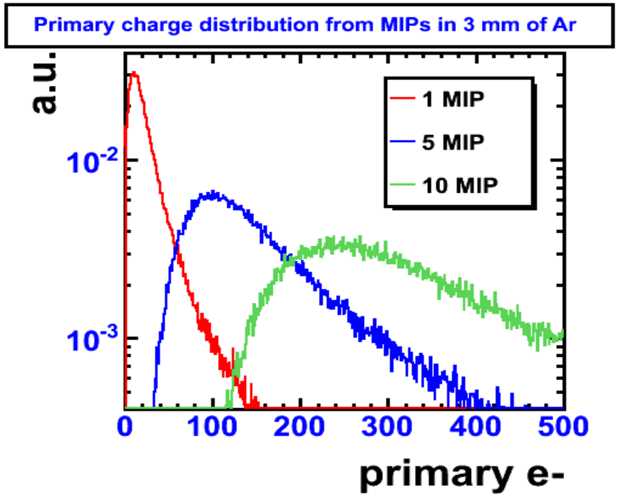
Micromegas for hadronic calorimetry

Pros

- Large area (CERN workshop, industry)
- Thin chambers (FE embedded on PCB)
- Fine lateral segmentation
- Standard gases (Ar/iso or Ar/CO_2)
- Insensitive to neutrons
- Low working voltages (< 500V)
- High rate capability (barrel & endcaps)
- High efficiency and and low hit multiplicity
- Proportional avalanche (number of MIPS/pad)

3 mm gas, 1x1 cm^2 readout pads, active thickness ~6 mm, 2 bit readout



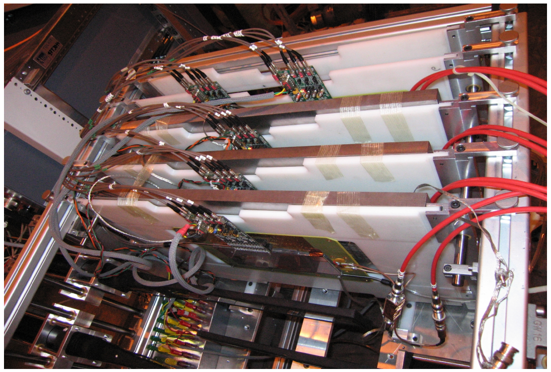


Cons

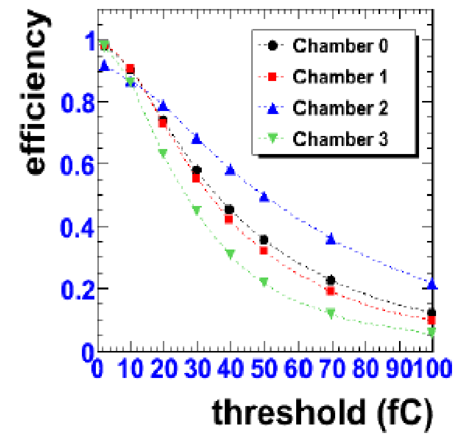
- Sparking: protections mandatory
- Small signals (25 fC for MIPs): low noise ASICs must used

Basic chamber characteristic

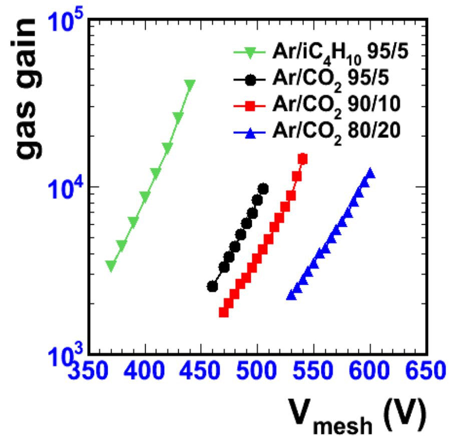
Measurements performed with small size prototypes with analogue readout



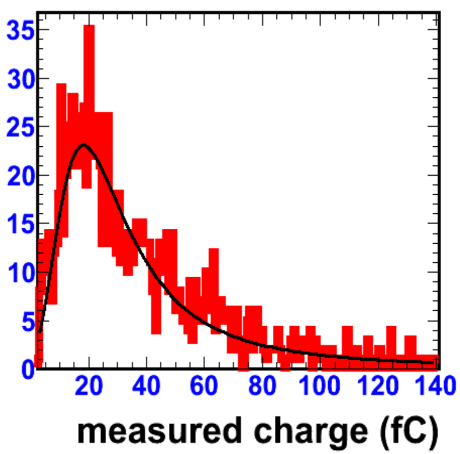
97% efficiency @ 1.5fC th.
Uniformity better than 1%



Gain > 10^4 @ 420V



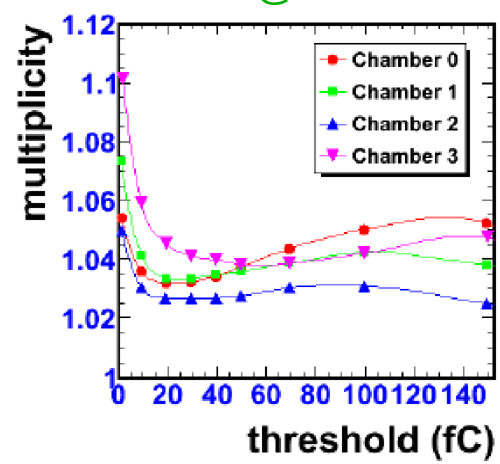
MIP MPV ~20fC
Variations of 11%



2009 JINST 4 P11023

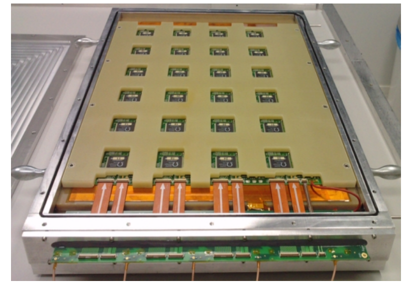
2011 J. Phys. 293 012078

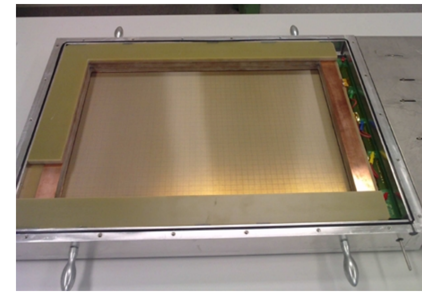
Multiplicity below
< 1.1 @ 1.5fC th.



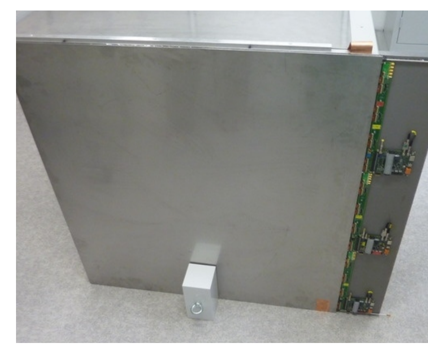
The first large scale prototype - 1x1m^2

Aim: to construct a digital calorimeter consisting from 40 1x1 m^2 layers.
Each layer is assembled from 6 Active Sensor Units





Active Sensor Unit (ASU):
48x32 cm^2 PCB with
- 1536 pads of 1x1 cm^2
- Bulk MICROMEGAS
- 24 HARDROC2 ASICs
- Spark protections
- 2 mm dead edges



First 1x1 m^2 prototype
1.2 cm thick chamber with
- 5 ASUs + 1 ghost
- Gas inlet/outlet
- 2 % dead area inside gas volume

Assembly takes ~1 week

Built and tested in a beam in 2010

Readout electronics

HARDROC2 chip developed by LAL/Omega for GRPC DHCAL

Circuitry:

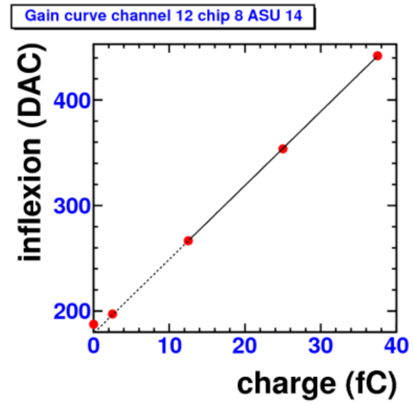
- Digital (2-bit) read-out with 3 thresholds
- 64 channels per chip
- Preamp. with individual gains
- Power-pulsing & self-triggering
- Fast shaping (~20 ns)

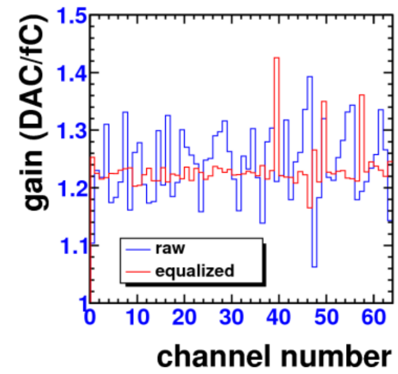
MICROMEGAS case:

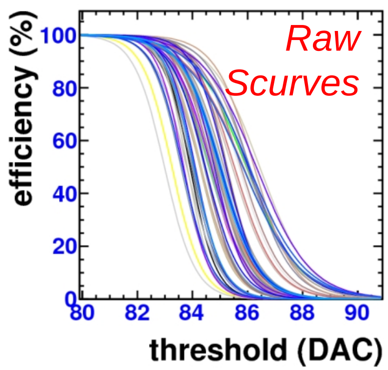
- Single channel noise on ASU ~1 fC
- Chip threshold ~12 fC (5*noise + pedestal dispersion)
- Signal (~25 fC) longer than shaping time
  → Threshold settings is CRITICAL

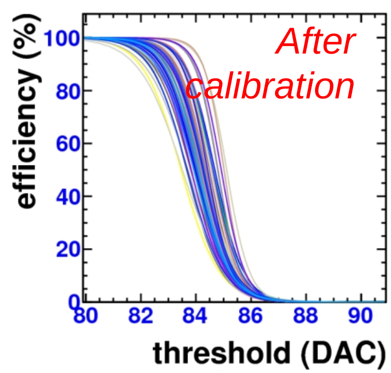
Calibration:

- Measure channel pedestal & preamp. gain (DAC/fC)
- Correct pedestal dispersion with individual preamp. gains
  → Final threshold of ~6 fC

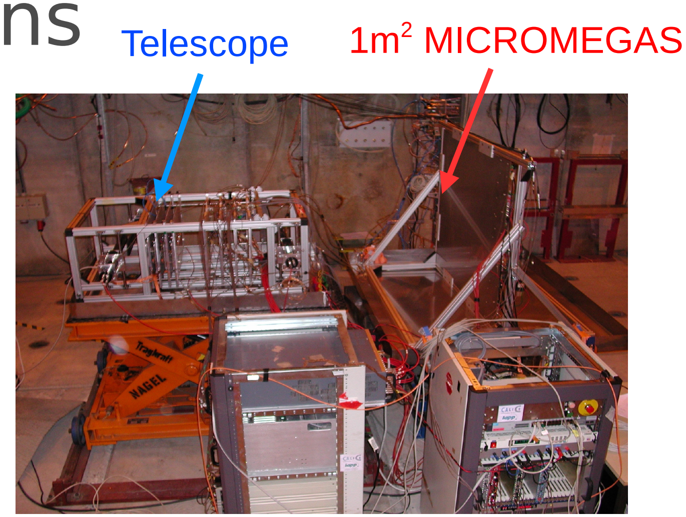






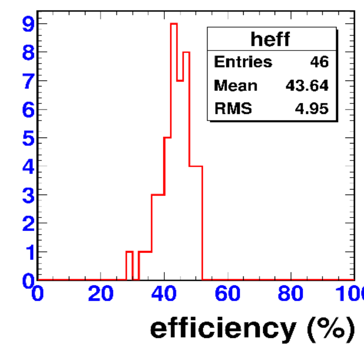


Test with muons



CERN SPS/H4 – June/July 2010
- 150 GeV/c muons
- Telescope + 1x1 m² prototype

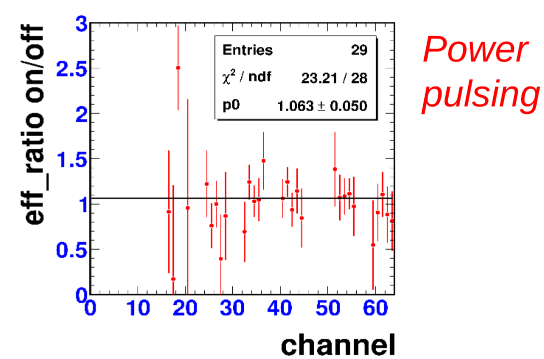
With lowest threshold settings and using 10 % of the 25 fC MIP charge:
- Efficiency of 43 %
- Multiplicity of ~1.05
- Noise probability/trigger ~10^{-5}



Position scan:
- Efficiency depends mainly on threshold not on position (close to spacers, edges, centre…)

Power pulsing:
- Essential for operation at ILC-like machine
- Power pulsing of analogue parts of all HR2 chips during SPS spill: - this corresponds to ~3 A
  - T(ON-OFF) = 2-10 ms

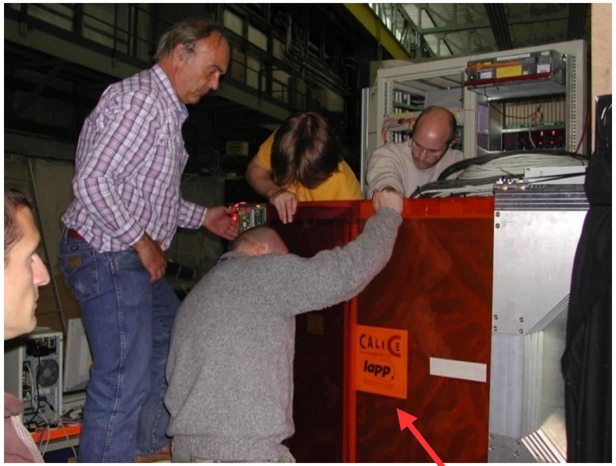
→ No significant effect on efficiency



Test in showers 1/2

CERN/PS/T7-9 - Oct/Nov 2010

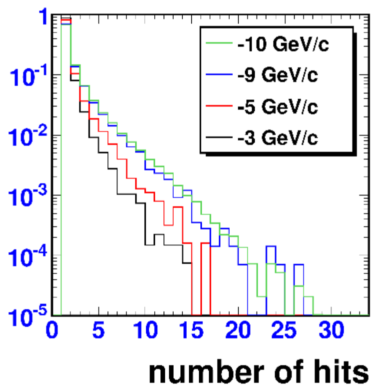
- Up to 10 GeV/c hadrons
- Join WHCAL TB equipped with scintillations and 1m^2 MICROMEGAS as a last layer (#31)

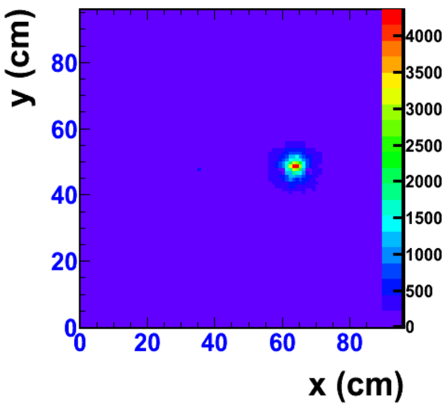


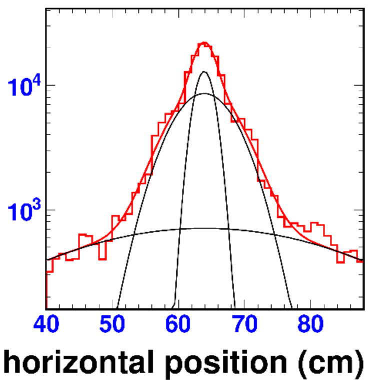
1m^2 MICROMEGAS

Behaviour in hadronic showers (multi-hit events):

- Chamber stability
- Number of hits vs. beam energy
- Hit profile





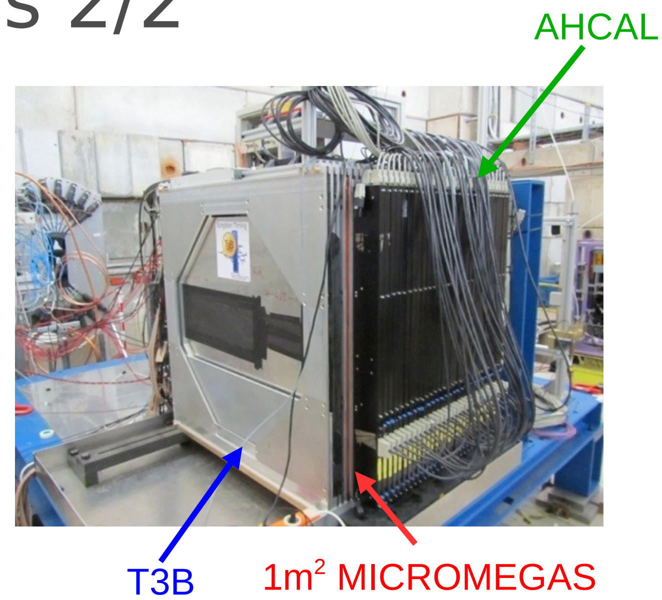


N.B. Limited performances due to low efficiency readout chips

Test in showers 2/2

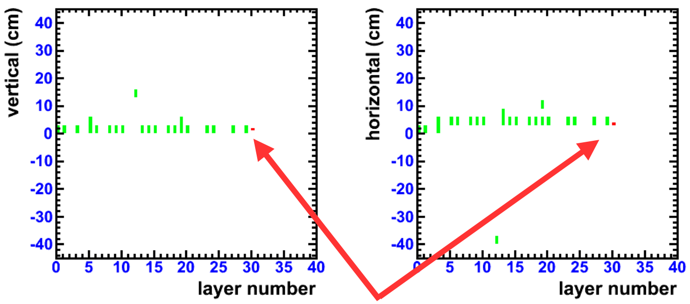
AHCAL and MICROMEGAS combined test:

- Different acquisition rate
  → synchronisation of AHCAL and MICROMEGAS
- Using common LCIO data format for event reconstruction



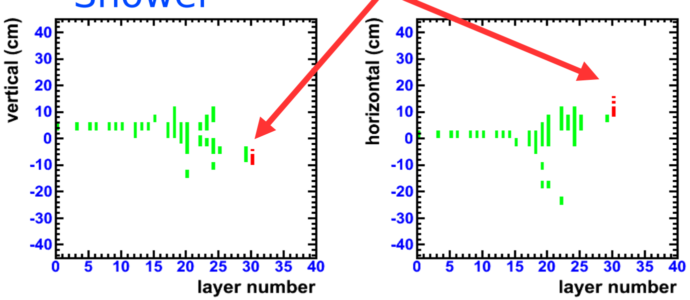
Events displays:

- MIP (example of a 1 event)

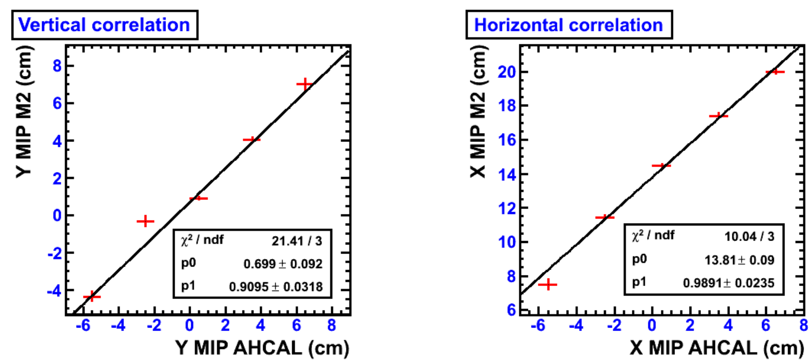


Hit in 1m^2 prototype

- Shower



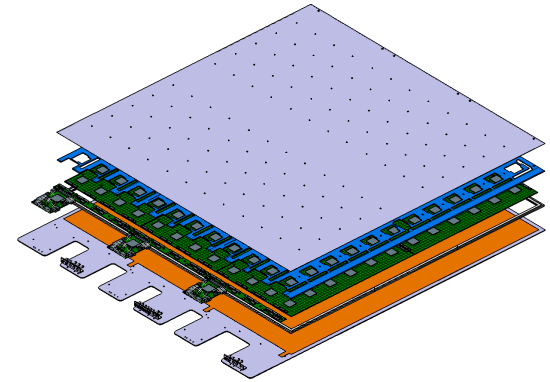
Correlation of MIP position in AHCAL and MICROMEGAS

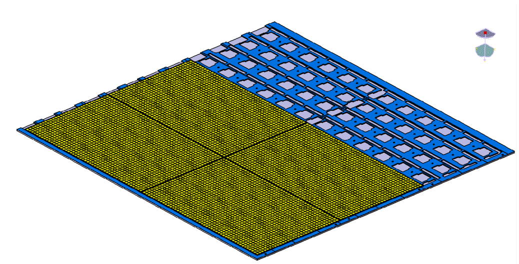


New 1m^2 MICROMEGAS chamber

Improved mechanical design:

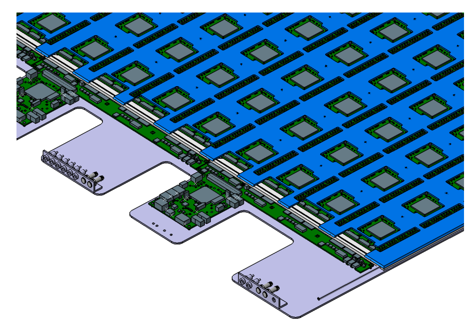
- Baseplate screwed instead of glued
  → Access to ASIC side of ASUs
- Gas tightness made by ASU and mask one side, drift plate on top side
  → Eventually: get rid of Fe baseplate
    → improve absorber stiffness (+2mm)
- ASU mask thickness reduced from 2 to 1 mm
  → Thinner chamber (7 instead of 8 mm active thickness)
- Easier access to DIF connectors and LV & HV patch panel when chambers are inserted inside structures





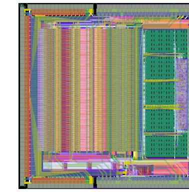
Readout electronics:

- New readout ASIC – MICROROC
- Fault tolerant design of PCB circuity
  → possible chip bypass
- Improved spark protection

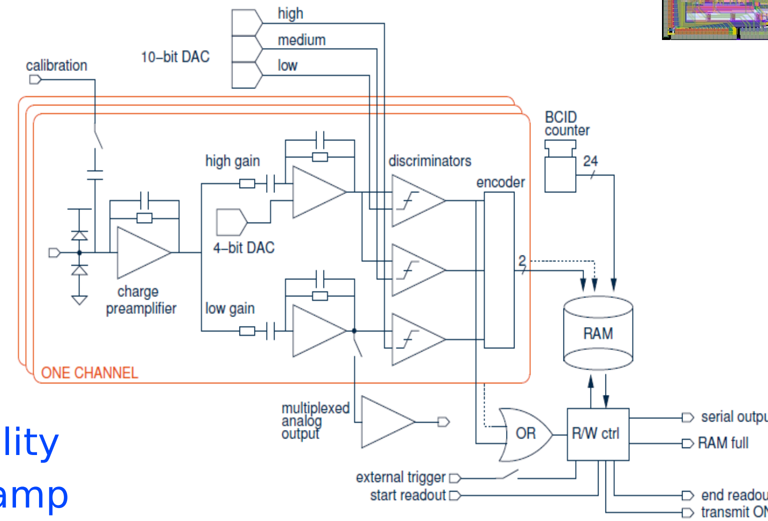


New prototype will be tested in a beam during august 2011

MICROMEGAS read-out chip

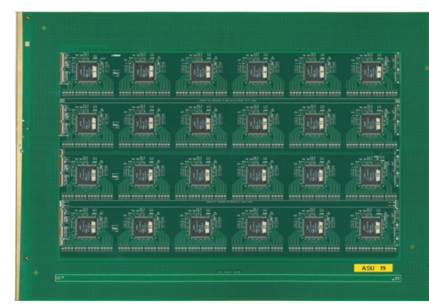


MICROROC developed in collaboration between LAPP & LAL/Omega



From HARDROC2 to MICROROC:

- Same digital part + pin-to-pin compatibility
- Current preamp replaced by charge preamp
- Additional spark protections inside silicon
- Fast shaper (~20ns) replaced by 2 tunable shapers (30-200 ns)
- 8 bit preamp gain corrections replaced by 4-bits pedestal corrections



Status:

- 350 chips produced, 200 tested, yield of 88 % (enough to equip two 1x1 m^2 prototypes)
- 6 ASU equipped and detailed calibration on-going

MICROROC ASU electronic tests

1m^2 MICROMEGAS = 6 ASU, 144 chips, 9216 channels

Pre-amplifier gain:

- Average all chips ~7.1 DAC/fC
- Variations all chips < 2.5 % RMS
- Variations single chip < 1% RMS
- Compatible with single chip measurements

Pedestal dispersion:

- ~5 DAC units which is about 1 fC
- Applying pedestal corrections
  → dispersion reduces by a factor of 2

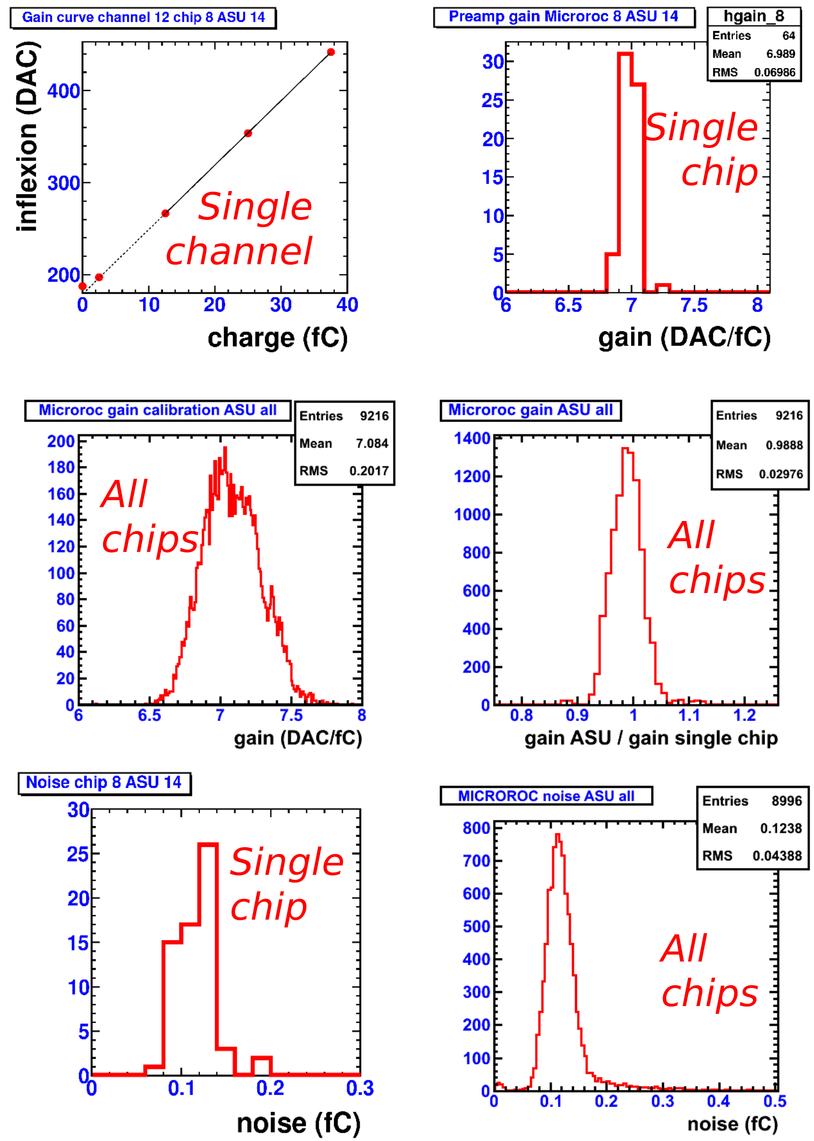
Noise level

- Average all chip ~0.12 fC
- Variations single chip ~0.03 fC RMS

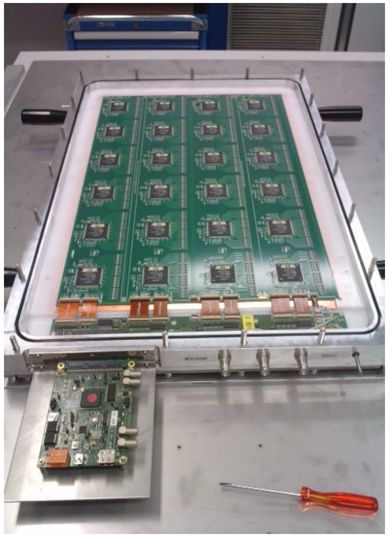
Detection threshold:

- 5*noise + dispersion leads to ~1 fC
- Threshold higher with Bulk: ~2 fC

Remember: MIP MPV is @ 25 fC
→ signal/noise ~12



MICROROC ASU tests in gas 1/2



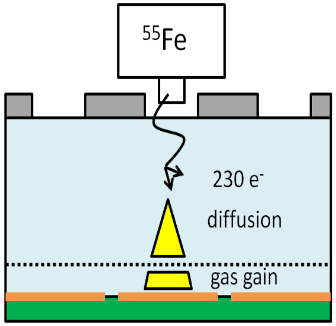
HV training

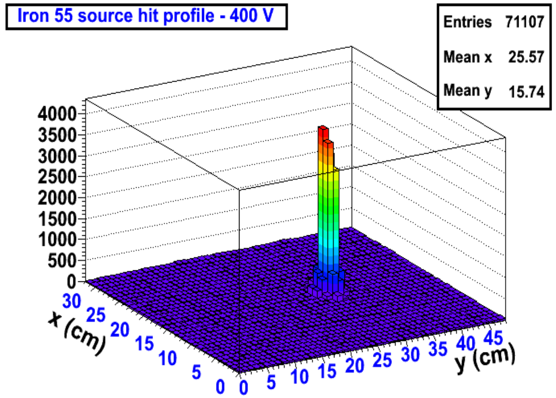
- ASU “cooking” in air (~800 V), very few sparks → manufacturing process @ CERN well controlled

X-ray and cosmic tests

- ASU installed in gas box (~1 cm drift gap)
- Test of completely chain (Bulk+VFE+DAQ)
- Each channel can be tested individually

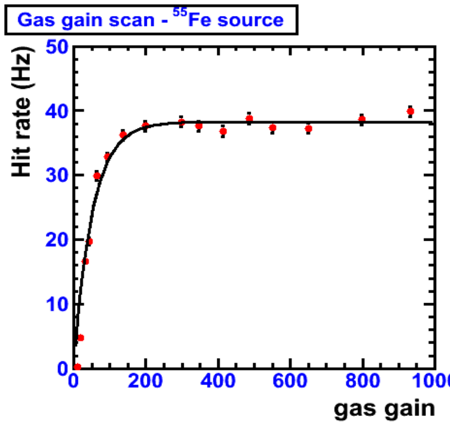
Response to an ^{55}Fe X-ray source

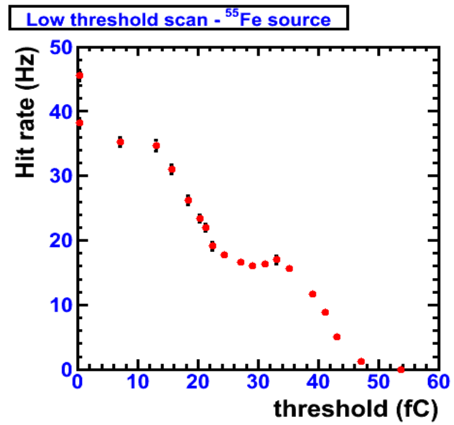


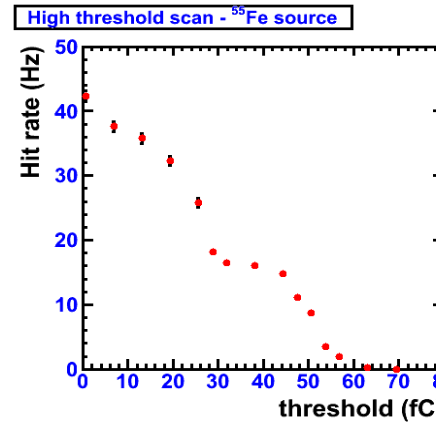


MICROROC ASU tests in gas 2/2

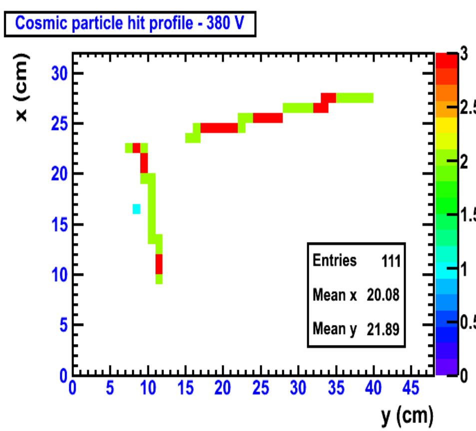
Study of chamber properties with an ^{55}Fe X-ray source

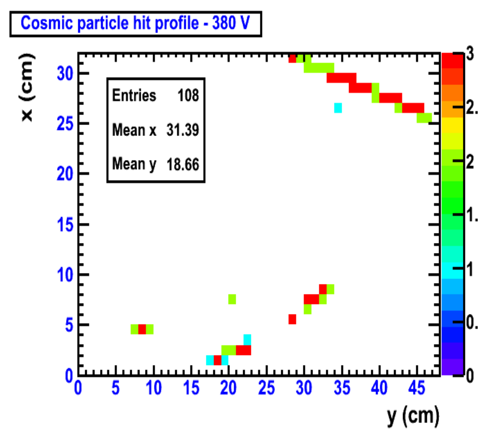


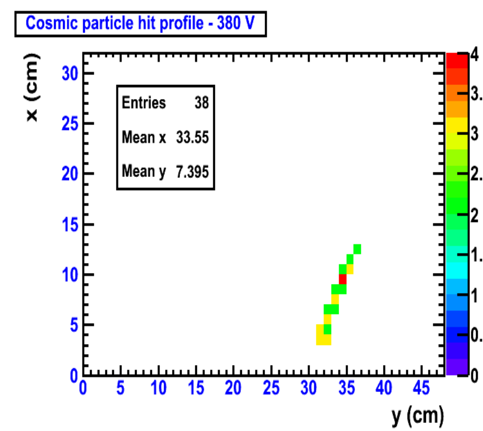




Event display for the vertical chamber position







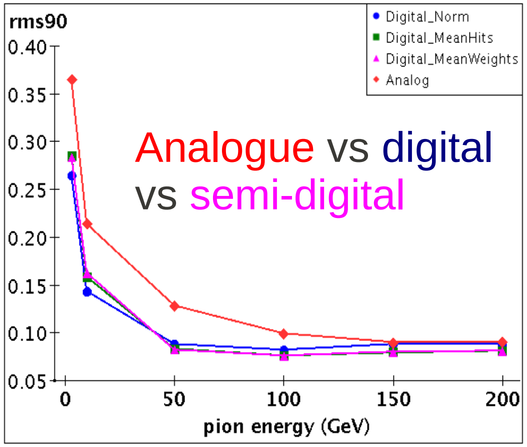
Next step: assembly of the 1m^2 chamber in June and TB in August

Study of MICROMEGAS-based calorimeter

Geant4 simulation studies in conjugation with chamber development:

Performance with a semi-digital readout

- Signal digitisation implemented:
  Energy, primary statistics, mesh transparency, gas gain, charge thresholds
- Optimisation of multi-thresholds for better resolution and linearity on-going



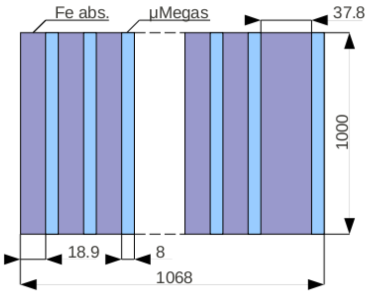
Optimization of the HCAL design

- Projective and tailed geometries
- Impact of the cracks on HCAL performance
- Energy containment and leakage corrections

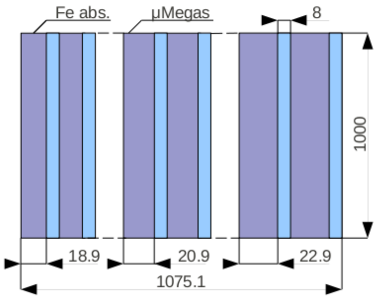
Test beam study

- Definition of the TB program
- Comparison of MC and data

1. HCAL with thick back plate



2. HCAL with progressive abs. thickness



Summary and outlook

Important achievements in 2010

- First 1x1 m^2 prototype fabricated and tested
- Several technical choice validated and TB goals reached
- Important hardware and software development

Moving forward with a new FE electronics

- Smooth transition from HARDROC to MICROROC
- Improved mechanical design
- Assembly of new 1x1 m^2 chamber in June, TB in August
- Second chamber in September
- TB in W/Fe structures at the end of the year

Sustain efforts

- Supporting simulation studies
- DAQ developments for CALICE collaboration

Acknowledgements

LAPP LC Detector group

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