Concept and status of the CALICE AHCAL engineering prototype

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TIPP, Chicago

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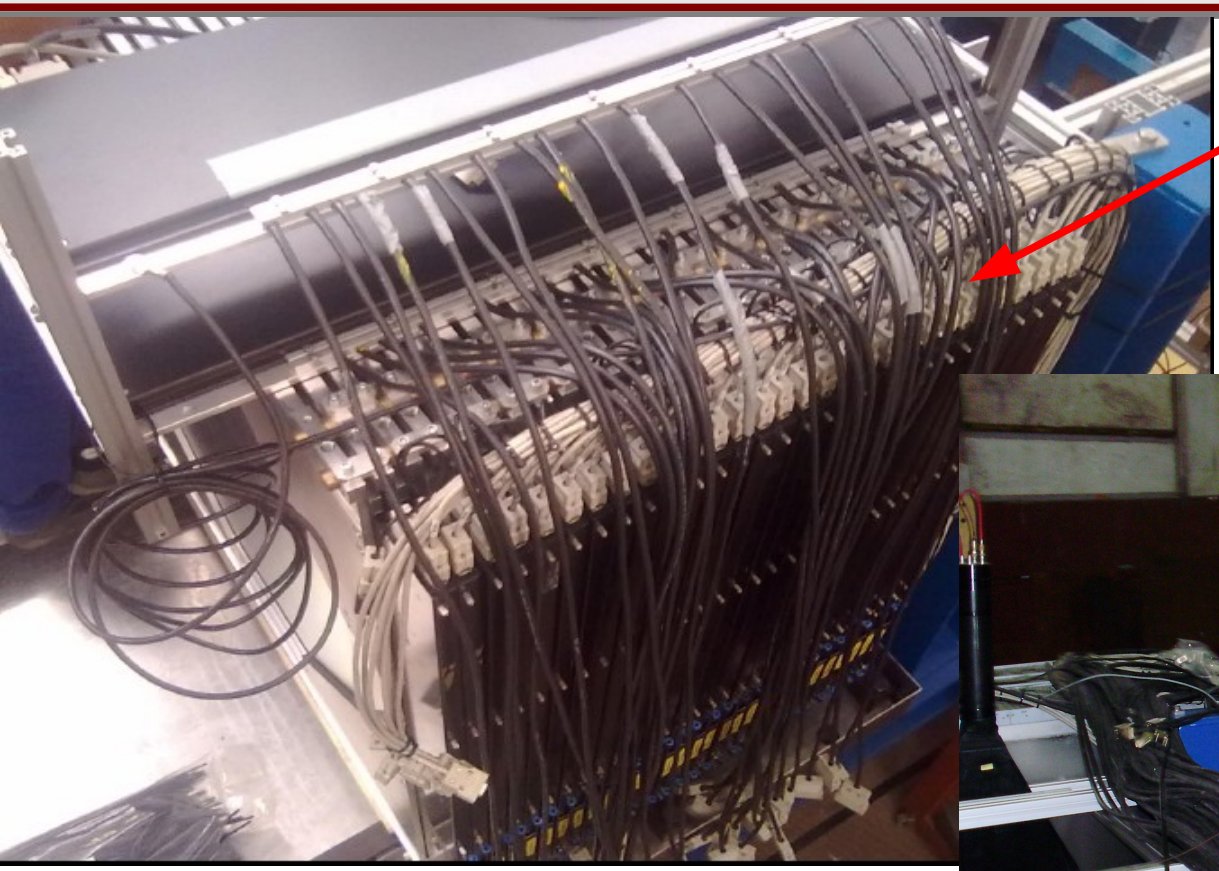
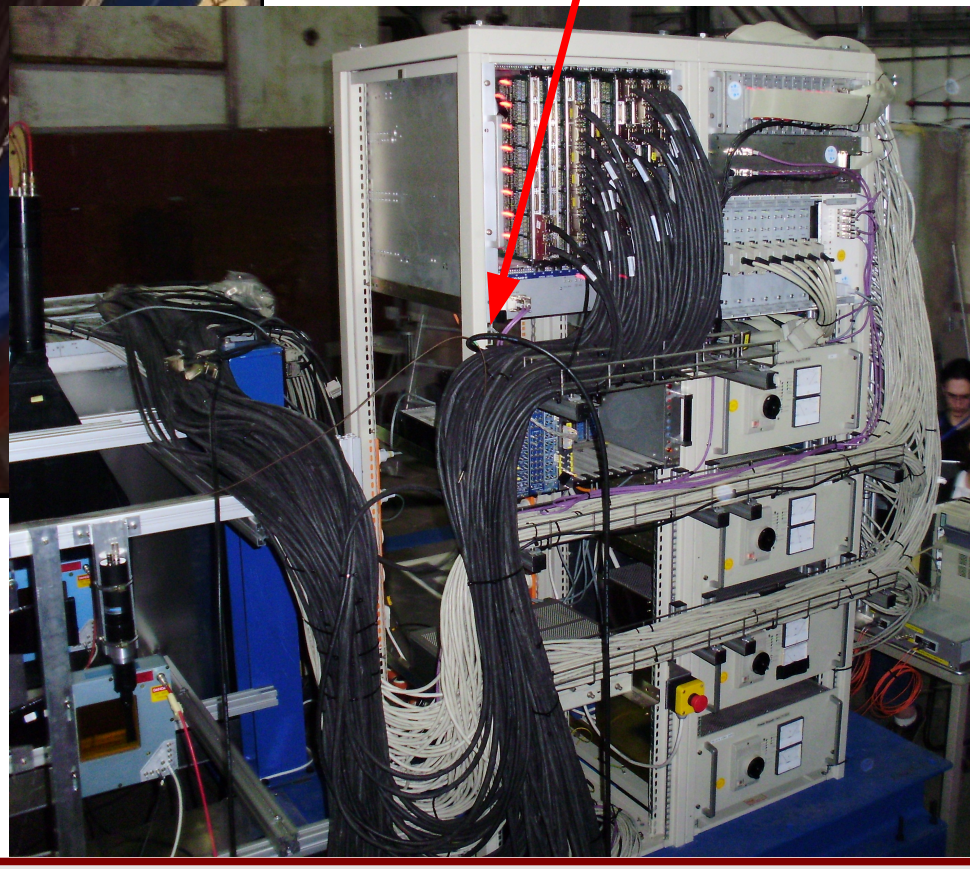
- Concept and status of components
  - New scintillator tiles
  - First tests of new ASICs
  - Power pulsing
  - DAQ integration
- Summary and outlook

The AHCAL physics prototype



Cables for calibration boards

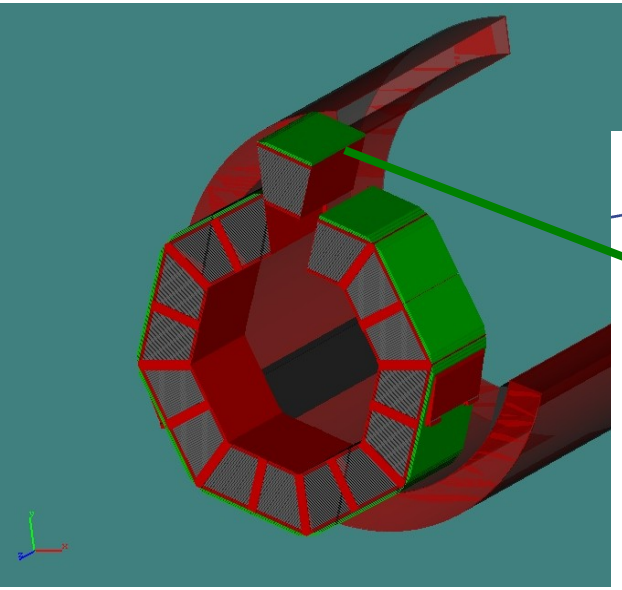
Cables from analog to digital part of electronics

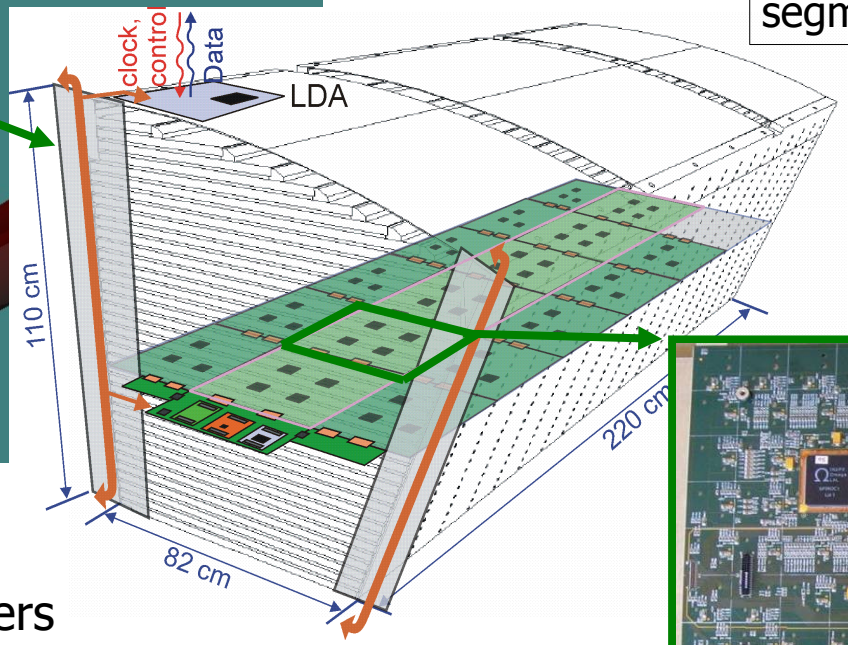


→ Need to build realistic engineering prototype

The engineering AHCAL prototype

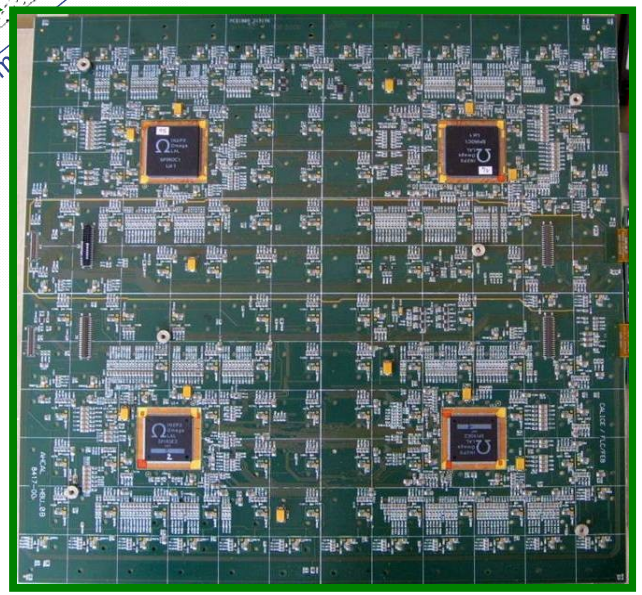
Development of scalable LC detector based on successful experience with physics prototype





Octagonal shape, 16 equivalent wedges, segmented in two along z

PCB with 4 ASICs, 144 scintillator tiles, SiPM readout



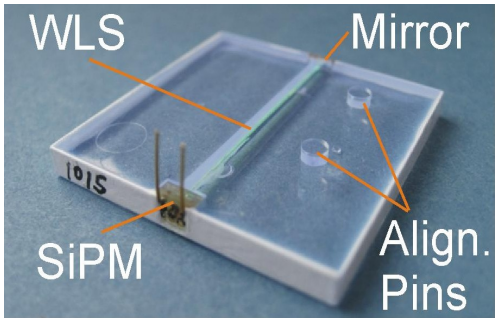
Challenges:

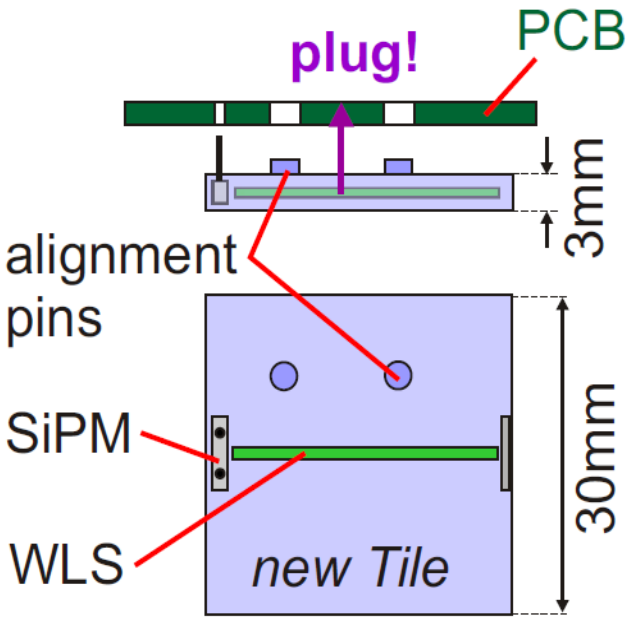
- No spacer between layers
- Minimize dead material between wedges
- Minimize gap between barrel and endcap

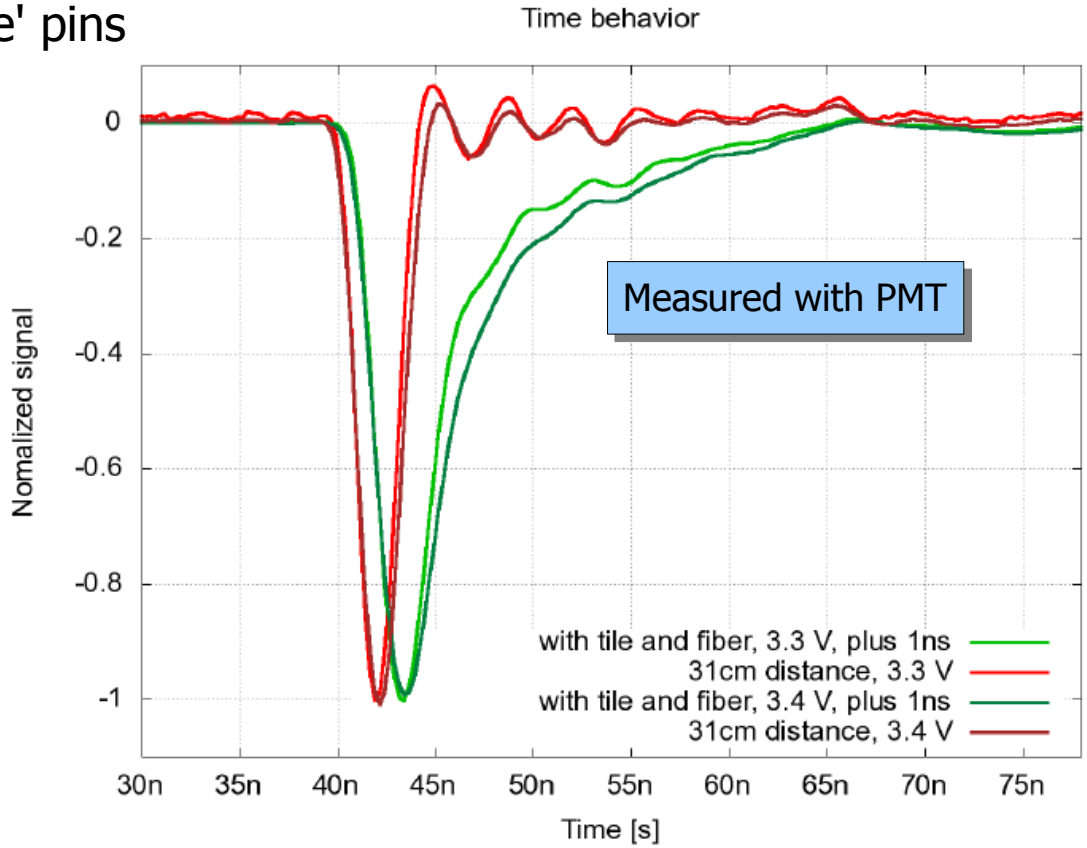
→ Integrated readout electronics

Scintillating tiles

- Signal sampled by scintillating tiles
  → 3x3x0.3cm^3, 2592 tiles per layer
- Wavelength shifting fiber, since SiPMs most efficient for green light
- Plugged into PCB with 'lego-like' pins
  → Nominal tile distance 100µm

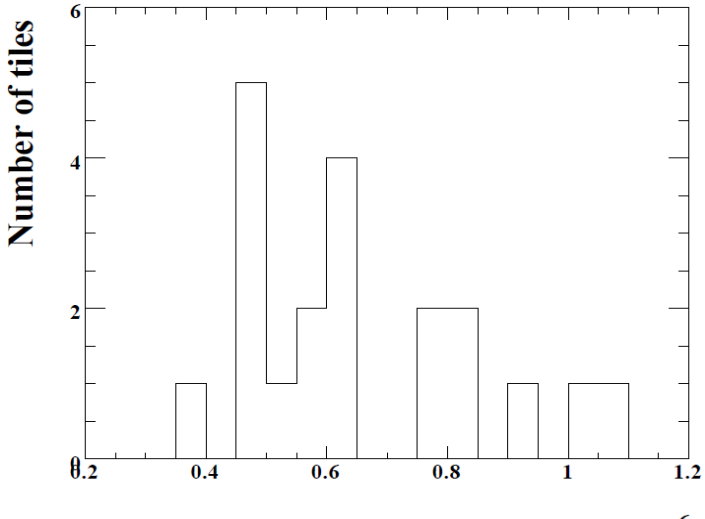


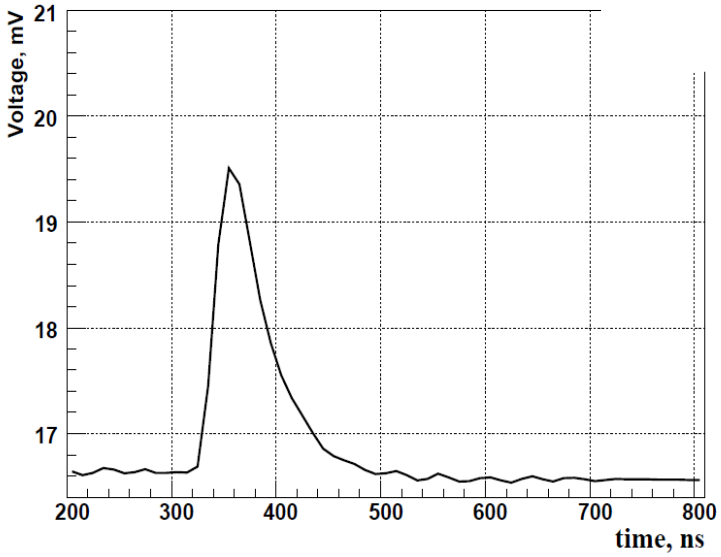


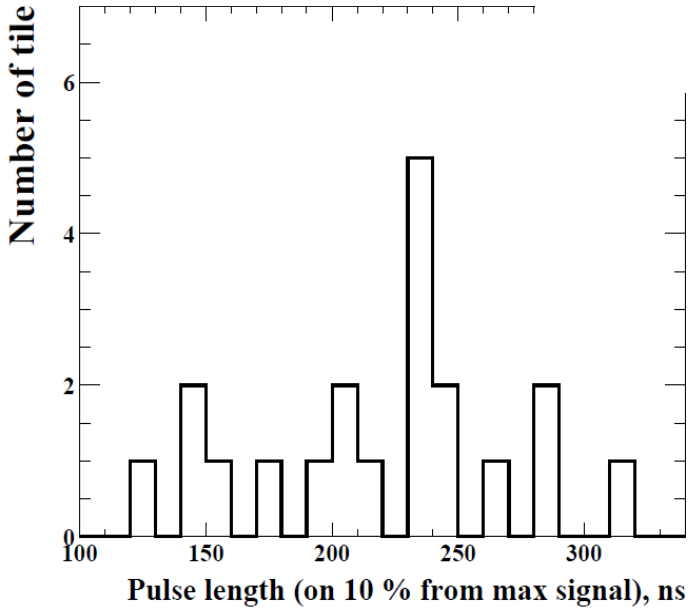


Scintillating tiles

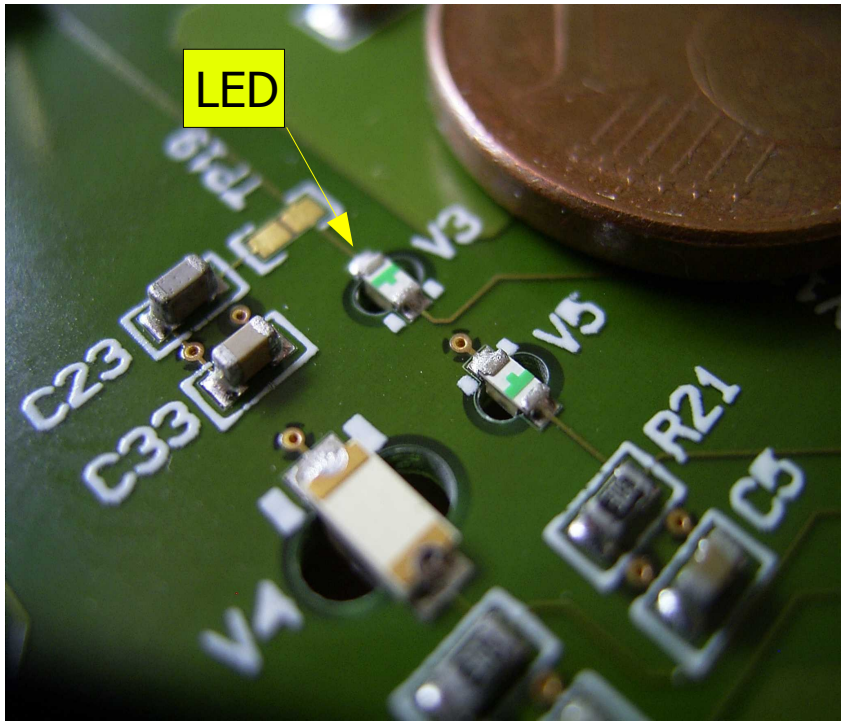
- First batch of new tiles with SiPMs with 796 pixels have been tested on simple testbench and with full readout chain
- Pulse length 120ns – 320ns
- Gain 0.4 – 0.8 * 10^6
- Calibration system needed for SiPMs

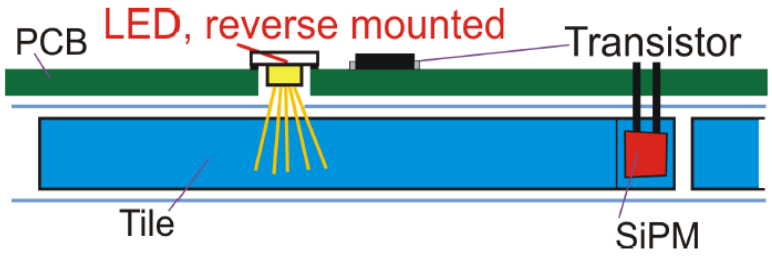






LED calibration system





System task:

- SiPM gain calibration via single pixel spectra
- SiPM saturation (limited number of pixels)

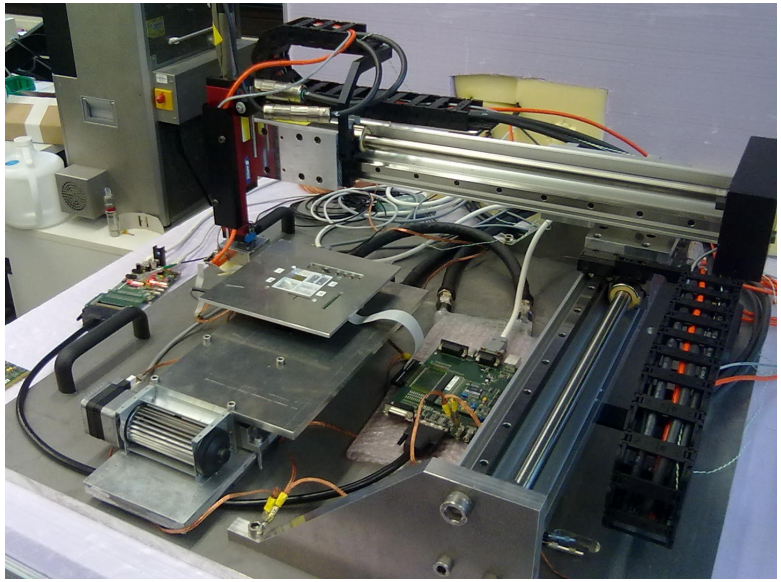
Solution for engineering prototype:

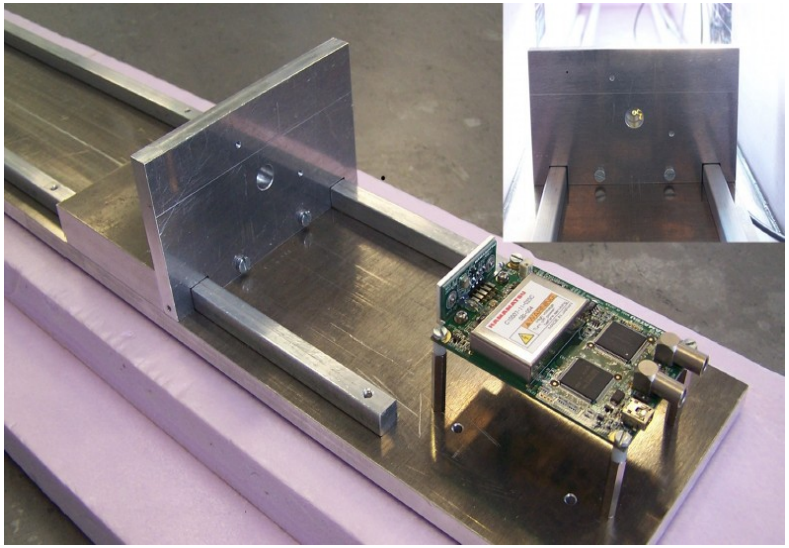
- Light directly coupled into the tile by 1 integrated LED per channel
- Easy to fully integrate
- BUT:

  → different light intensity for each channel (using common bias voltage)

  → limited LED bias to prevent electrical cross talk

LED calibration system





Blue vs UV LEDs

- High internal capacitance for blue LEDs (market requires high light output...)
- Blue pulses too long for current tiles

→ Chose UV LEDs, blue option for future

Test results:

- System tested with PMT and full tile/SiPM readout
- Light pulse length ~10ns for different amplitudes
- LED loading capacity array on each channel to improve uniformity of LED output

→ Design of LED driver circuit finished, tested and implemented in new front-end board design

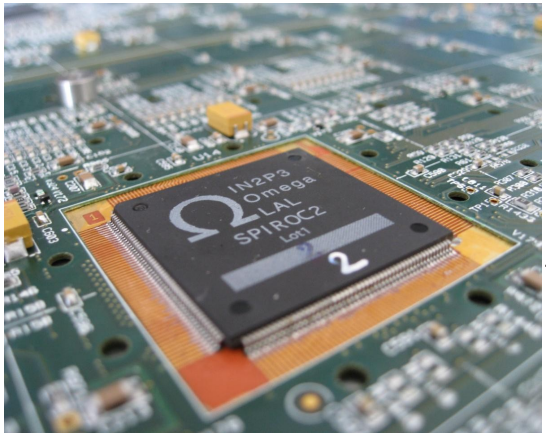
SPIROC2

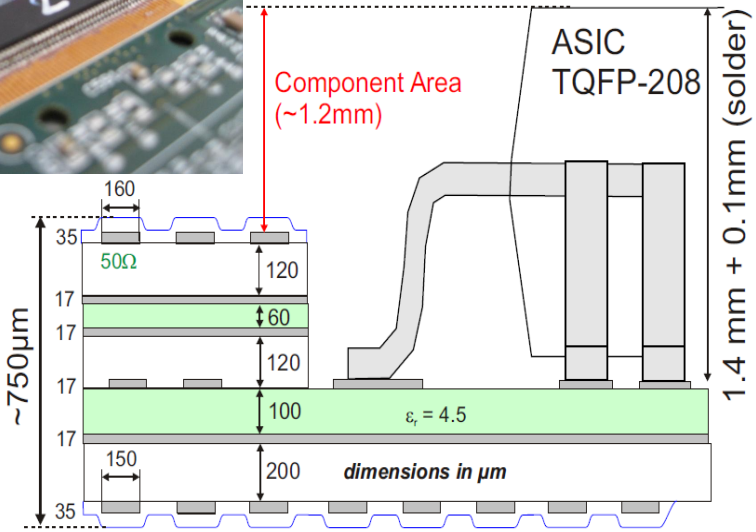
Specific chip for SiPM readout:

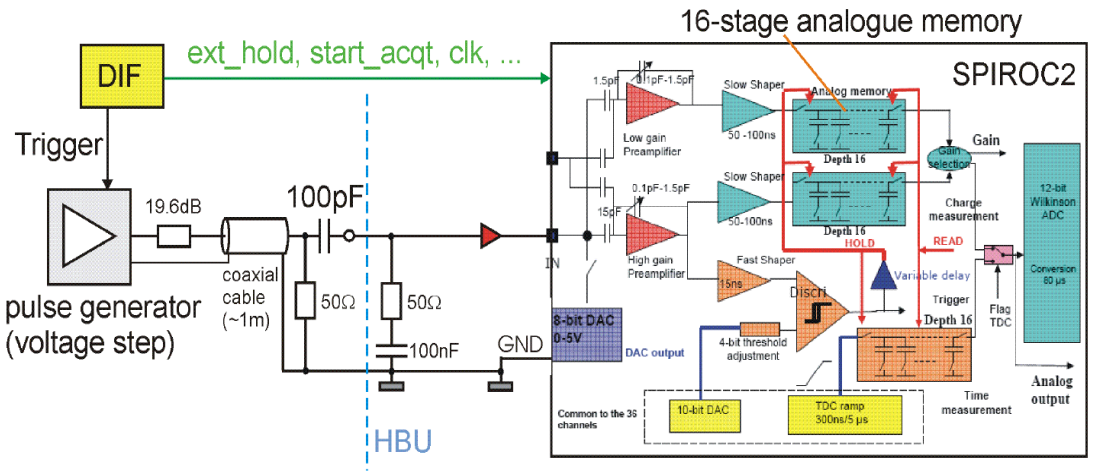
- Input DAC for channel-wise bias adjustment (36 channels)

Designed for ILC operation:

- Power pulsing → 25µW/ch
- (Auto) dual-gain setup per channel
- Internal ADC
- Autotrigger mode
- Time stamp (300ns ramp, 12bit TDC)







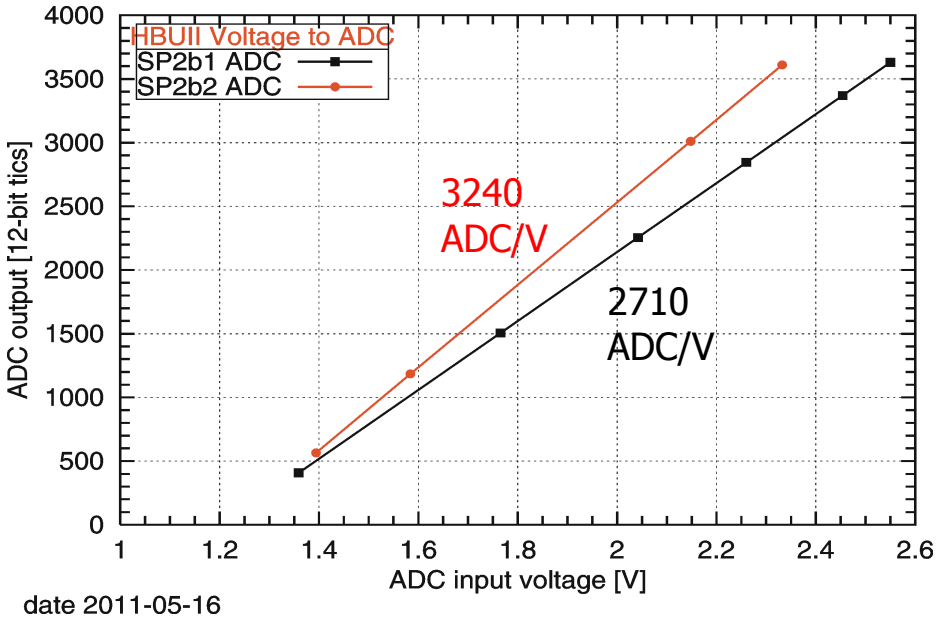
Charge injection setup

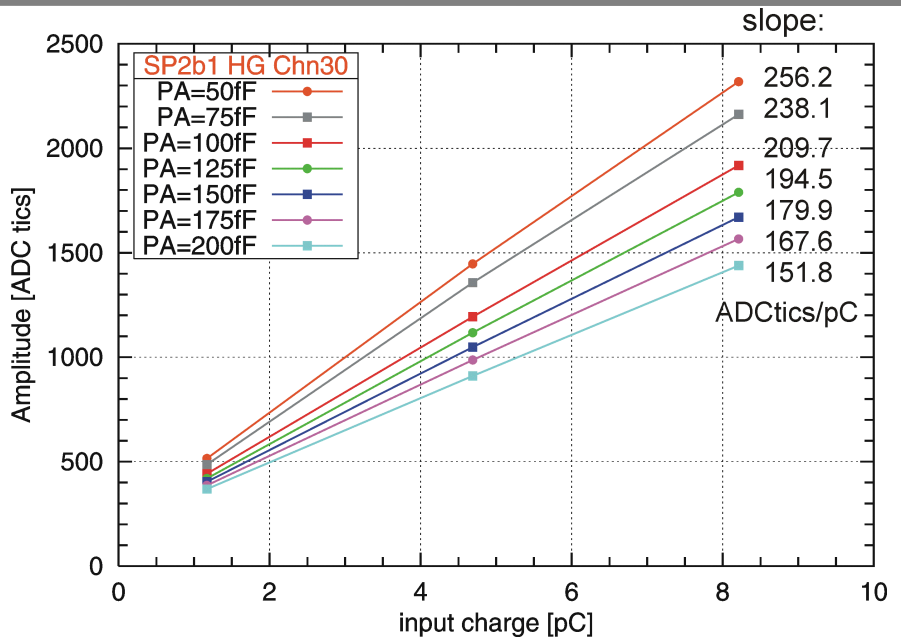
Placement of components in PCB cutouts

→ 300µm/layer

→ 30mm in total!

SPIROC2b – First tests





- New version of ASIC -SPIROC2b- integrated in front-end board for first tests

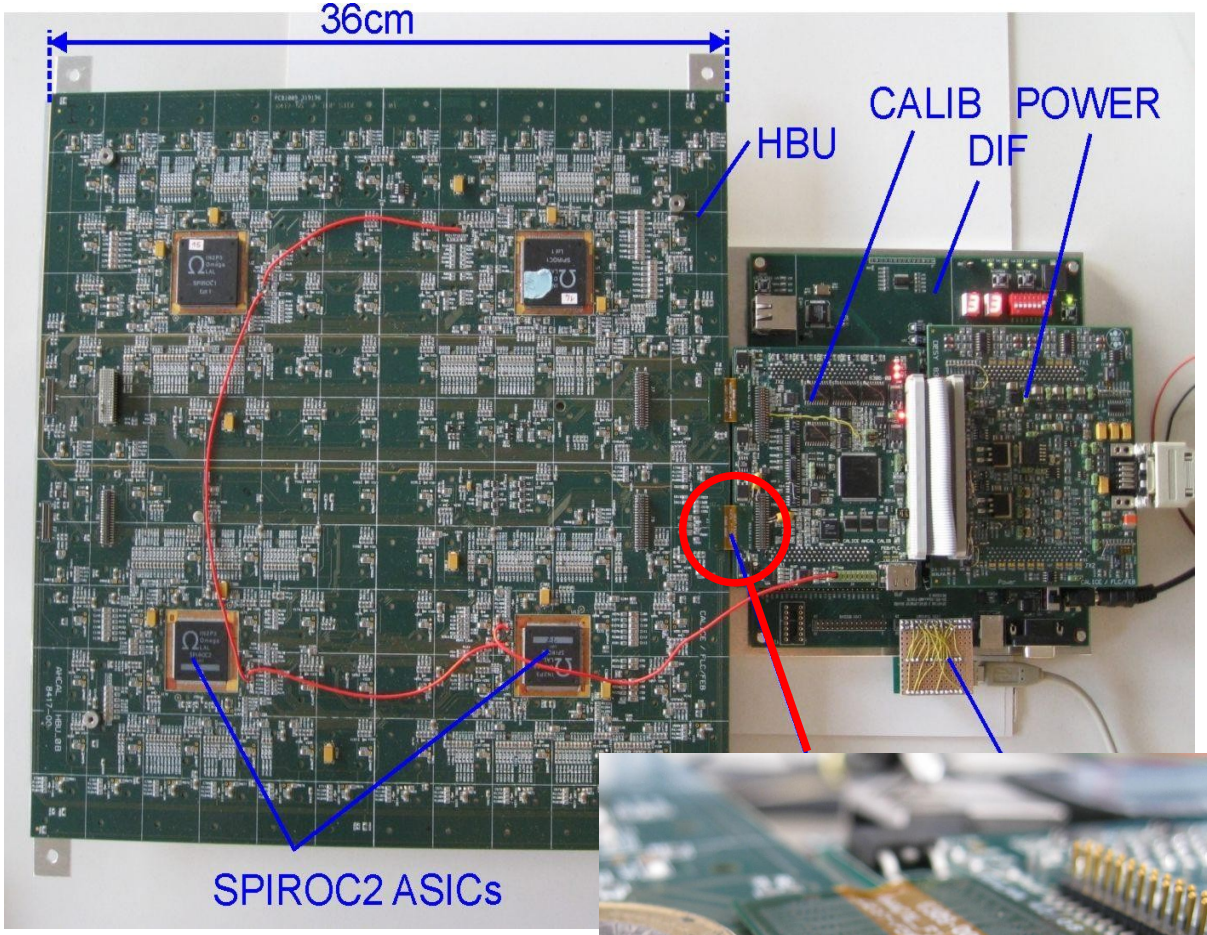
  → Channel-wise gain and trigger threshold selection since SPIROC2b
- Debugging of system integration ongoing
- Started first measurements of linearity, output DACs, PA gain ...

The front-end board - HCAL Base Unit

- PCB with 4 ASICs
- 144 channels equipped with scintillator tiles, LEDs, SiPM readout
- Interconnectivity with ultra-thin flex leads
- 6 PCBs in a row (2.2m), 3 rows per layer
- No cooling in layer!

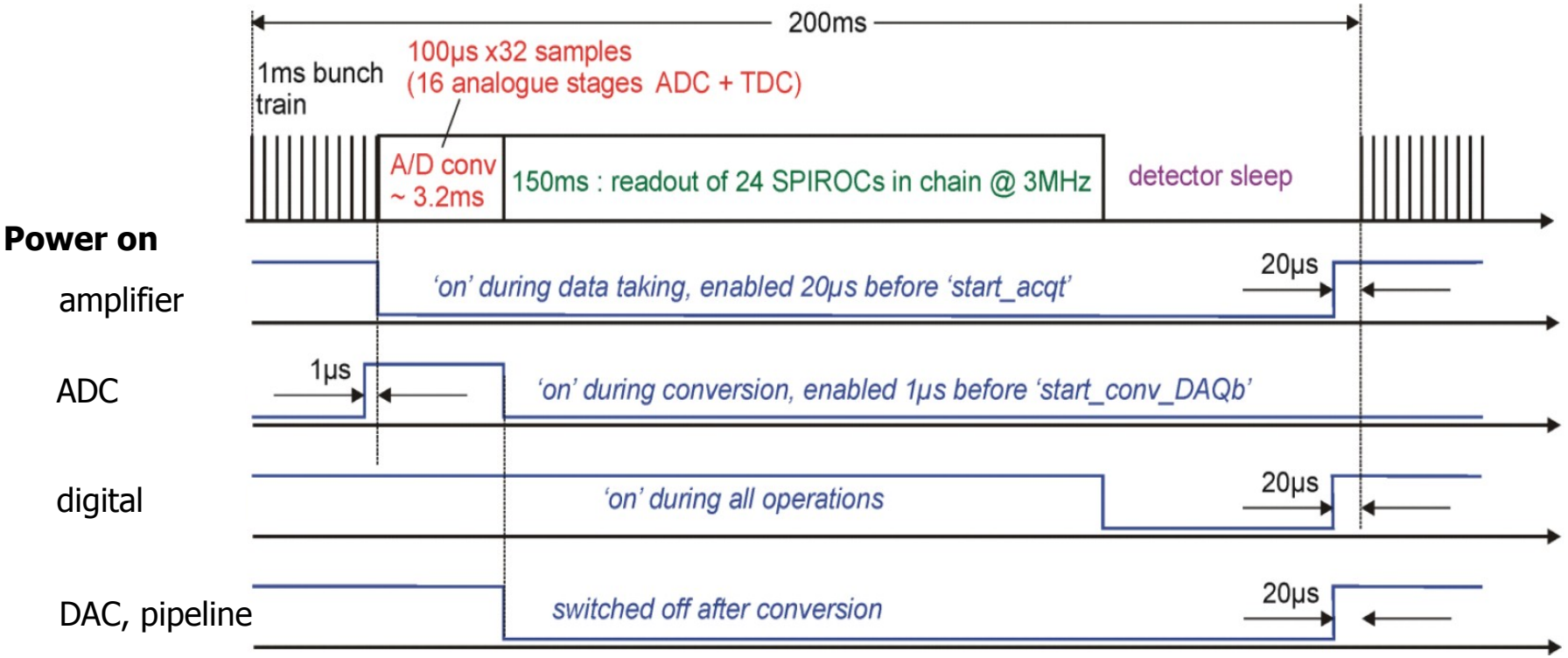
  → Power pulsing
- ~30.000 PCBs in HCAL barrel

New design finished, production ongoing

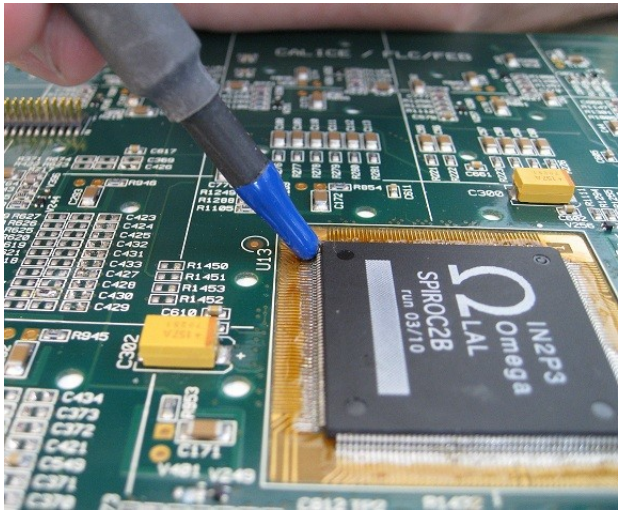


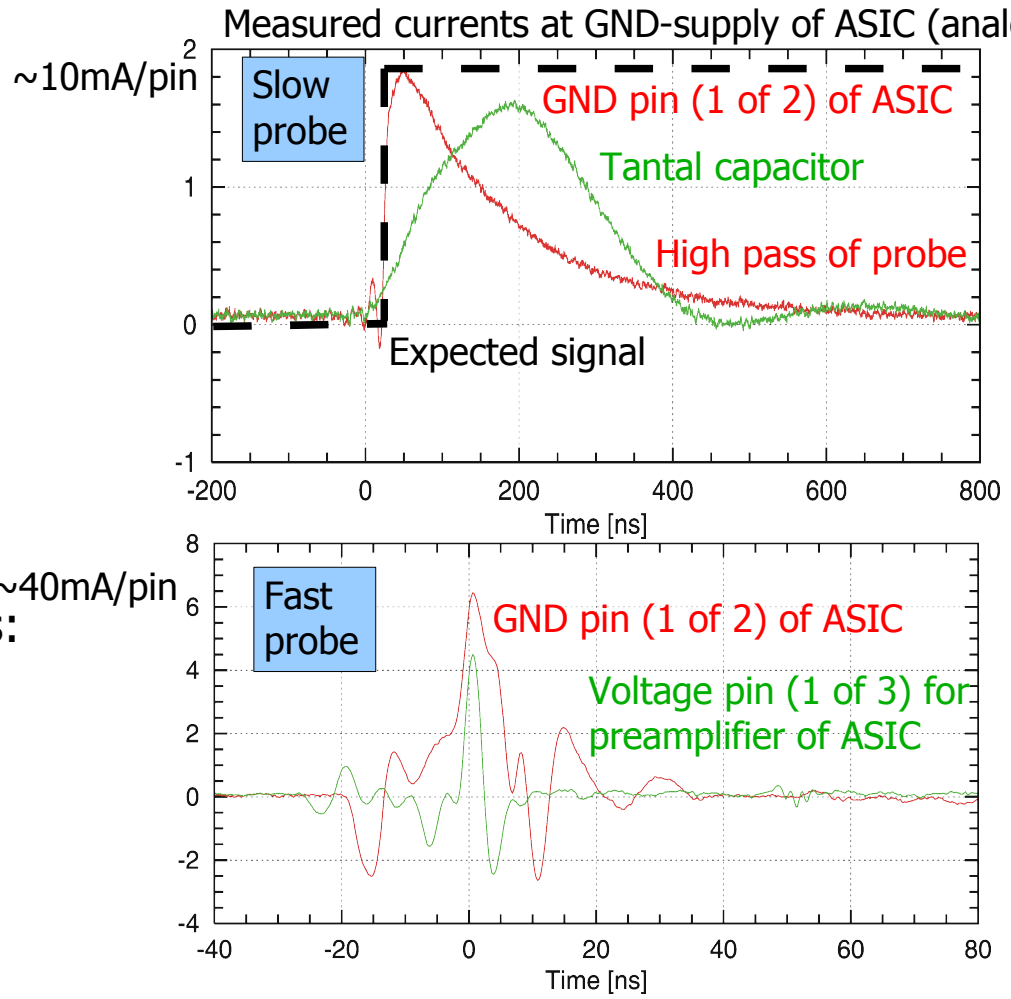
Power pulsing

- Mechanical constraints: no cooling within layers, only at end of steel structure
  → Power pulsing of ASICs needed to reduce heat development
  → Allowed power consumption for ASICs: 25µW per channel
- High voltage (SiPM bias) not pulsed: 15µW per channel



Power pulsing – ASIC current





- PWR-GND for board with 4 ASICs:

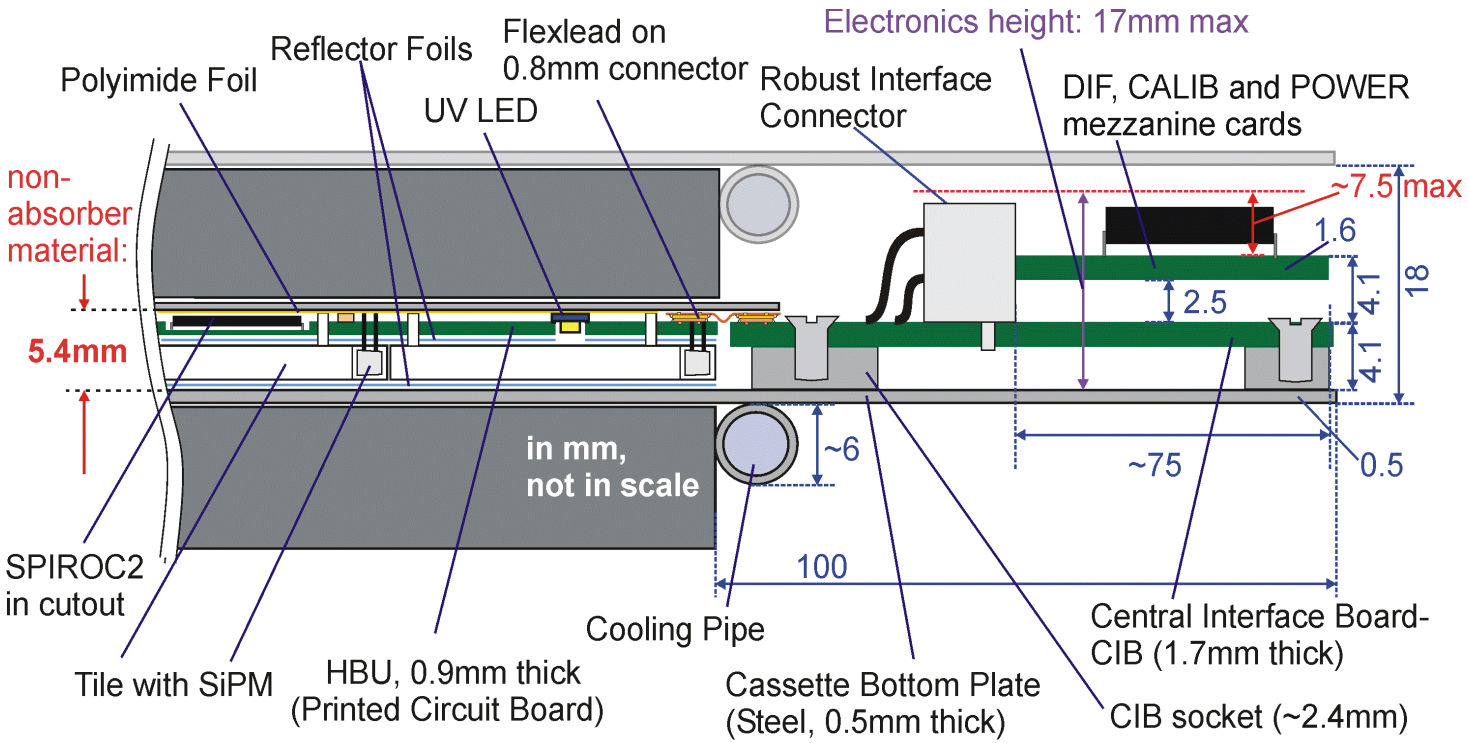
  → 75nF in PCB, 10µF ceramic, 800µF Tantal
- Currents switched: ~40mA/ASIC
- Measurement of current:

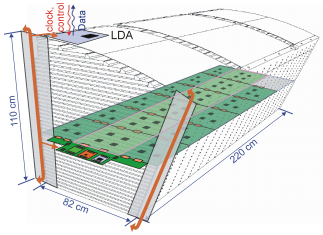
  → Slow: 0.25MHz – 50MHz

  → Fast: 30MHz - 3GHz

→ System has to deal with 5Hz from train repetition to few 100MHz, 2.2A for a layer

AHCAL layer – cross section

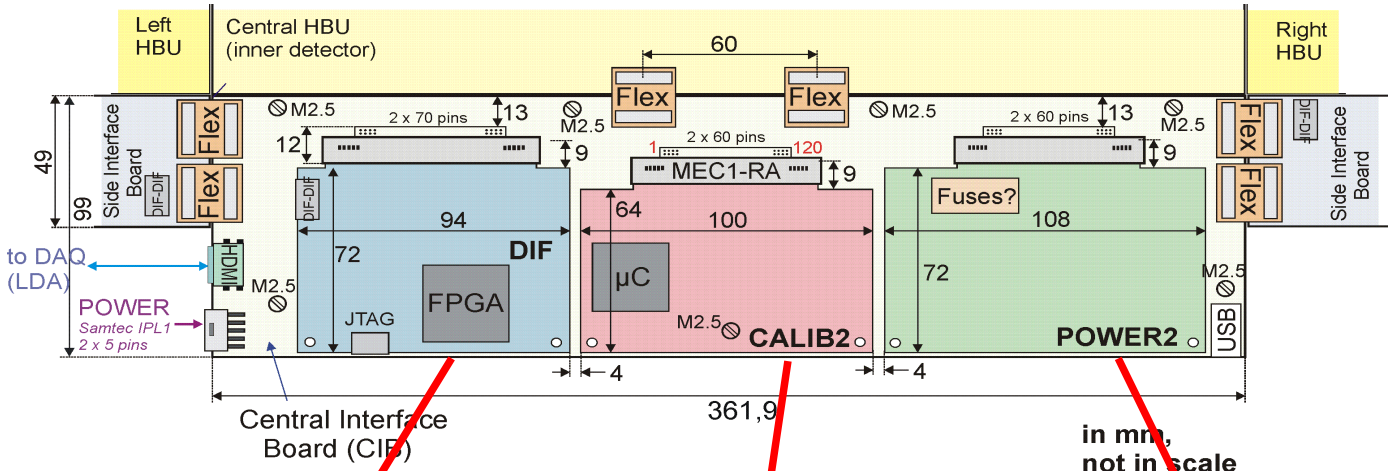


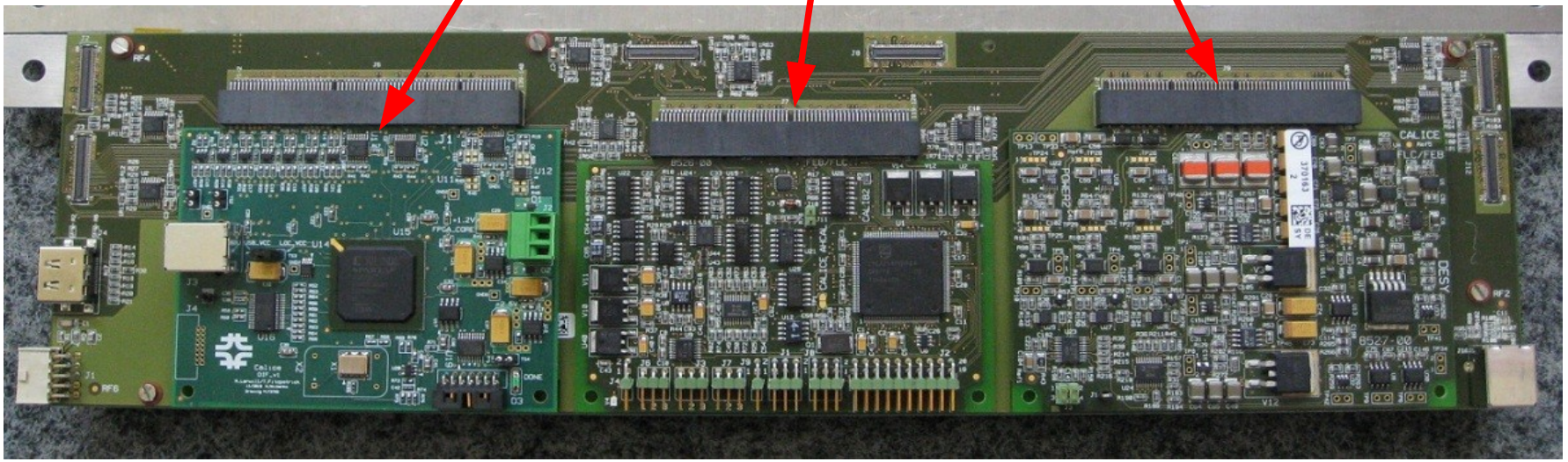


Abbr.	Name
DIF	Detector Interface Board
CALIB	Steering for LED calibration
CIB	Central Interface Board
HBU	Front-end board

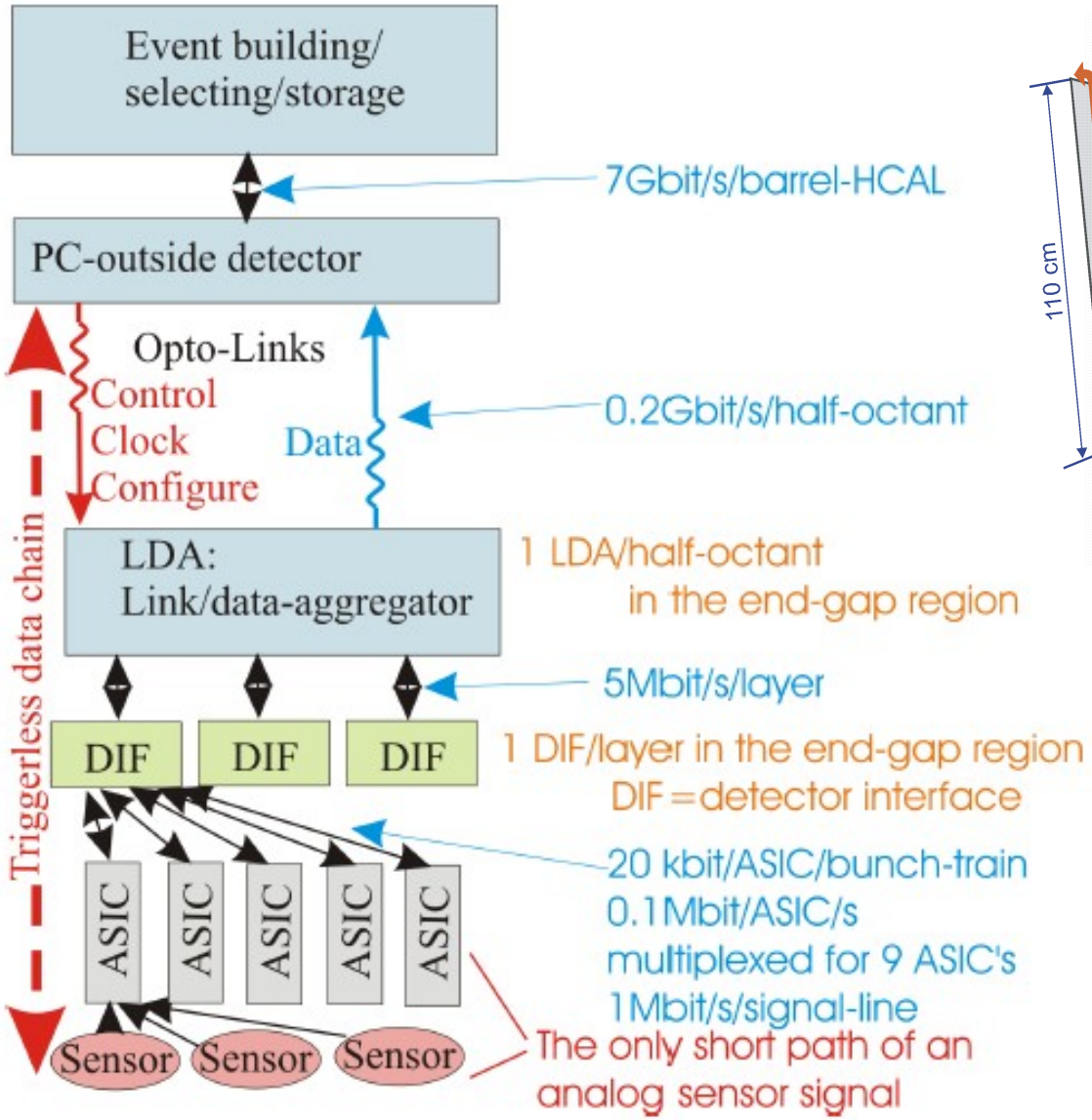
- Compliant with steel and tungsten options
- Redesign and production of components almost finished

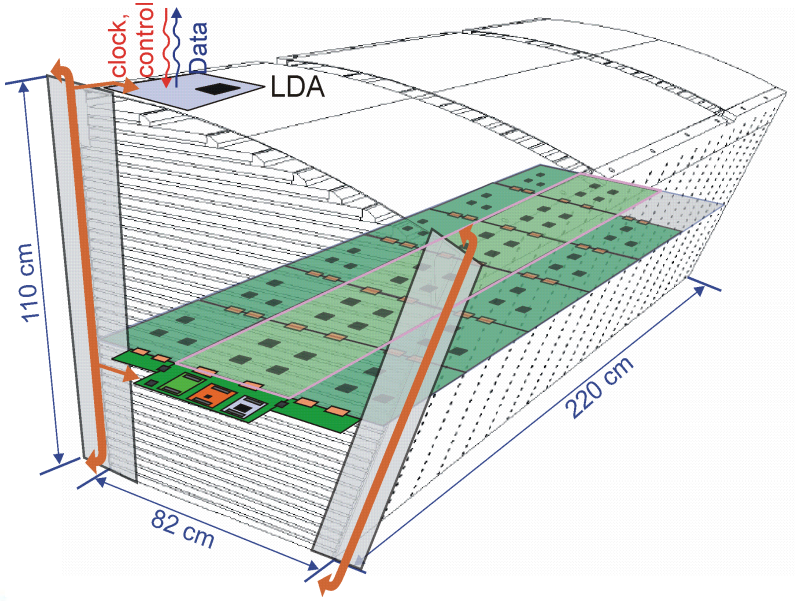
DAQ interface electronics





Data acquisition

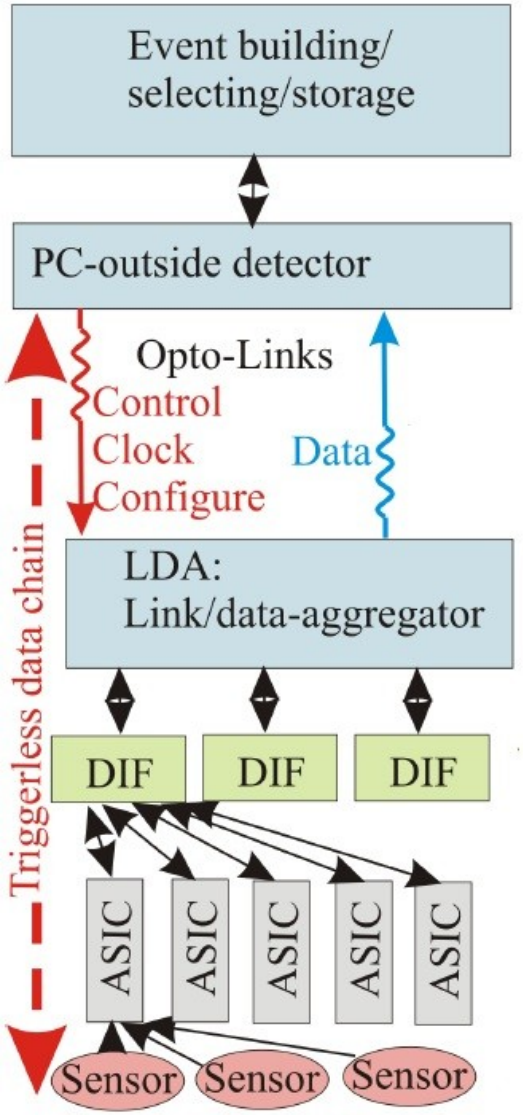


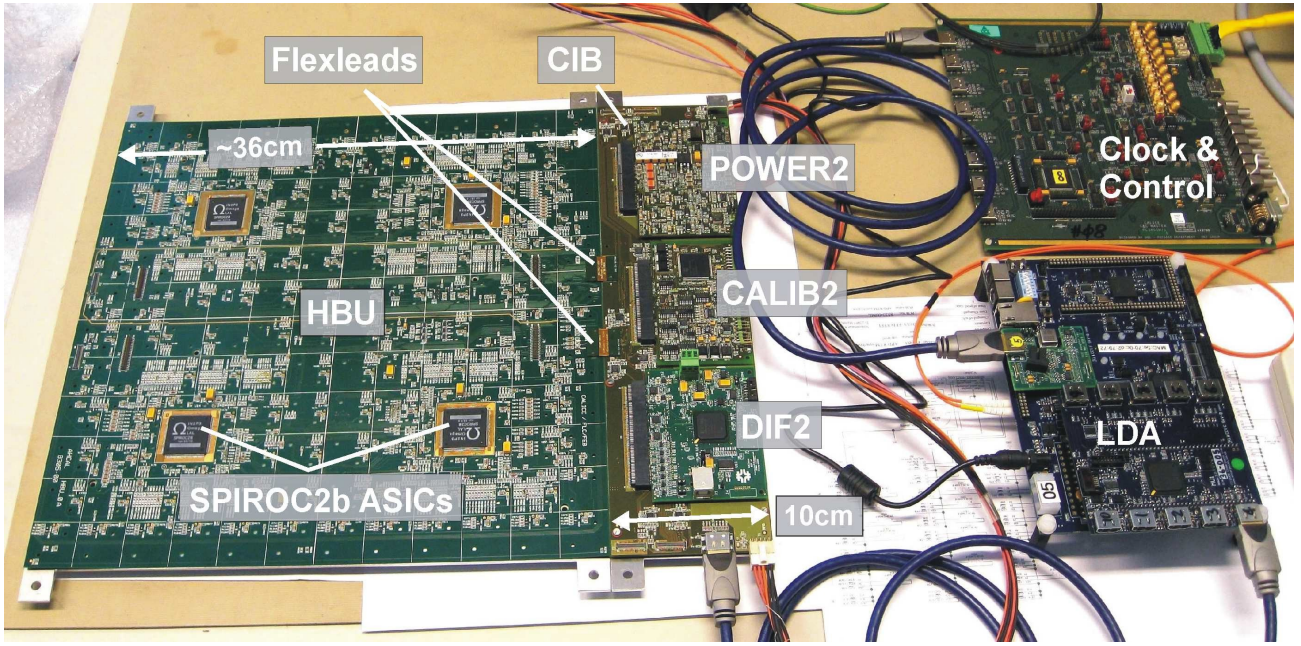


- Moderate data rates using channel-wise self-triggering

  → No need for further front-end event selection

Data acquisition





- All components assembled at DESY
- Started to use testing interface from LLR
  → Setup of communication chain ongoing
  → PC → LDA → DIF → ASICs and back

Summary and outlook

- New technological AHCAL prototype under development
- New tiles tested successfully
- LED calibration system development for new front-end board finished

  → Redesign of front-end board finished
- First SPIROC2b tests
- First steps for DAQ integration successful
- First tests of power pulsing

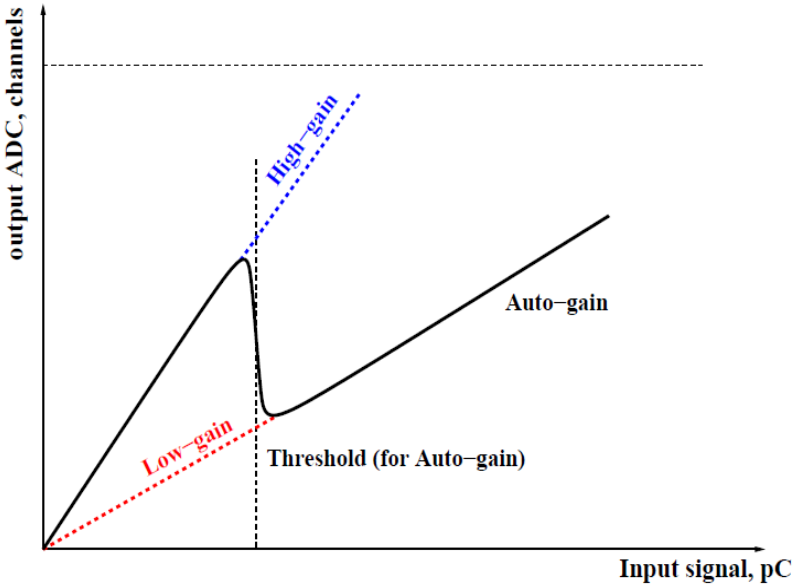
To do

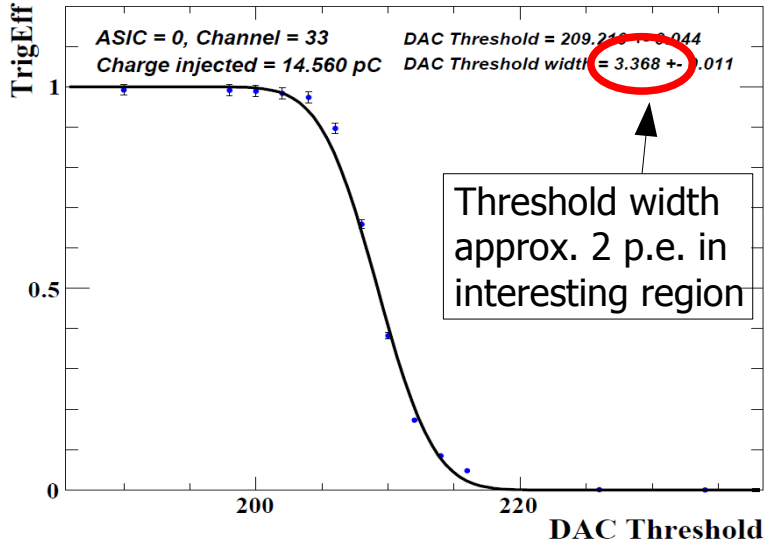
- Further tests of ASICs and power pulsing
- DAQ integration and further development
- This year: Integration to full slab (2.2m calorimeter layer)

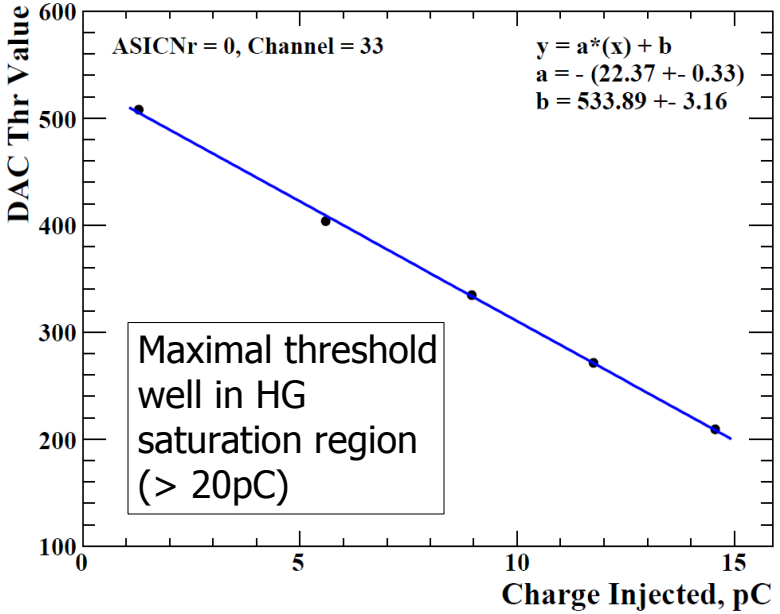
  → Measurement of time structure of hadron showers in test beam

Autogain performance

- Autogain: automatically switch between high gain and low gain mode
- Compare signal with predefined (10 bit) DAC threshold
- Good linearity, similar performance as for auto-trigger

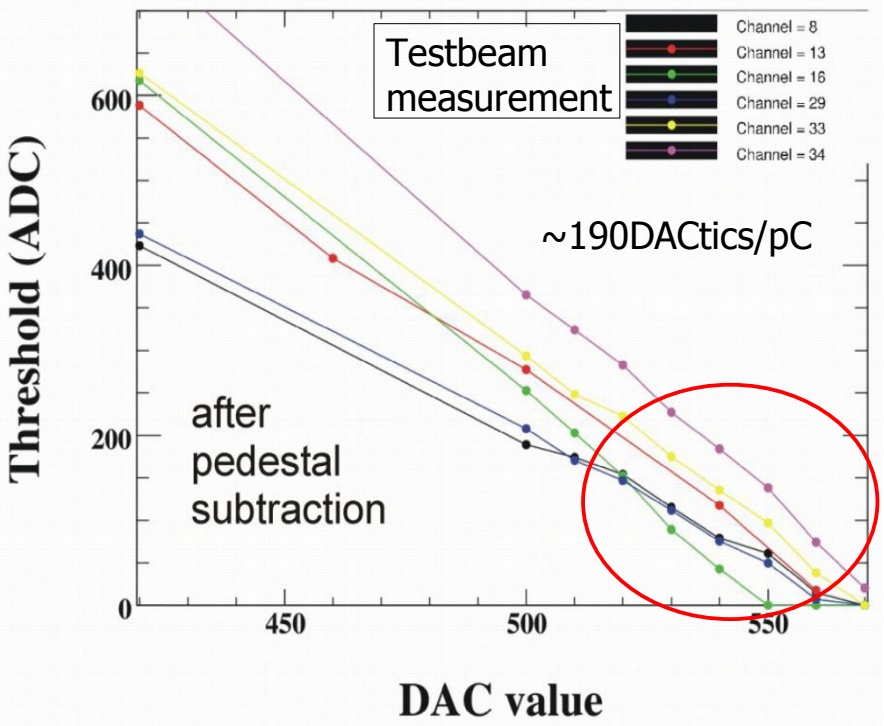


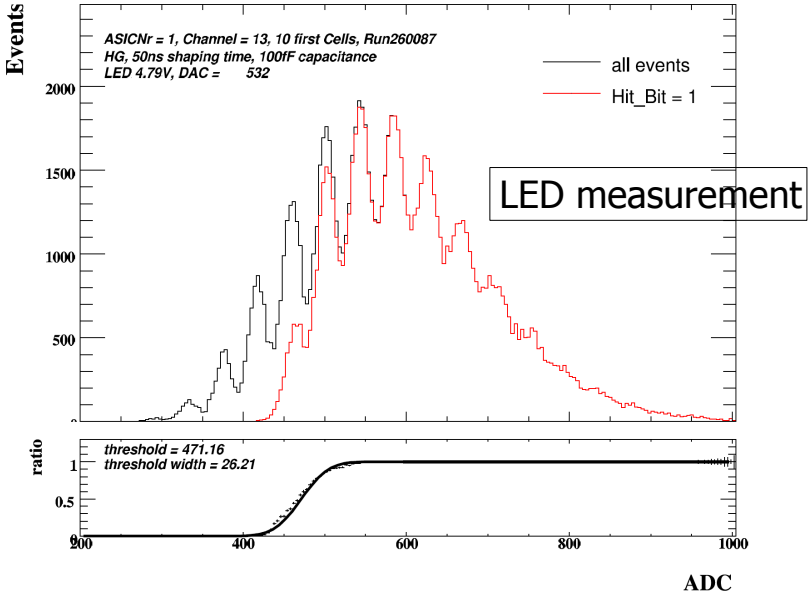


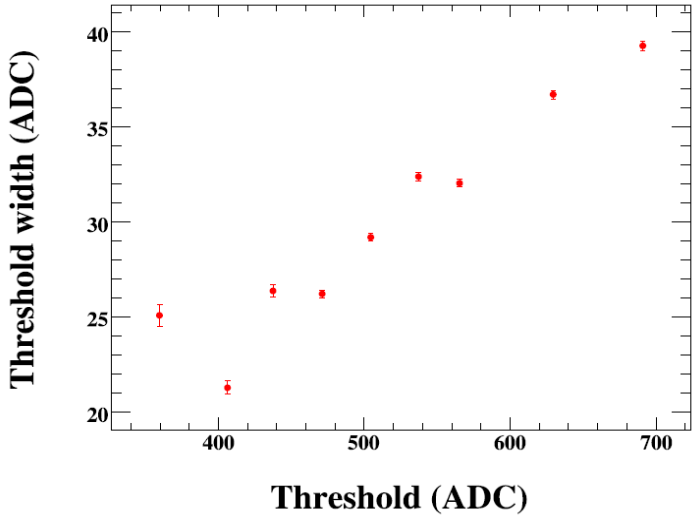


Autotrigger performance

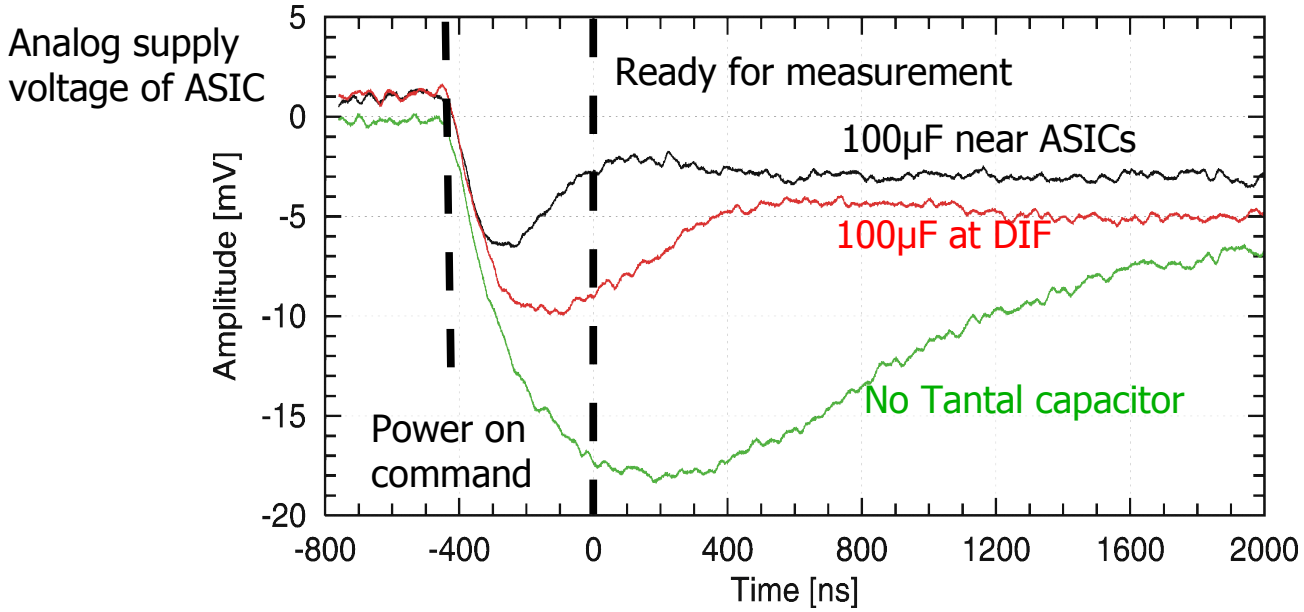
- Autotrigger: mode of ILC operation
- Compare fast shaped signal with predefined (10 bit) DAC threshold
- Set threshold to minimize noise hits and maximize MIP efficiency







Power pulsing – Voltage stability



- DC voltage shift of ~4mV ok for tests, to be looked at for 6 HBUs (~80mV)
- Higher AC shift, if Tantal is further away

  → Thin 33µF Tantal available to mount near ASICs on HBU
- Plans:

  → Understand DC shift

  → Signal performance of SiPM + ASIC + Power pulsing

  → Plan and measure supply chain: ASIC → HBU → DIF → PWR