University of Glasgow | Experimental Particle Physics

The LHCb Velo Upgrade

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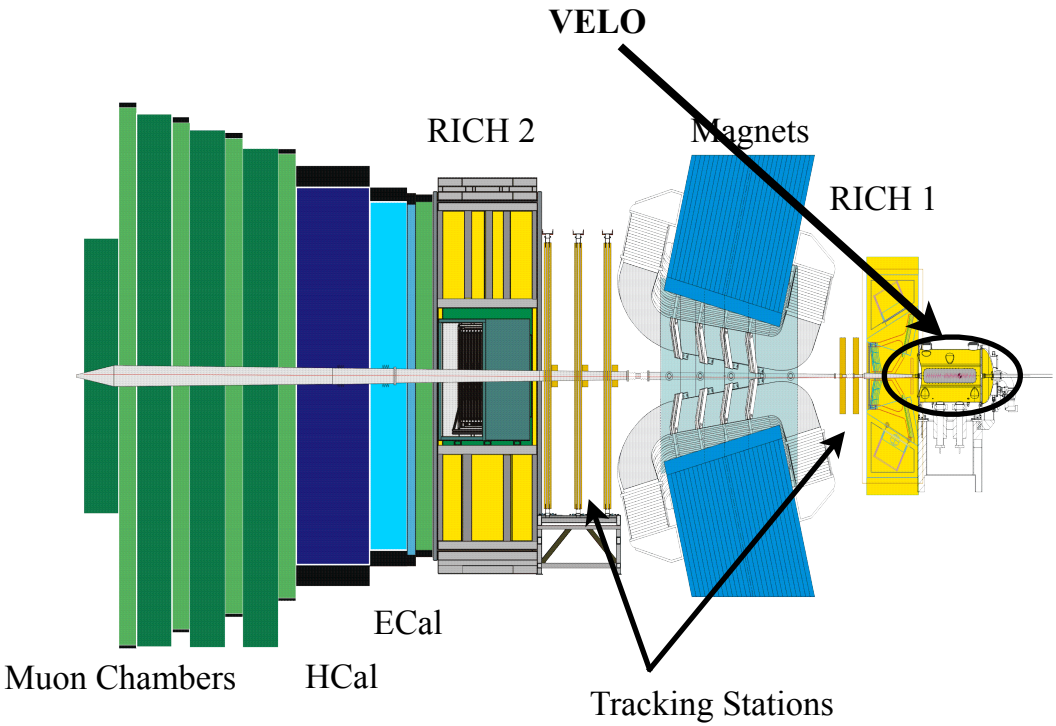
On behalf of the LHCb Velo Group

LHCb at a glance....

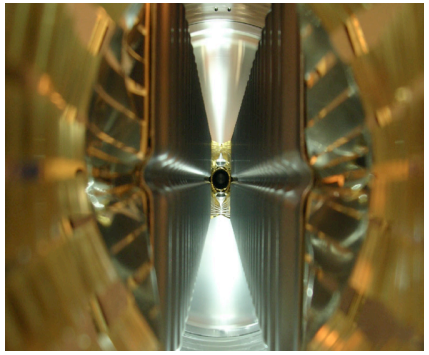
- Heavy flavour physics experiment at the LHC
  - Studies of b- and c-quark decays, New physics via CP violation, rare decays....
- High correlation of b-quarks in rapidity => forward arm spectrometer design
- b-quark mesons typical decay length ~ 1cm => vertexing critical to identify PV

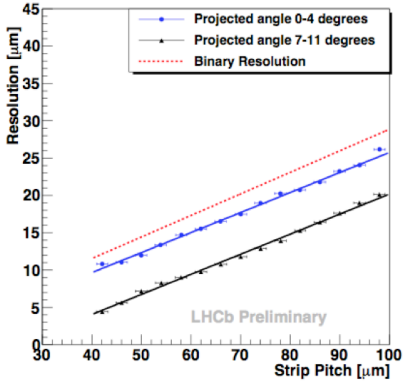
- Main requirements/features:
  - Excellent vertex resolution
  - Excellent PID
  - Efficient triggering and tracking



The VErtex LOcator

- Silicon strip detector with back to back modules - strips in radial and angular directions
- Highest resolution vertexing at LHC!
- Demanding requirements
  - Proximity to proton beams (7mm)
  - High radiation environment
  - Detector sits in vacuum
  - The whole thing **moves.....**



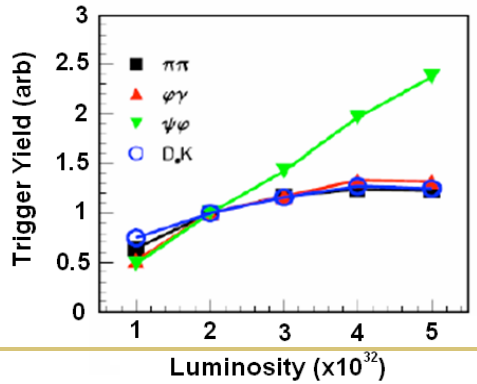


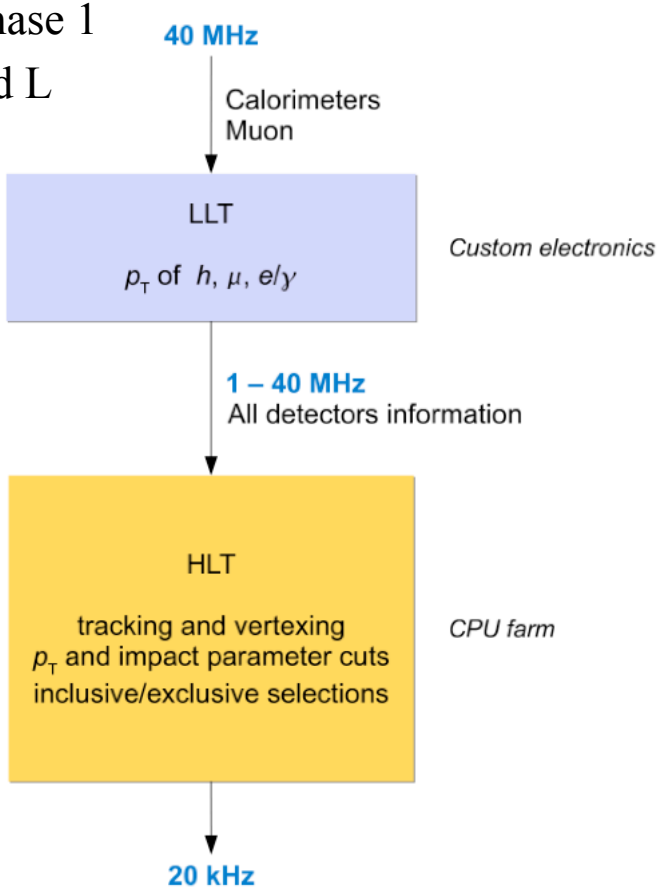
- n^+- implanted n-type sensors (1 n-in-p sensor!)
- Proper time resolution ~ 40 fs
- IP resolution ~ $13 + 25/p_T$ μm

See talk by T.Latham

Beyond the current detector...

- Primary physics goals of LHCb based on ~ 5 fb^{-1} of data - Phase 1
- Beyond this point will be statistics limited - aim for increased L
- Current detector runs at ~2×10^{32} $cm^{-2}s^{-1}$ luminosity
  - Maximum luminosity limited by L0 **trigger**!
  - Current L0 hardware trigger runs at 1 MHz
- Simply increasing luminosity not enough
- Read out the detector at 40 MHz.....
  - Trigger in software
  - Increase from ~2×10^{32} $cm^{-2}s^{-1}$ to 10^{33} $cm^{-2}s^{-1}$
  - ~double efficiency in hadronic modes

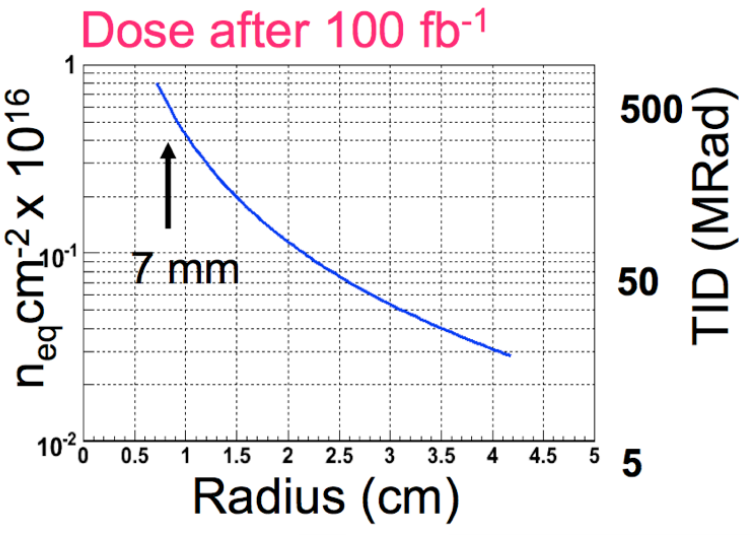




See talk by A.Gallas

Moving Velo into the future

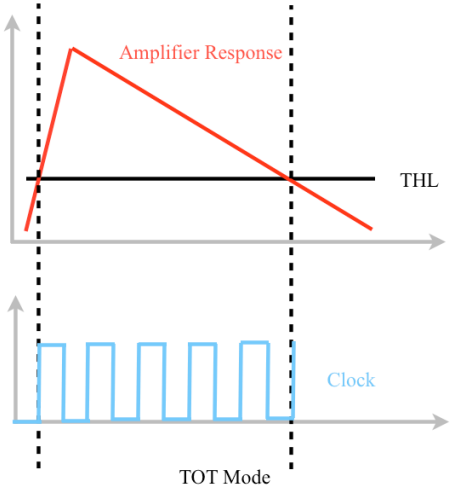
- Current Velo not suited to upgrade scenario
  - 40 MHz readout
  - Radiation tolerance (thermal runaway)
- Large parts of the current Velo can be kept:
  - CO_2 cooling plant
  - Mechanics
  - HV and LV systems



- However.....
  - Silicon modules must be replaced - rad. hard to > 5×10^{15} 1 MeV $n_{eq}cm^{-2}$
  - FE electronics upgraded to 40 MHz readout
  - New module geometry => new RF foil design
  - Aim for low occupancy

ASIC baseline - Timepix

- Development from Medipix collaboration
  - Return to HEP from medical physics
  - Velopix, Clicpix, Time projection chips.....
- Pixel ASIC with shutter-based readout
- 256 × 256 pixel matrix with 55µm pitch

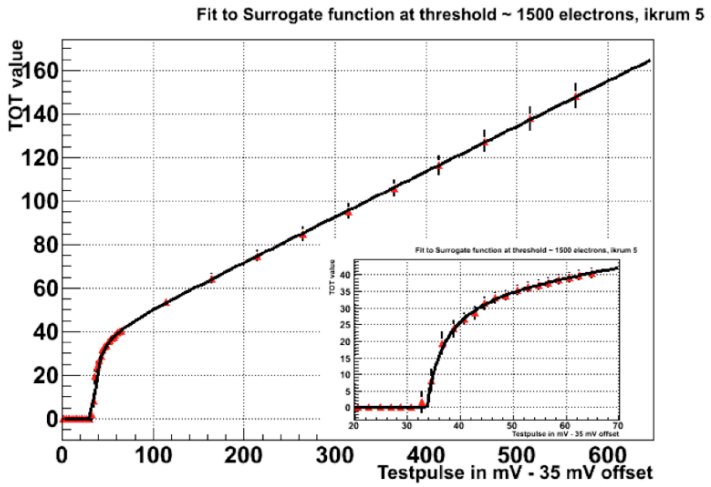


- Several operating modes:
  - Particle Counting (Medipix)
  - Time of Arrival (TOA)
  - **Time over Threshold (TOT)**

From Timepix to Velopix

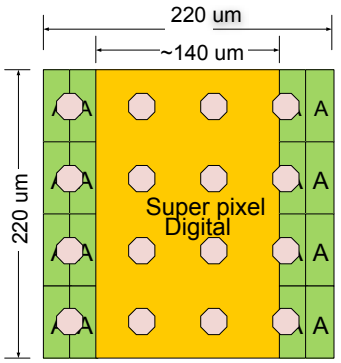
- Much more stringent requirements on Velopix
  - Replace shutter based readout with data-driven (ZS) readout
  - Reduce timewalk < 25ns (1000e^-)
  - Include TOA **and** TOT
  - Lower (~500e^-) threshold
  - Reduced non-linearity near threshold
  - Cope with anticipated particle flux in the upgraded LHCb
  - Keep data loss < 0.5%
  - **Data rate critical!!**

- An ambitious project! Still much to do....
  - Main constraints will be power and data flow



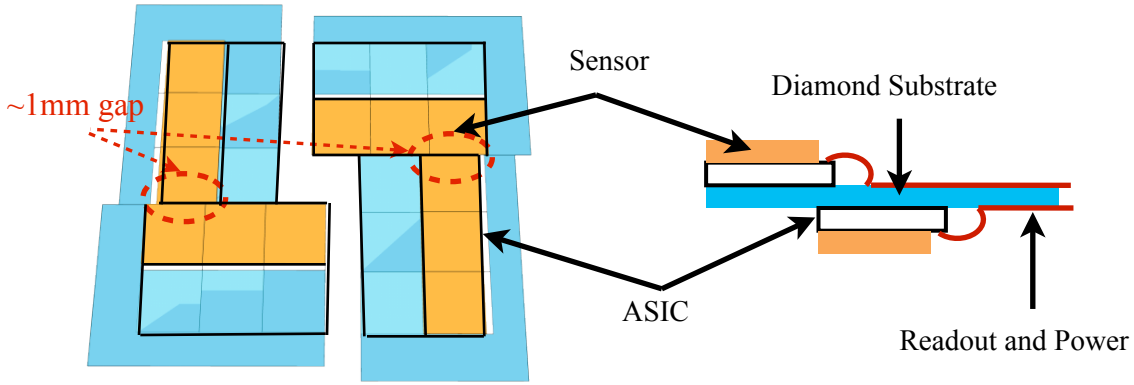
Data rates

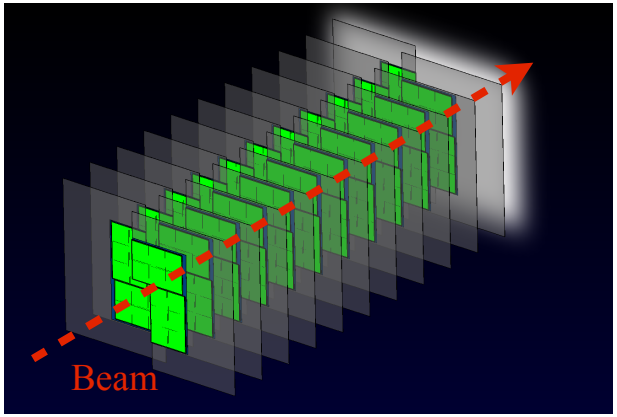
- Particle rate for chips closest to beam ~ 6 particles / bunch crossing
  - Average 2 pixels per hit, 32 bits per pixel read out (16-bit ID, 12-bit BCID, 4-bit TOT)
  - $6 \times 32 \times 2 \times 40$ MHz gives data rates of almost 15 Gbit s^{-1}!!
- Biggest challenge to Velopix - manageable data flow!
- Super Pixel Packet format proposed - group together clusters of 4×4 pixels to create Super Pixels
  - Share time-stamping information (crossover of digital regions)
  - Save ~ 30% bandwidth
  - Still requires several multi-gigabit readout links
- Challenge to divide work between FPGA readout and ASIC logic
- Current questions:
  - Can we specify stream sizes to reduce workload on DAQ system?
  - How much information should we decode for trigger pattern recognition stage?
  - Is it worth making life difficult on-chip? Yes, power needs to stay < 1 W/chip



Proposed module design

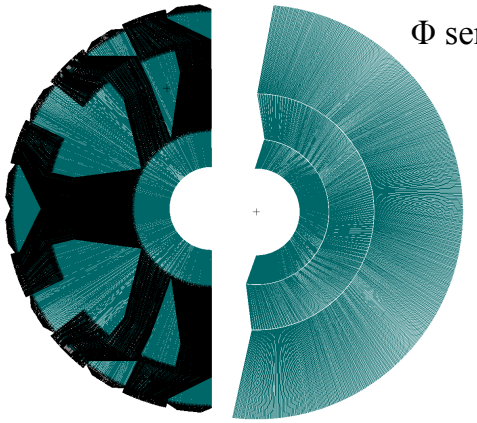
- Each Velo half to consist of 12 ASICs in 2 staves
- Each stave consists of:
  - CVD diamond support structure (essential high thermal conductivity)
  - Front- and back-mounted tiles of 3 ASICs with sensors bump-bonded on top
  - Readout and power traces on the substrate
  - Minimise radiation length

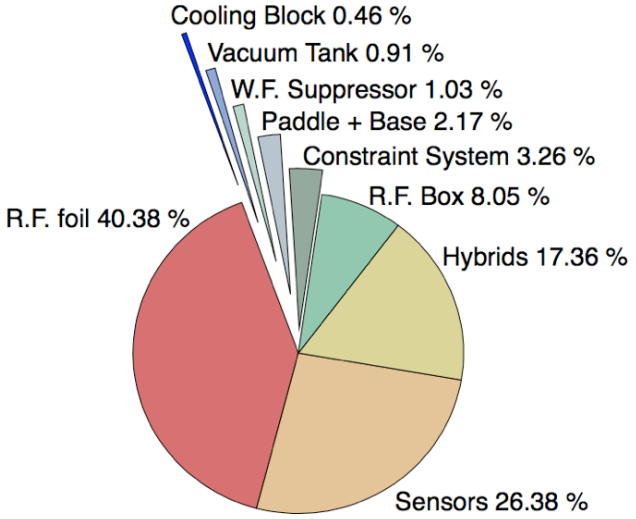




Strip sensor option

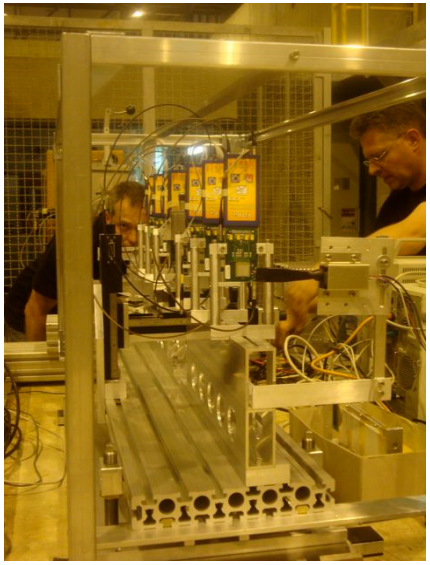
- Background development of strip sensor option
  - Should pixels exceed power/material restrictions
- Still challenging work to
  - Keep strip capacitance low
  - Increase number of strips - aim for occupancies < 0.5%
  - Radiation hardness and performance - n-on-p sensor baseline
  - 40 MHz readout chip still to be developed, overlap with LHCb Silicon Tracker upgrade program
  - Reduce X_0

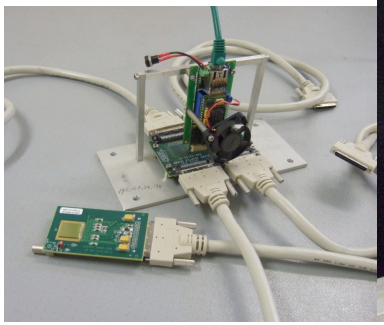


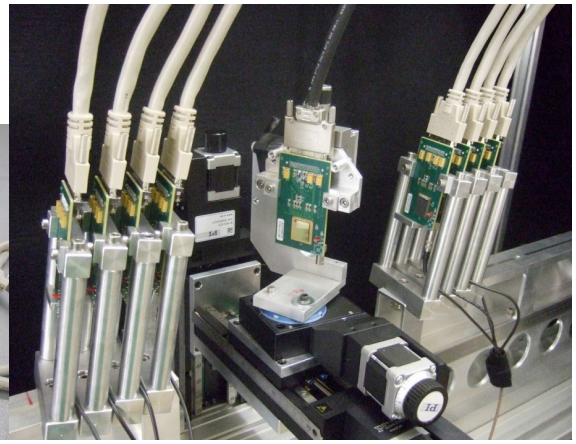


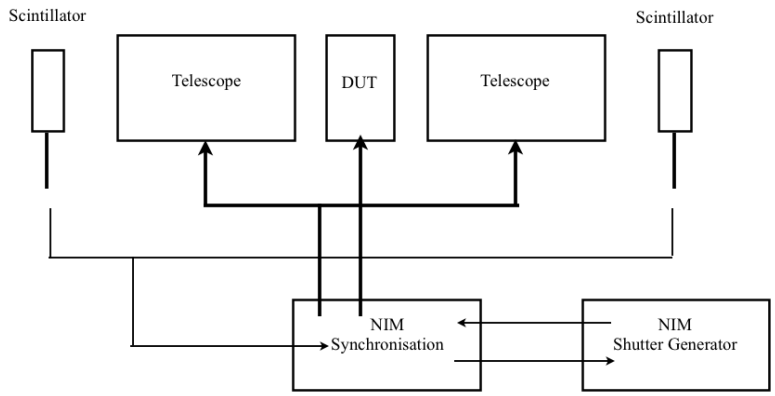
Timepix telescope

- 8 telescope planes, 7 in TOT mode and the other in TOA
- NIM crates providing shutter logic (coincident scintillator hits)
  - 40MHz-synchronised triggers
- FPGA based readout - RELAXd
- From “what if....?” to world class telescope in less than a year!
  - ~1μm resolution at device under test
  - ~1ns timestamp
  - > 5 kHz track rate







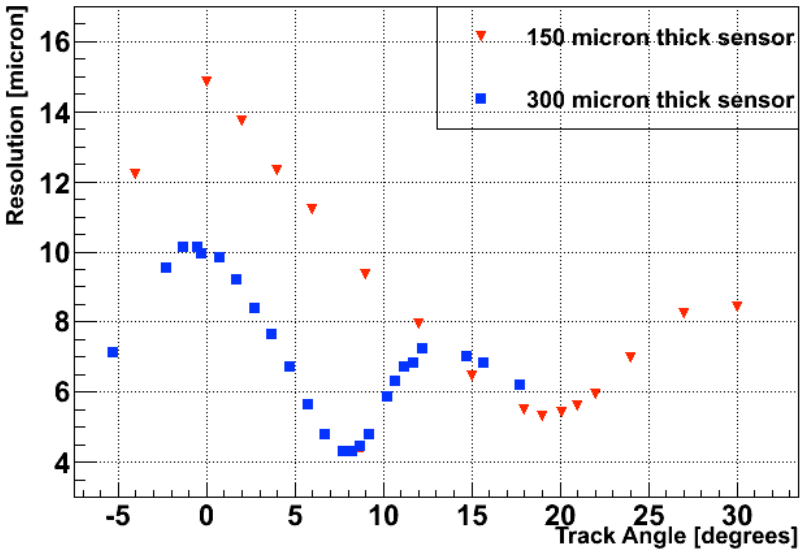


2009 + 2010 data already published (more to come!) http://arxiv.org/abs/1103.2739

Timepix for tracking

- Timepix performance comparable to current Velo sensors
- Resolution with TOT better than binary resolution (aim for min. 4 bit TOT)
- Extensive studies on charge sharing
  - Angular dependance of resolution
  - HV dependence
  - Sensor thickness

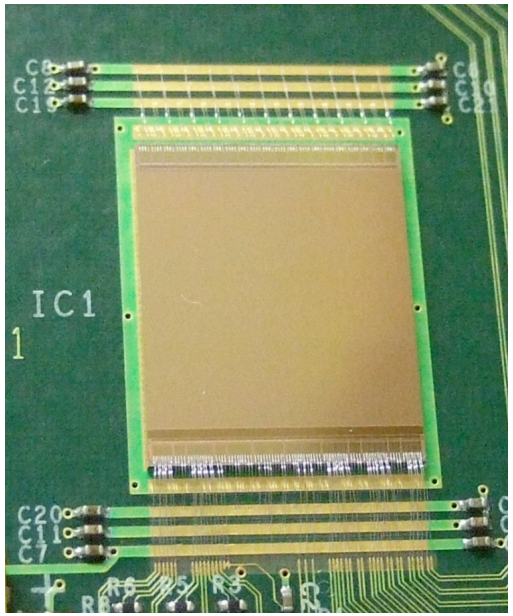
Resolution versus Incident track angle



Looking to the future...

- Latest chip from Medipix collaboration - Medipix3
  - Similar to Medipix2 - no TOT, TOA
  - 2 threshold counters per pixel, *limited* charge discrimination
    - Group 4 pixels together to gain 3 bit TOT!
  - Radiation hard, 130nm process => sensor irradiation studies!
- Next step (submission ~end of 2011) **Timepix3**
  - Simultaneous TOT and TOA
  - Analogue FE identical to Velopix requirements
  - Real prototype production and testing
- Many irradiated sensor studies planned for this year
  - n-on-p
  - Double sided 3D
  - Diamond sensors
  - Guard ring designs
- Finalise decisions about Velopix architecture!

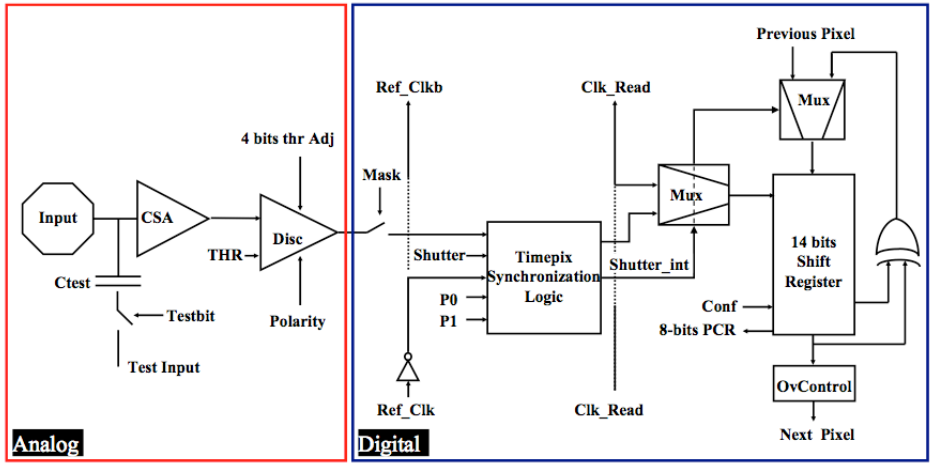
See talk by A.Mac Raighne



Summary

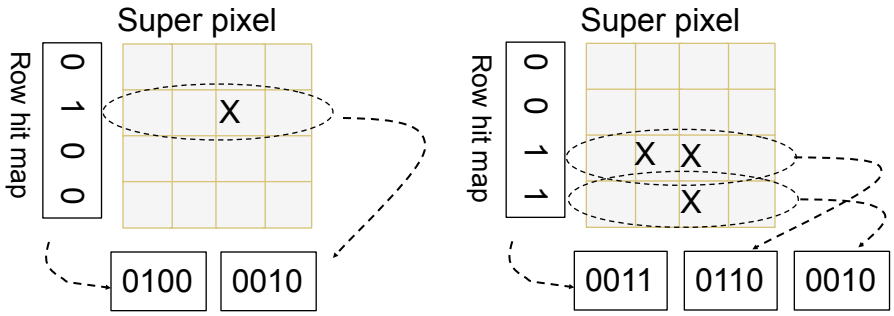
- Velo upgrade program well advanced and ambitious
- Velopix baseline pixel ASIC, strip option still realistic alternative
- Challenges “manageable” (ask us in 2 years!!)
  - Radiation hardness comparable to requirements on other LHC experiments
  - Power consumption must be kept low
  - Data rates must be fine tuned and workload sensibly distributed
- Project independent of LHC upgrades!

Backup

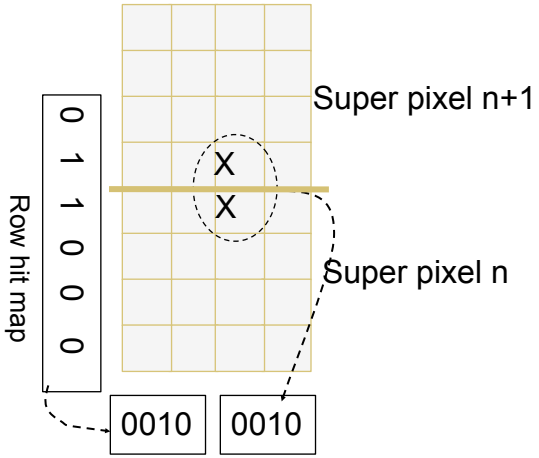

Analog
Input
CSA
4 bits thr Adj
Disc
THR
Ctest
Testbit
Polarity
Test Input
Digital
Ref_Clkb
Clk_Read
Previous Pixel
Mux
Mask
Mux
Shutter
Timepix
Synchronization
Logic
Shutter_int
14 bits
Shift
Register
P0
P1
Conf
8-bits PCR
OvControl
Ref_Clk
Clk_Read
Next Pixel

Data reduction schemes

- Unformatted:
  - 16 bit pixel address
  - 12 bit bunch ID
  - 4 bit TOT
  - 32 bits per pixel!

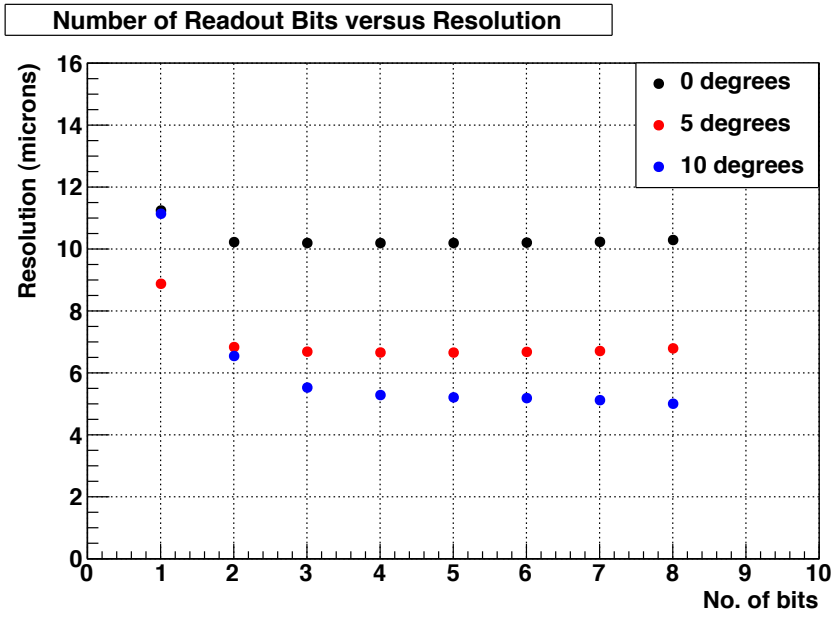


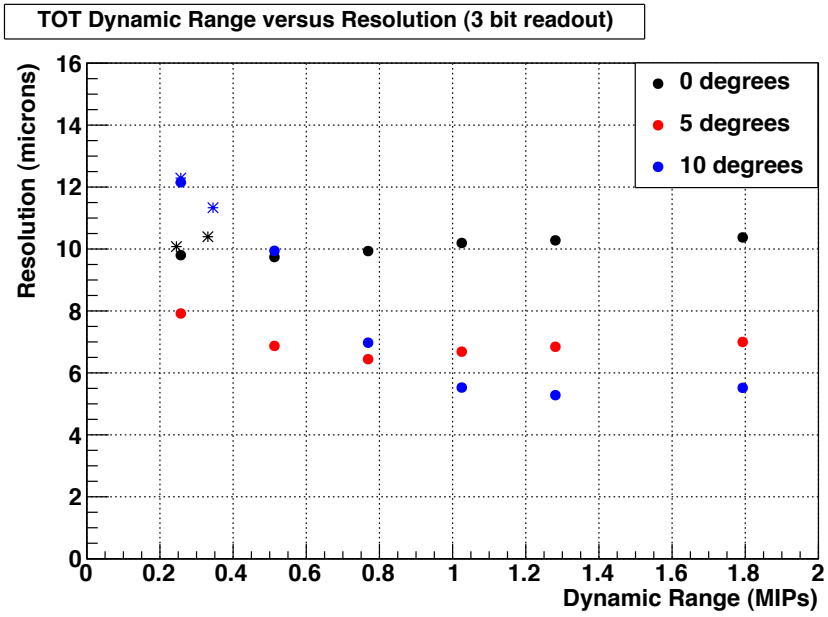
- Using SPP format:
  - Fixed 30 bit header (BCID, super pixel ID, row hit map)
  - Variable length column hitmap with TOT
  - Share information across row boundaries of super pixels
  - Bandwidth reduction ~ 30%



Design lessons for Velopix

- For single hit clusters no need for TOT
- On multi-pixel clusters TOT essential for accurate reconstruction
  - Study into TOT requirements for Velopix front end
  - Necessary to tune preamplifier response, etc.





Bias voltage