Design and verification of an FPGA based Bit-Error-Rate-Tester

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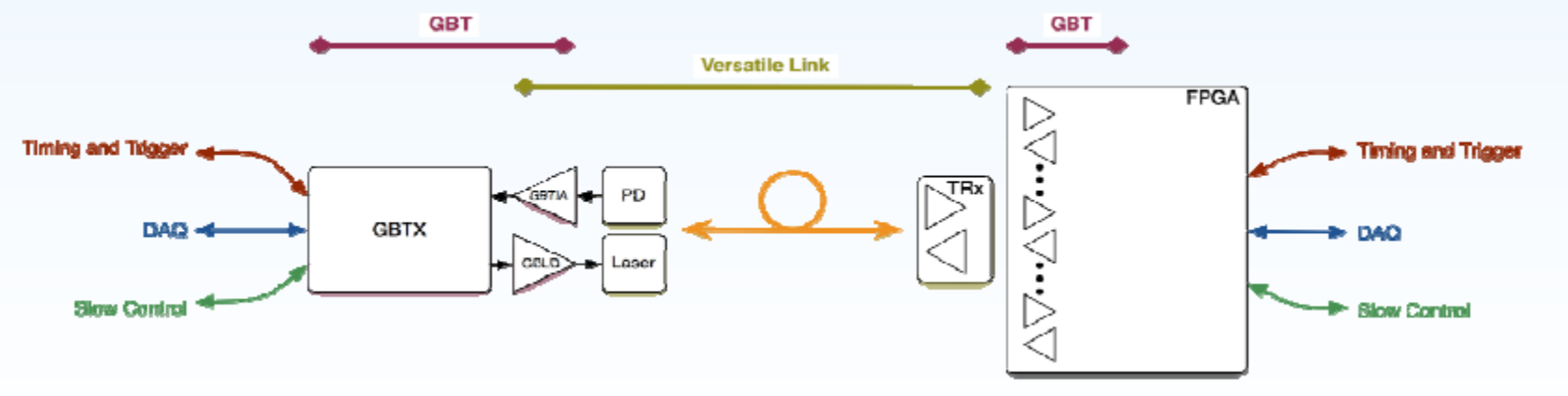
Outline

- Introduction
- FPGA platforms
- Transceiver characteristics
- BERT architecture
- Test setup and results
- Updates and availability
- Summary

Introduction

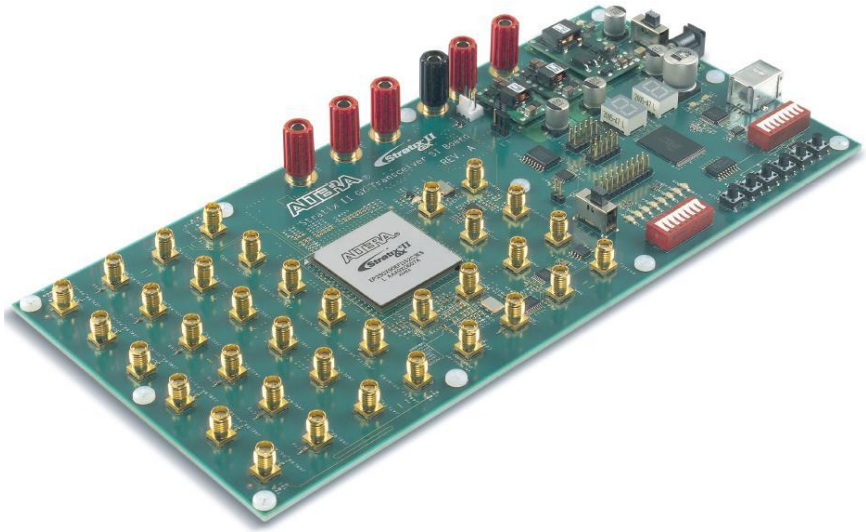
- Background of study
  - Multi-gigabit per second serial optical links are widely proposed to support data transmission in particle physics experiments.
  - Bit Error Rate (BER) testing is the fundamental measurement of the integrity of each digital communication link.
  - A system demonstrator is conceived for the Versatile Link project which develops a high speed radiation tolerant optical link for LHC upgrade.



Introduction (2)

- Motivation and application
  - With the integration of high-speed transceivers inside an FPGA, the embedded BERT solution provides a cheaper alternative to traditional stand alone test equipment.
  - FPGA based test bench can be easily customized to verify system design, protocol implementation and link interoperatibilty.
  - The compact evaluation kit can be used both in the laboratory and in a radiation environment (with proper shielding).

FPGA platforms

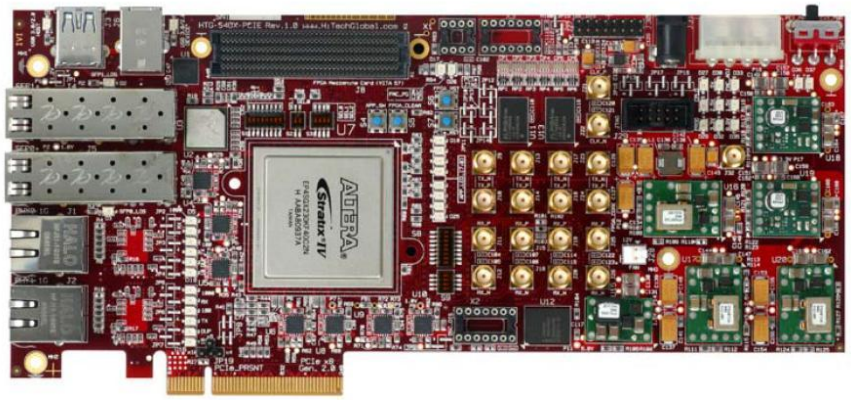


- Altera Stratix II GX transceiver signal integrity development board features:

- Altera Stratix II GX EP2SGX90 device
- Six duplex transceiver channels at up to 6.375 Gbps each channel via on board SMA connections
- USB connection as serial port to communicate to host PC
- General user access (header, LEDs, push-buttons) for easy control, monitor and debug

- The Stratix II FPGA device available in production today, but the development kit is updated to Stratix IV edition

FPGA platforms (2)



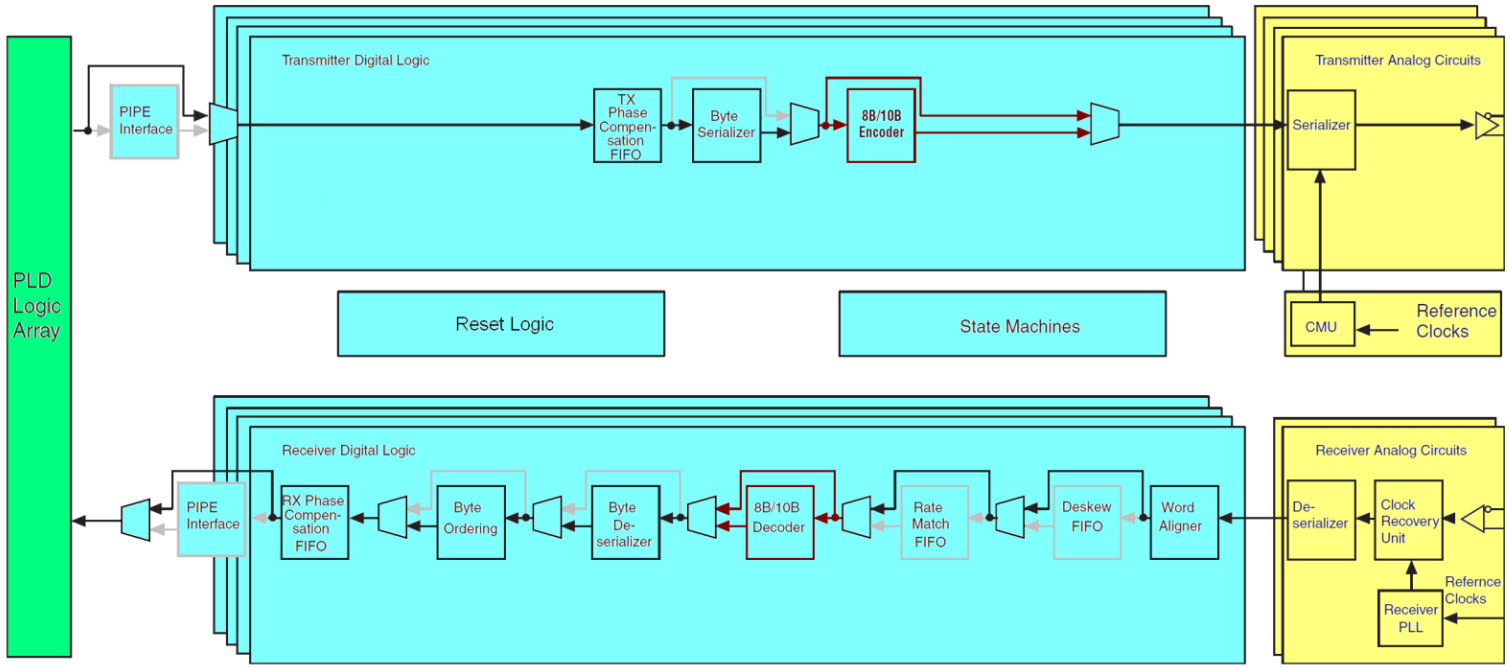
- HiTech Global Stratix IV GT development platform features:

- Stratix IV GT EP4S100G2 device
- Twenty-four duplex transceiver channels at up to 11.3 Gbps each channel
- Four of which are via on board SMA connectors

- High speed FMC (field programmable mezzanine card) for hosting custom modules (8 transciever, 60 LVDS and clocks)
- One x8 PCI express Gen 2 edge connector, USB3.0/2.0 host and device and two gigabit Ethernet ports
- Two SFP+ (including dual channel EDC chip) hosts

Transceiver Characteristics

- Altera FPGA transceivers incorporate dedicated embedded circuitry that supports many serial data communication standards (PCIe, SONET, XAUI, Gigabit Ethernet etc.)
- Basic mode is configured here in the custom BERT for simplicity and flexibility.
- 8B/10B encoding is studied as a demonstrative protocol (not available in 11.3Gbps rate).

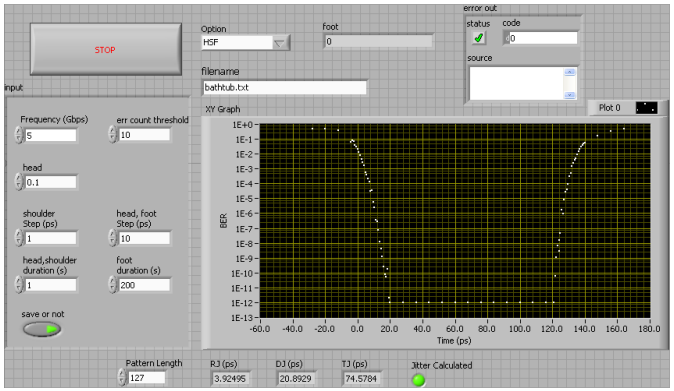


Transceiver Characteristics (2)

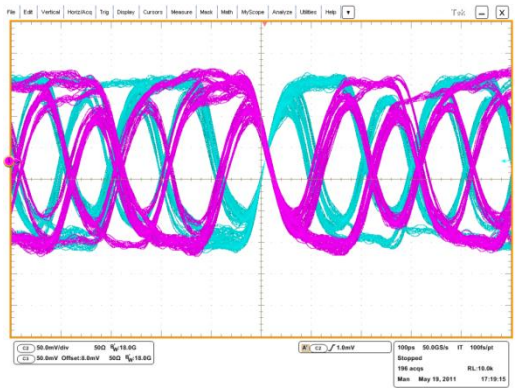
- Transceiver signal integrity are characterized at the basic configuration. The results demonstrate good performance and are compliant to 4GFC and 10GbE requirements.
  - Transmitter eye diagram
  - Transmitter and commercial BERT receiver bath tub scan
  - Receiver sensitivity via reference optical link
  - Transmitter jitter transfer and receiver jitter tolerance

OTx output, 5Gb/s

Bath tub scan

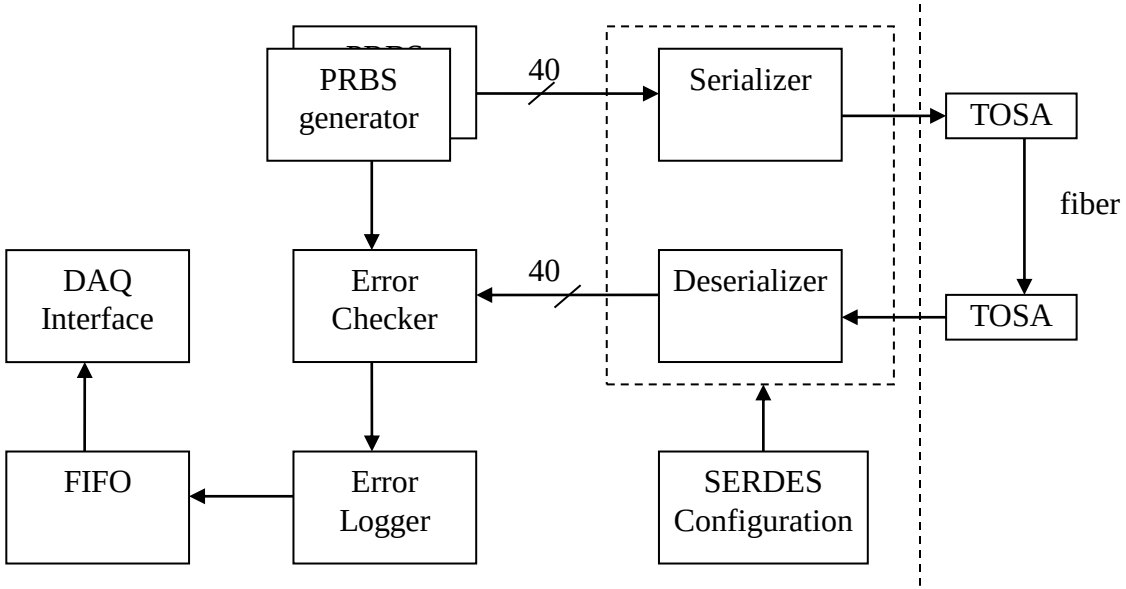


OTx output, 10Gb/s



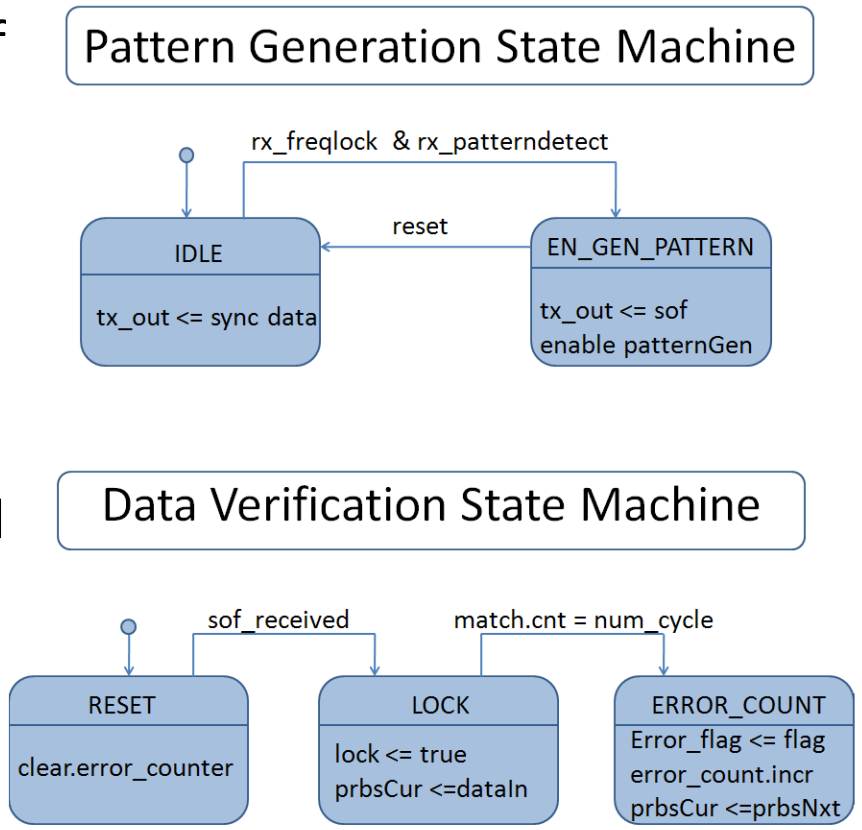
BERT architecture

- The custom firmware is developed in VHDL and PC interface developed in LabVIEW
  - PRBS generator, error checker, error logger function blocks are platform agonistic
  - Transceiver instantiation configure in basic mode
  - User interface optimized for high throughput (UART bulk mode)



BERT architecture (2)

- The PRBS generator produces long stress patterns without using a lot of memory (PRBS7, 15,23,31 are implemented)
- The PRBS detector self-aligns to incoming bit streams without needing the receiver to acquire boundary alignment.
- The detector switch from incoming bits to locked internal seeds to avoid transient disturbance.
- Link reset can be initiated from transmitter or receiver individually.



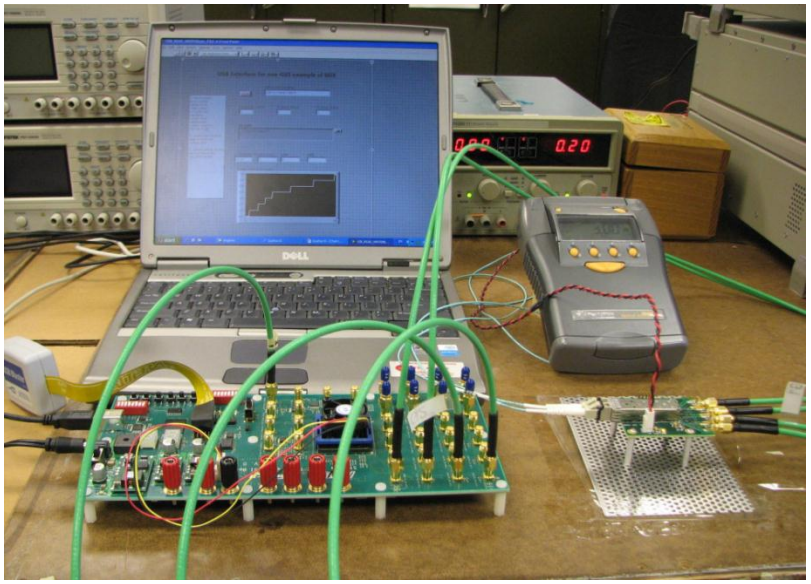
BERT architecture (3)

- The error logging FIFO records both bit error data and link status data for in situ process and offline analysis.
- Recorded time stamp and XOR pattern of received and expected data can reproduce transmitted and received data, given known PRBS.
- When a link event occurs, it is always time stamped and logged in the reserved portion of the FIFO.
- The FIFO is set to 4K in length, 12 bytes in width per transceiver channel. About 35% of on device memory are used for the total of 4 channel. The USB interface achieves a throughput of 5Mbps in bulk mode.

Event	Event flag	Time stamp	Event data	Note
SEE	001	48bit	XOR	
Locked	010	48bit	Exp'd data	Error detector locked to generator
Link Lost	011	48bit	Exp'd data	Receiver CDR lost synchronization
FIFO Full	100	48bit	Exp'd data	Stop recording SEE events
FIFO Ready	101	48bit	Exp'd data	Resume recording SEE events

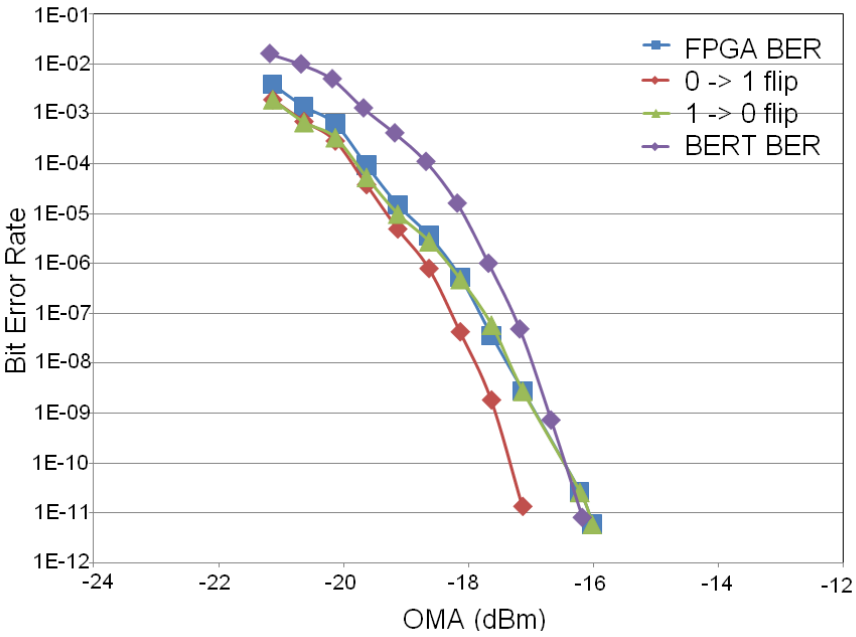
Test setup & results – s2gx

- The BER tester is demonstrated on a point-to-point optical link.
- 156.25 MHz on board oscillator provides frame clock. Jitter performance limited by internal PLL.
- SFP+ optical transceiver is driven by the BERT at 5Gbps.
- Variable optical attenuator is inserted in the fiber loop to provide signal stress.



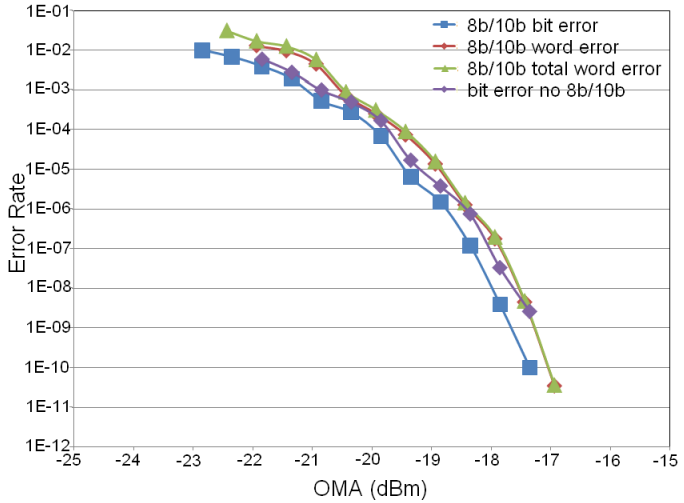
Test setup & results – basic BER

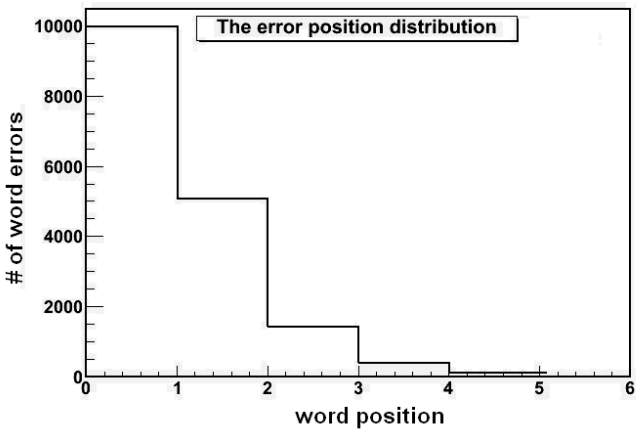
- BER vs. optical modulation amplitude is measured.
- With the same reference link, measurement results are comparable between FPGA BERT and commercial BERT.
- More one-to-zero bit flips than zero-to-one bit flips are observed at lower error rate, possibly due to the post amplification circuitry of the optical receiver that favorites one state over the other.



Test setup & results – 8B/10B coding

- The 8B/10B coding is used by many protocols to achieve DC balanced data stream; sufficient level transitions; and unique code groups.
- The Statrix devices support two dedicated 8B/10B encoders in each transceiver channel and they can be cascaded.
- A single bit flip can affect single bits or spread into multiple code groups.
- Test results confirms that there are more word errors that bit errors.
- Simulation shows that error propagation is quickly stopped.

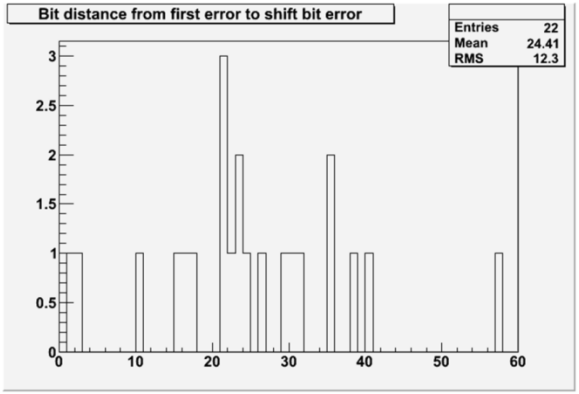




Test setup & results – SEE analysis

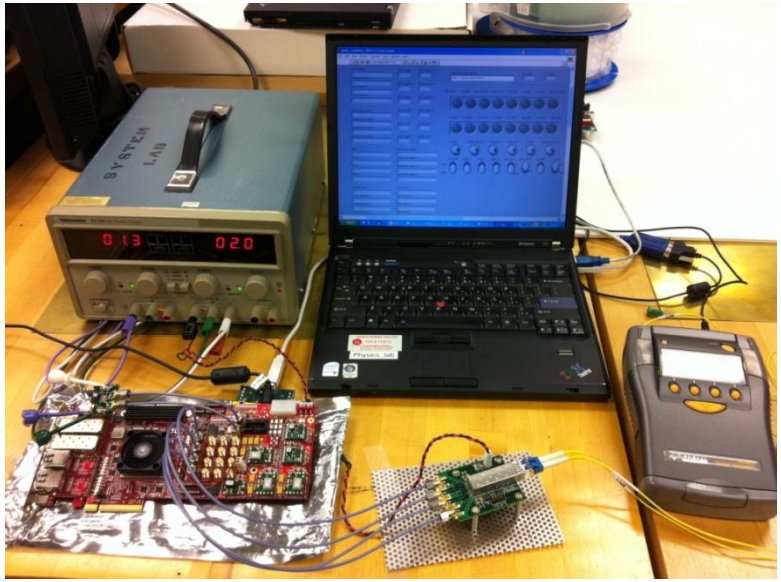
- The BERT is deployed in a radiation test on a 5 Gbps customer serializer chip (LOCs1) with a 200 MeV proton beam at Indian University Cyclotron Facility.
- Parallel PBRS data were injected to the serializer and data output were feed to the BERT receiver channels.
- Two serializer boards were placed in the beam and the rest of the system in shielded area.
- Post-test analysis shows that two types of SEE events occurred during high flux irradiation run: single bit flip and single bit shift.
- Error bursts that render bit shift are constrained within two frame clocks.

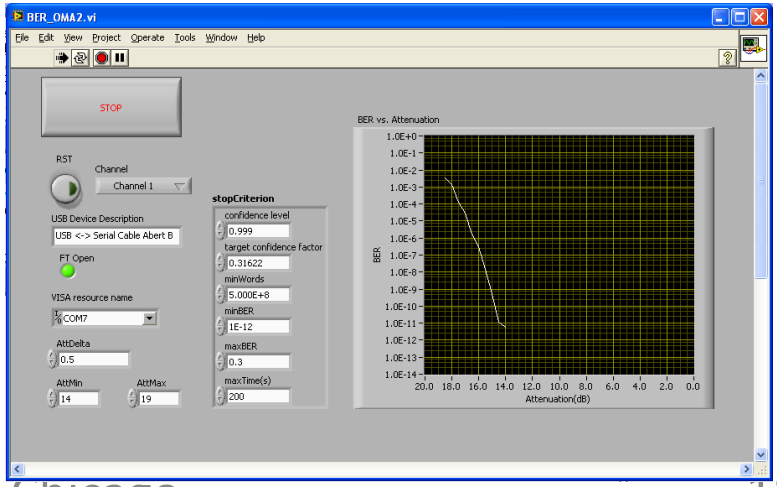
Error Type	Synchronization Error		Single-Bit Error	
Module ID	6	12	6	12
Number of errors	8	17	5	0
$\sigma(cm^2)$	3.4×10^{-14}	7.3×10^{-14}	2.1×10^{-14}	4.3×10^{-15}



Test setup & results – s4gt

- A clock oscillator module off board provides reference input. Jitter performance limited by internal PLL.
- Transceivers instantiate in low latency basic mode to support highest data rate.
- Error free over 2 hours achieved in back to back optical link at 10Gbps.
- BER vs. OMA measured with automated LabVIEW routine.





Updates and Availability

- Reference designs are available for interested users. Please email to request the IP suite and documentation (cxiang@smu.edu).

- Ten duplex channel FMC mezzanine implementation will be benchmarked in the near future.

- Data acquisition user interface will be implemented on more interfaces such as Ethernet and high-speed serial port.

Summary

- A customized Bit Error Rate test bench using an FPGA with embedded transceiver is demonstrated and characterized.
- The test bench deploys basic PHY configuration, PRBS generator and error detector, advanced error logging FIFO and optimized user interface.
- Customized testing are implemented to facilitate system verification, error analysis and irradiation testing.

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Thank You!