



The Data Acquisition System for the KOTO Detector

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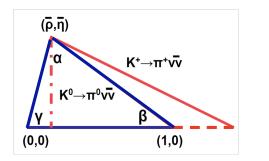


KOTO Physics



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KOTO (K⁰ at Tokai) aims at discovering the FCNC $K_L \rightarrow \pi^0 v v$

- Forbidden at tree level $BR(K_L \rightarrow \pi^0 vv) = (2.43 \pm 0.39 \pm 0.06) \times 10^{-11} z^0$ (PRD 83, 034030, 2011)
- Dominated by heavy particle loops which can be calculated in perturbation theory at 2-3%
- Direct CP violating process $\propto \eta^2$ (height of CKM unitarity triangle)
 - \Rightarrow CKM "Golden Mode", very sensitive to new physics

Present limits are:

1) From E391a @ KEK (PRD 81, 072004, 2010) BR($K_L \rightarrow \pi^0 vv$) < 2.6 × 10⁻⁸ (@ 90% CL)

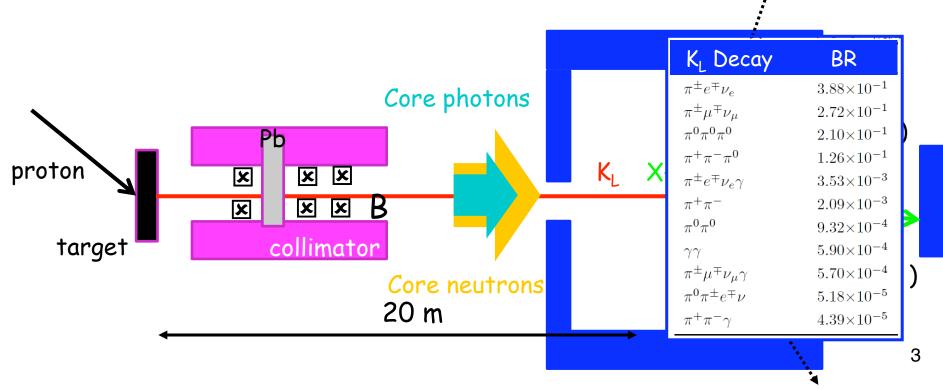
2) from E949 @BNL, which measured $BR(K^+ \rightarrow \pi^+ \nu \nu) = (17.3 \pm 11.0) \times 10^{-11}$ + isospin symmetry relation (Grossman-Nir bound) (*PRL 101, 191802, 2008*) $BR(K_L \rightarrow \pi^0 \nu \nu) < 1.5 \times 10^{-9}$ (@ 90% CL)





KOTO detects $K_L \rightarrow \pi^0 \nu \nu$ decays by looking for the two photons from the $\pi^0_{.}$ Improves on experimental method pioneered by KEK-E391a.

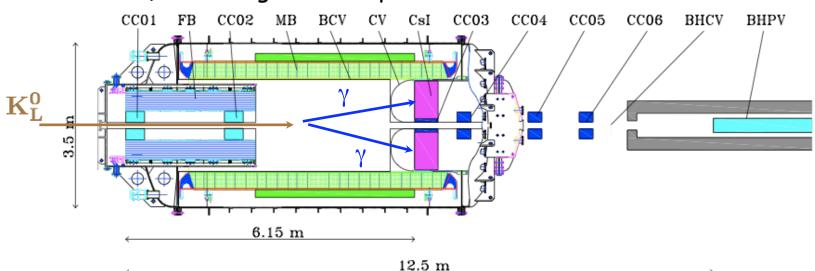
- 1. Dedicated beam line for clean pencil-size K_L beam to minimize halo particles and constrain K_L decay vertex
- 2. High acceptance detector for photons, highly segmented to reconstructed separate clusters
- 3. Hermetic veto for photon and charged particles







KTeV CsI calorimeter (~3000 channels) plus charged/neutral vetos (~1000 channels) inside high vacuum pressure vessel



- About 65 collaborators from 15 institutions (Japan, US, Korea, Russia, Taiwan)
- Use 30-GeV Proton Synchrotron at J-PARC in Tokai, Japan
 - $2 \times 10^{14} \text{ POT} \Rightarrow 8.1 \times 10^{6} \text{ K}_{\text{L}}/\text{spill}$
 - spill length/repetition time 0.7s/3.3s
 - <P(K_L)> = 2.1 GeV/c for 16° extraction angle







Huge background rates from $K_L \rightarrow \pi^0 \pi^0$ require 1 MeV sensitivity for veto signal rejection. Also expected maximum photon energy deposition ~1.5 GeV.

⇒ with 10 cnt/Mev, 14 bit dynamic range for energy measurement

To minimize effect of accidental veto rejection, measure scintillation pulses with sub ns timing resolution.

To reach SM sensitivity, need to detect as many $K_L \to \pi^0 \nu \nu$ decays as possible.

 \Rightarrow Pipelined frontend and trigger to limit dead time

To limit cost:

Shape analog frontend signals and extract charge and time information with a single digitization.

Build trigger and readout around these shaped signals.







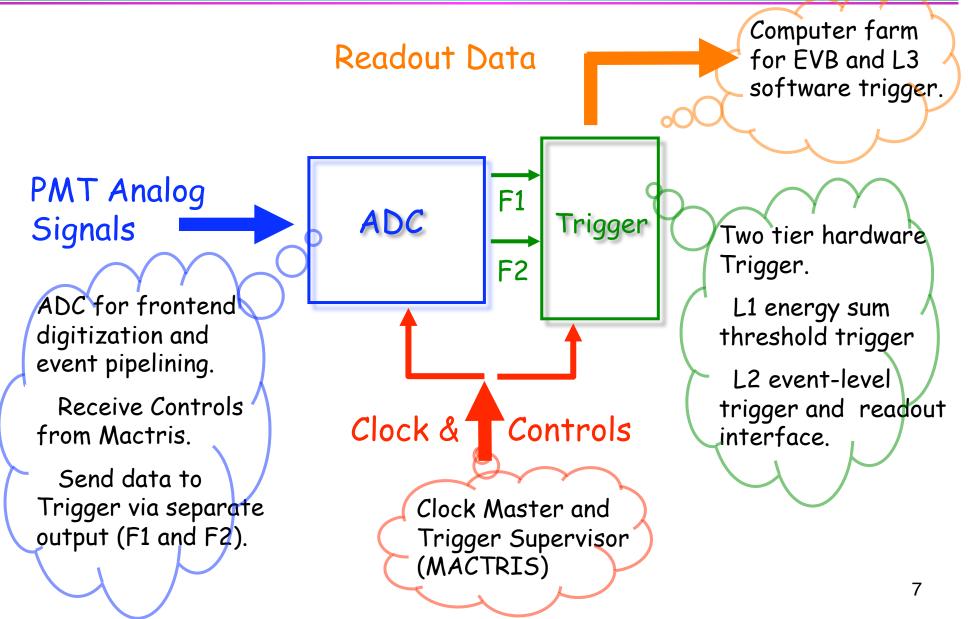
PMT Analog Signals

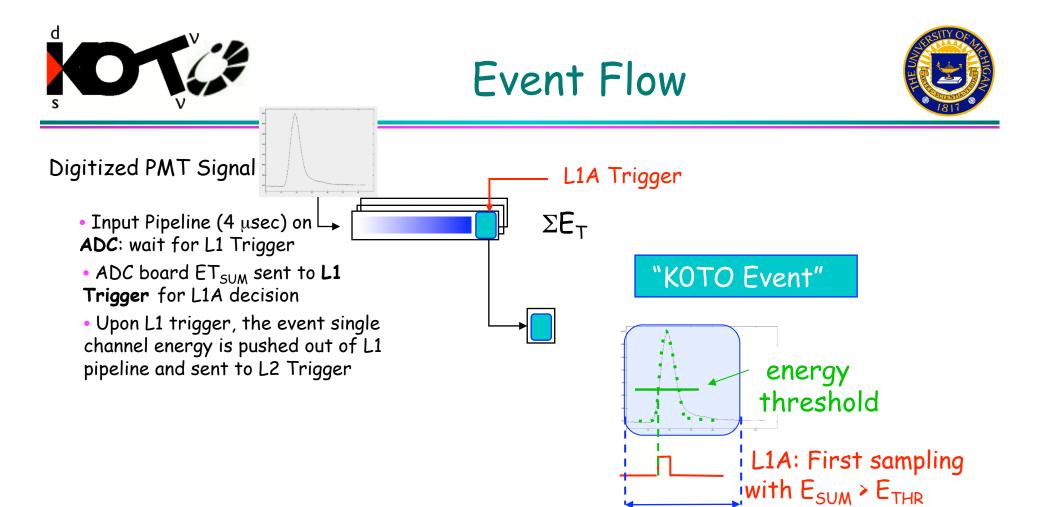




T&DAQ Architecture







Width: 40-64 samples





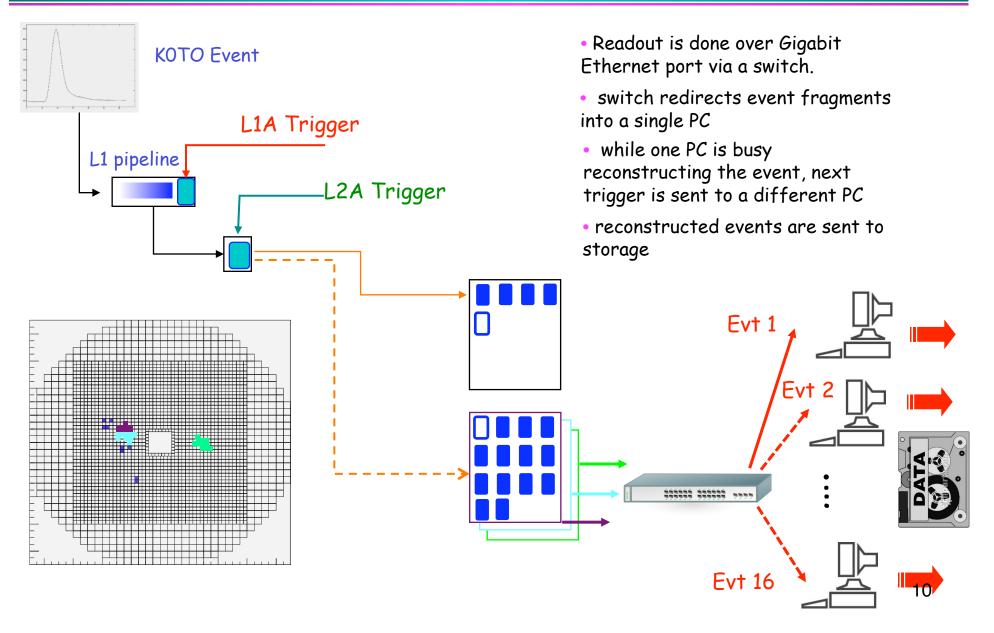


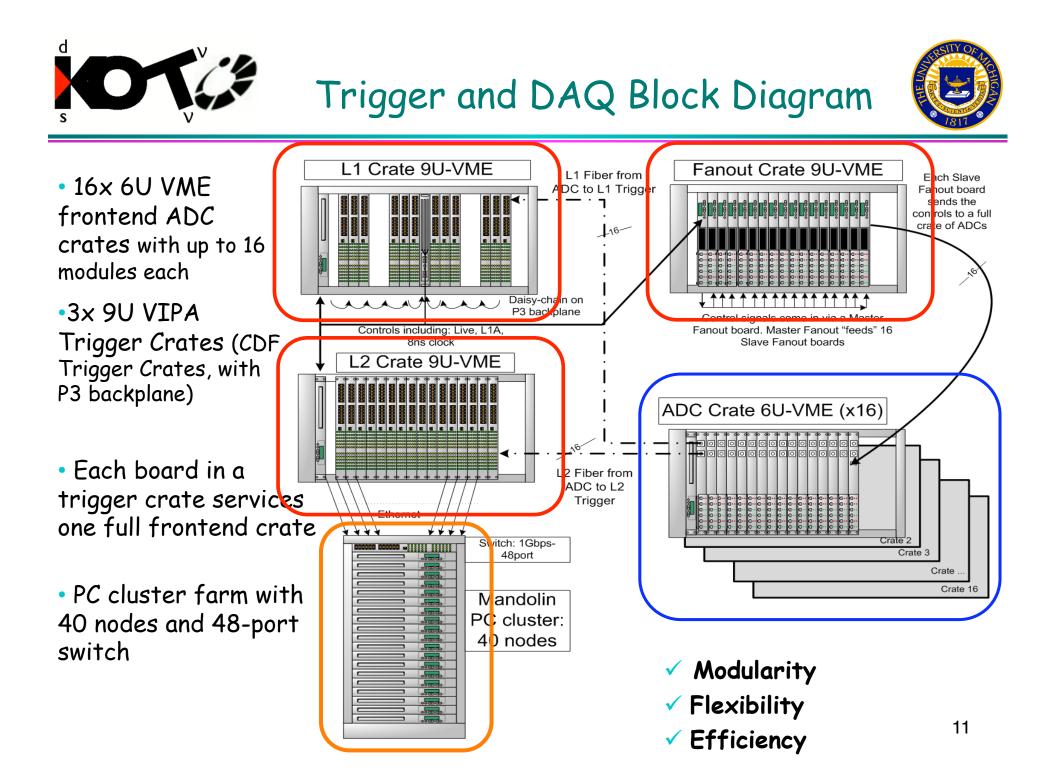
candidate of KL → π0 π0 π0_ Digitized PMT Signal L1A Trigger Input Pipeline (4 μsec) on ADC: wait for L1 Trigger L2A Trigger ADC board ET_{SUM} sent to L1 Trigger for L1A decision • Upon L1 trigger, the event single MEM 1 channel energy is pushed out of L1 pipeline and sent to L2 Trigger • L2 Trigger receives sequential events and for each issue a L2 accept/reject decision. WRITE Sequential L2A events are sent to one of two DDR2 2 Gb memories. Memories are alternatively in WRITE mode (for 0.7s spill) or READ mode (for 3.3s spill repetition time). With this scheme, we can reach READ 14 kHz L1 trigger rate (for 48 sampling trigger) with automatic L2A and no zero suppression. MEM 2



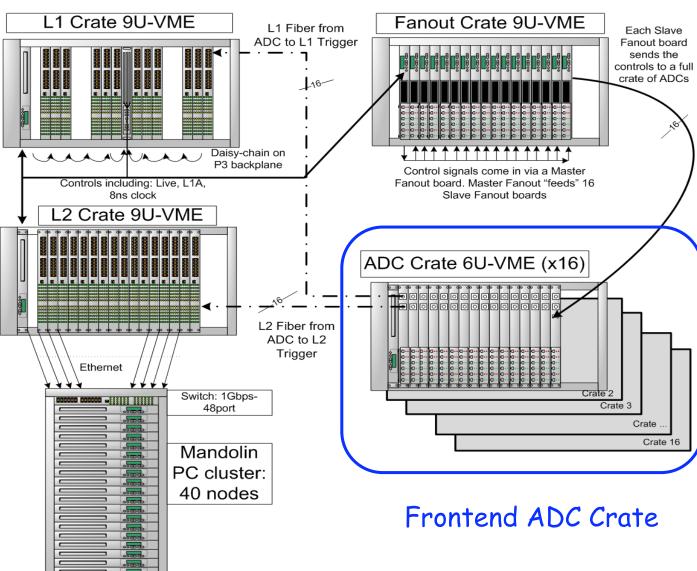










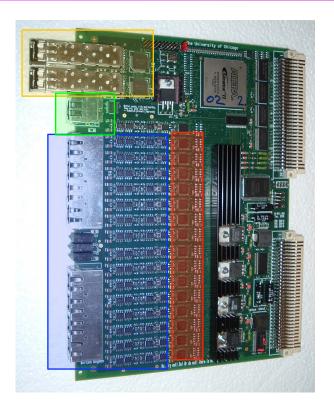


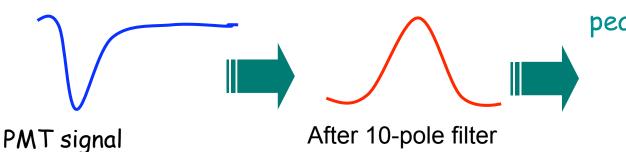


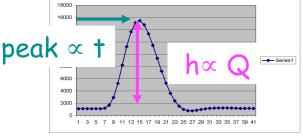




- (see Jiasen Ma's poster "A Pulse Shaping and Digitizing System with Subnanosecond Timing Resolution")
- 6U VME board with fully pipelined deadtimeless design
- 16 analog inputs are shaped by 10-pole Gaussian filter taylored to PMT pulse characteristics
- resulting 45ns FWHM gaussian shape is digitized with 125MHz/14 bit FADC (110 ps resolution for 200 MeV)
- Controls are LVDS signals via CAT6 cable
- Two 2.5Gbs transceivers via optical fiber driver for signals to L1/L2 trigger







After digitization



Trigger and DAQ Block Diagram

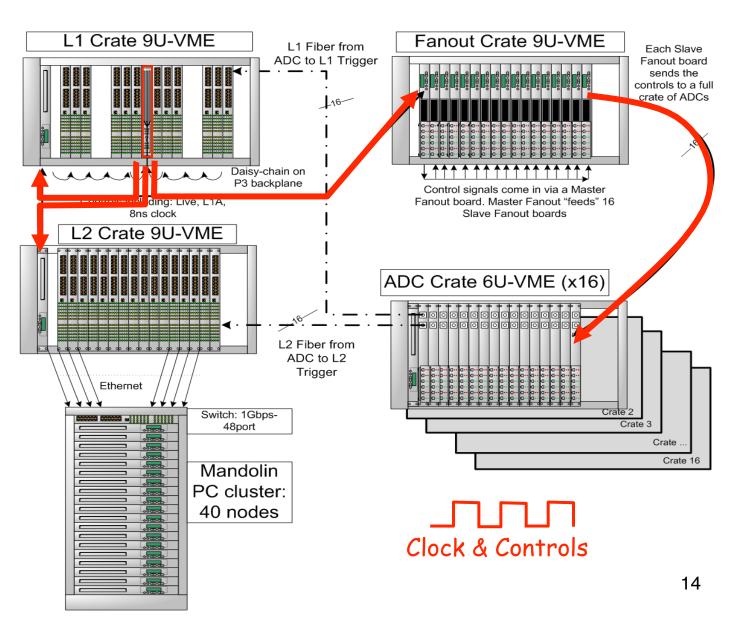


MACTRIS Master Clock and Trigger Supervisor Board

 oversees system integration

• sits in L1 Trigger crate at the end of ET_{SUM} daisy-chain

 connects to each crate in the system

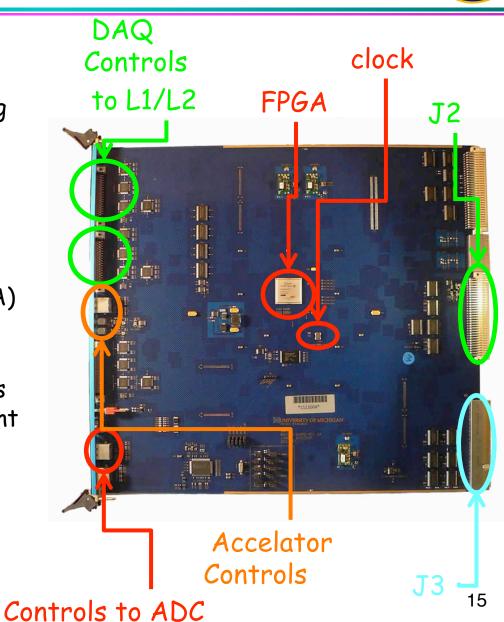




MACTRIS Board

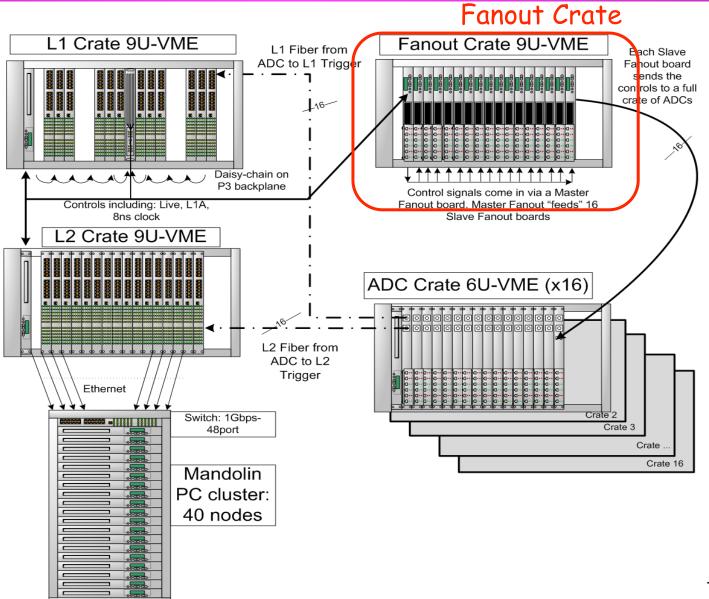


- generate 8 ns system clock
- generate system LIVE (beam gate defining t₀) plus L1A decision using programmable logic (on-board FPGA)
- receive daisy-chained ET_{SUM} from J3 backplane connector
- distribute Controls (clk, LIVE, L1A) as LVDS to ADC via RJ45 front panel port
- distribute clock and DAQ Controls to L1 and L2 crates via 68-pin front panel connector and inject them into P2 backplane (Slave Mactris)
- provide interface to accelerator signals via NIM/LVDS front panel ports







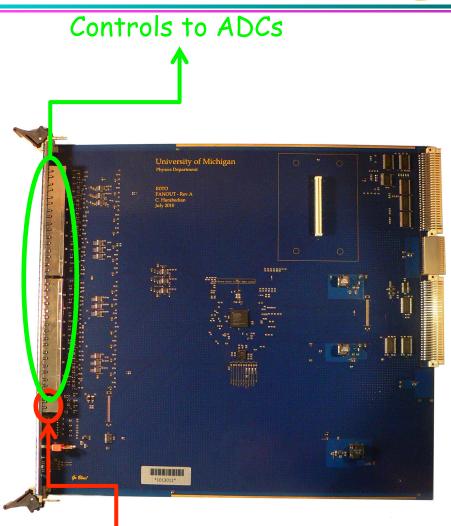








- 1-to-16 Repeater board for Controls from Mactris to one ADC Crate
- Four LVDS Controls: 3 outputs (clk, t0 and L1A), one input (ERROR)
- receives master copy via front panel RJ45
- generates 16 copies to ADCs via front panel RJ45
- Used in cascade: Master Fanout to 16 Slave Fanouts to 16 frontend Crates

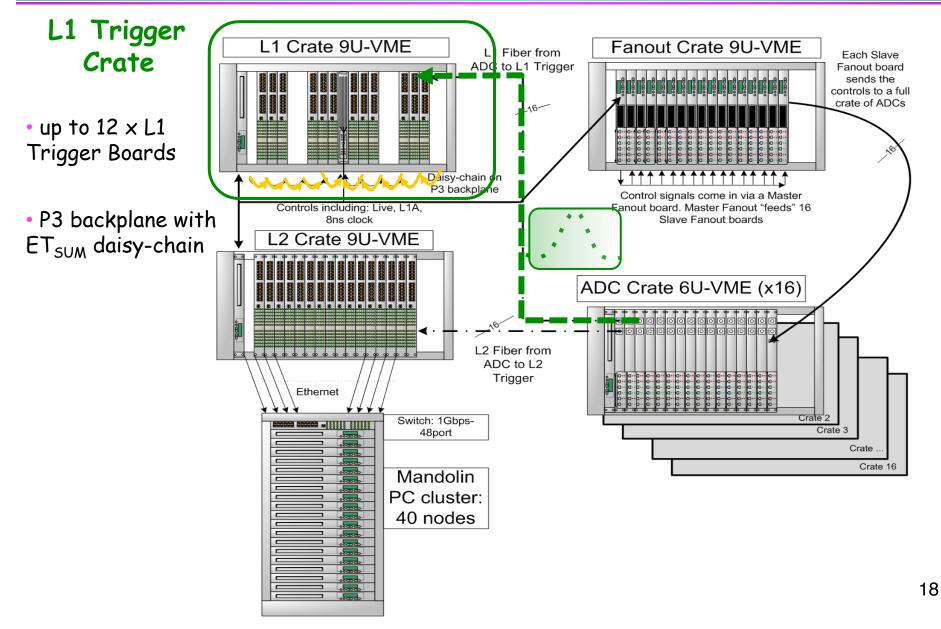


Controls from MACTRIS







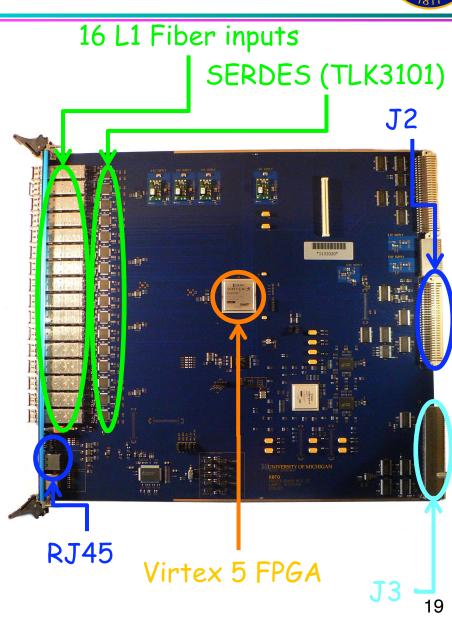




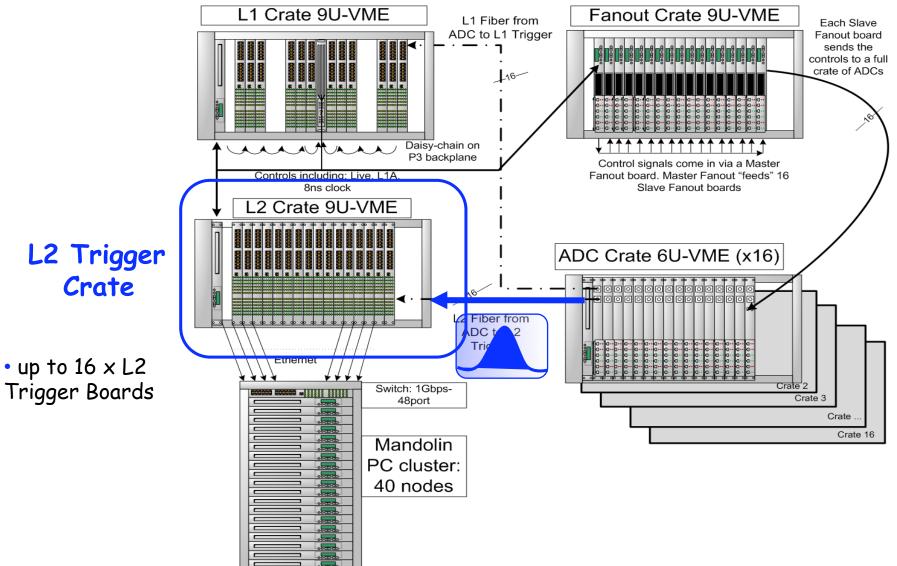
L1 Trigger Board



- 16x2.5Gbs optical fiber inputs to SERDES (Texas TLK3101)
- DAQ Controls via J2 connector or front-panel RJ45 connector
- Et_{sum} daisy-chain via J3
 backplane
- Xilinx Virtex5 FPGA:
 - align energy of 16 input fibers to system clock
 - ♦ generate ET_{SUM} for full ADC crate
 - Align local ET_{SUM} to ET_{SUM} from daisy-chain
 - ♦ VME Interface
- Clock and data bus routing are critical to avoid TLK loss-ofsync







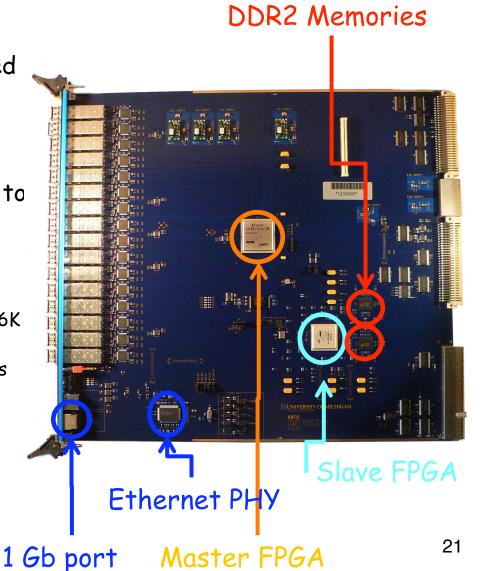


L2 Trigger Board

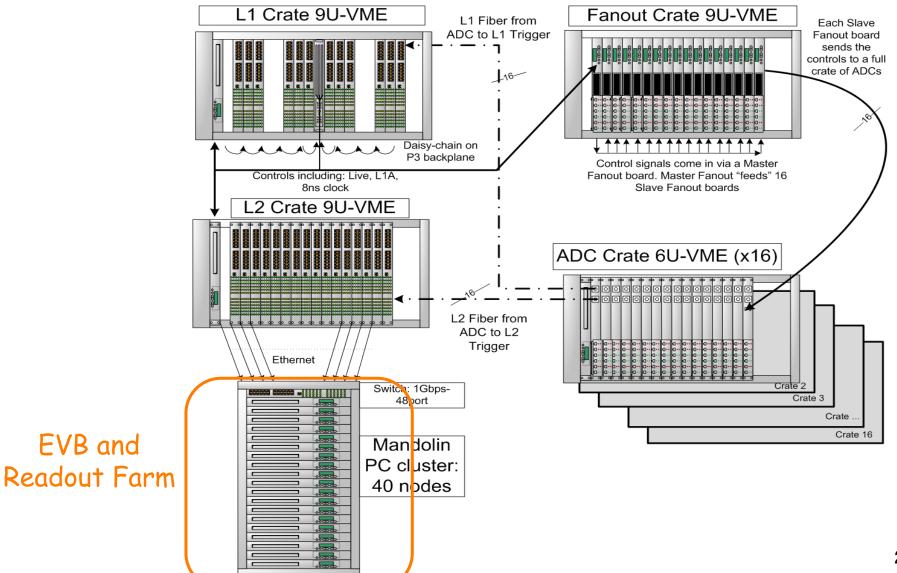


Same layout as L1 Trigger board. Unlike L1 Trigger board, it also uses:

- Xilinx Virtex 4 FPGA (slave) connected to Virtex 5 FPGA (master) via 32-bit data bus
- 2x 2Gb DDR2 memories
- Ethernet PHY and 1Gb Ethernet port to PC Farm
- Virtex5 FPGA:
 - store ADC energy after each trigger into 16K deep FIFOs
 - multiplex input fiber energy onto 32-bit bus
 - ♦ event gaussian fit logic
- Virtex4 FPGA:
 - ♦ host DDR2 memory interface
 - ♦ host Ethernet MAC interface
 - build Standard/JUMBO Ethernet packets using IP/UDP protocol













- Provides offline reconstruction, online monitoring and temporary data storage
- 41 Dell PowerEdge SC1435 servers (1 Head, 40 Clients)
 - 2 dual-core AMD Opteron 2.6-GHz processors each
 - 16 GB memory
 - two 1Gb Ethernet NIC cards
 - 250-GB system disk and 750-GB data disk each
- 48 port Dell Power Connect Layer 3 switch
 - up to 184 Gb/s capacity
 - four 10 GB ports
- Event fragments from N consecutive triggers will be routed to N separate PCs (N=16)







3000 channels of **calorimeter** readout (frontend and trigger) are completed and either delivered to Japan or under test at University of Michigan.

MC simulation requires some minimal veto trigger to keep L1 trigger rates at 120 KHz for 300 MeV Et_{SUM} threshold (assuming final K_L yield) Veto channels production

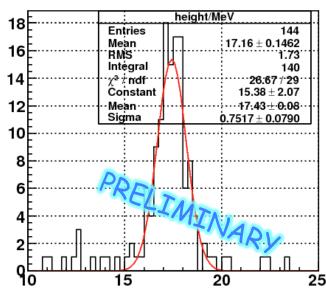
- majority will be digitized by the same 125 MHz ADC boards
- ~100 channels of beam hole photon veto (BHPV) will use 12bit/500 MHz digitization of unshaped PMT signal. Board Design ready. Waiting for funding
- L1 Trigger board under design. Waiting for funding.
- L2 Trigger/Readout board common to whole system. FPGA and software under development.



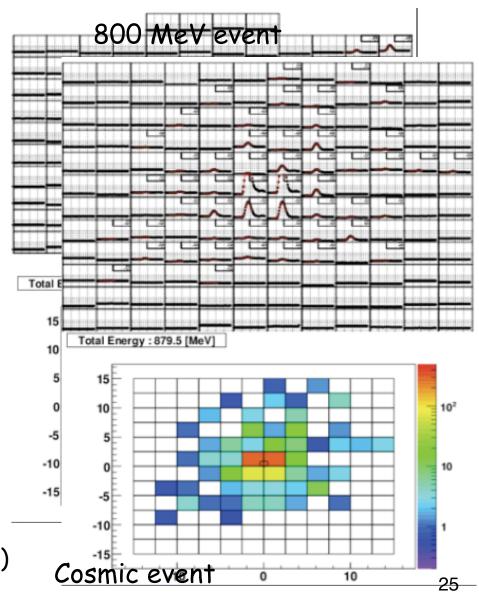




- 12x12 calorimeter channel beam tests were done at LNS Electron/Photon beam in 2010:
- check of analog readout performance
- test of trigger/DAQ chain with prototype boards



Gaussian height calibration (cnt/MeV)

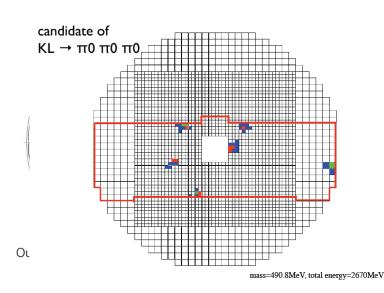


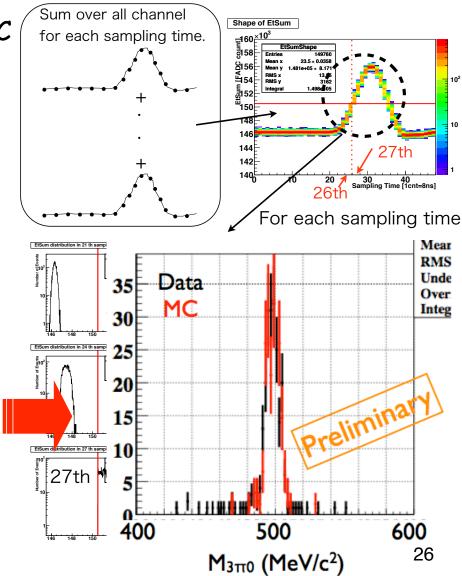




Partial (~1800 Csi crystals) calorimeter test was done in JPARC using final beam line in Dec. 2010 (with upstream tracking chambers in magnetic field)

- ADCs readout via VME to Mandolin cluster
- ET_{SUM} trigger using 90 channels
- reconstructed K_L mass from K_L $\rightarrow \pi^+\pi^-\pi^0$ and K_L $\rightarrow \pi^0\pi^0\pi^0$ decays











- Before March 11 Earthquake, schedule had full detector run in Dec.
 2011, followed by physics run aiming to reach GN limit in Spring 2012
- Earthquake/tsunami created no major visible damage to accelerator or K_L beam line or KOTO detector. Tests still under way.
- On May 20th, JPARC posted a recovery plan with the goals of:
 - 1) start beam commissioning in Dec. 2011 with beam in instanting to conf











- KOTO experiment is to discover $K_L \rightarrow \pi^0 v v$
- New Trigger & DAQ built to comply with physics requirements of:
 - pipelined readout and trigger electronics with no deadtime
 - 14-bit dynamic range on the energy measurement
 - time resolution of 0.5 nsec
- New beamline at JPARC 30 GeV proton accelarator plus upgraded detector ready to take data by end of 2012



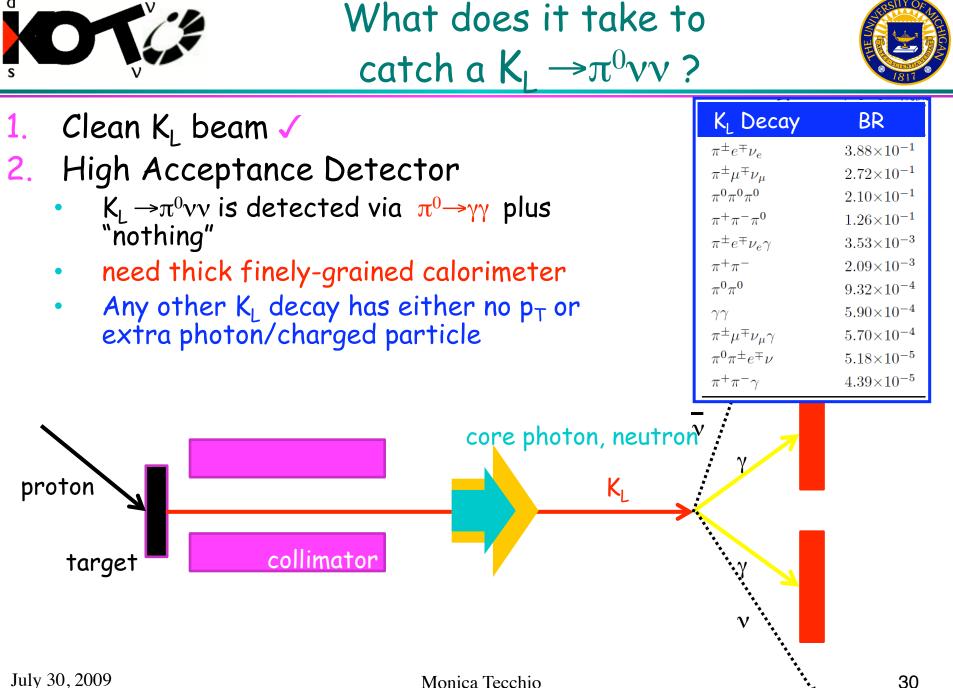


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Backups

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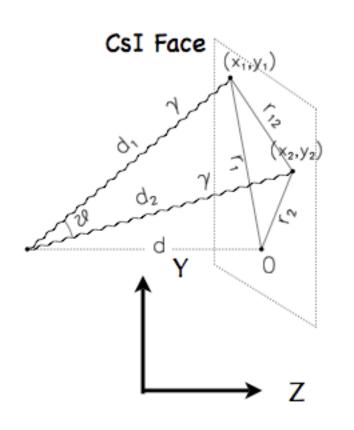
Monica Tecchio

$K_L \rightarrow \pi^0 v v$ Reconstruction



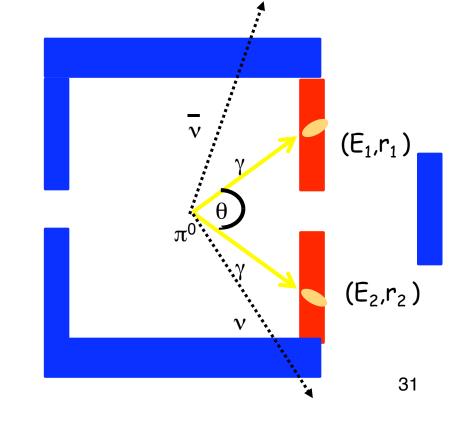
Fully reconstruct $K_L \rightarrow \pi^0 v v$ kinematics

- calorimeter gives γ energy and position
- by constraining 2γ system to π^0 mass, get the two photon opening angle θ
- assuming K decay vertex on beam line, determine Z_{vtx} of π^0 decay



$$m_\pi^2 = \left(p_{\gamma_1} + p_{\gamma_2}
ight)^2 = 2\,E_1\,E_2 imes\left(1-\cos\, heta
ight)$$
 $r_{12}^2 = d_1^2 + d_2^2 - 2\,d_1\,d_2\cos\, heta$

NB: E
$$\propto$$
 1/ θ while m $\propto \theta$





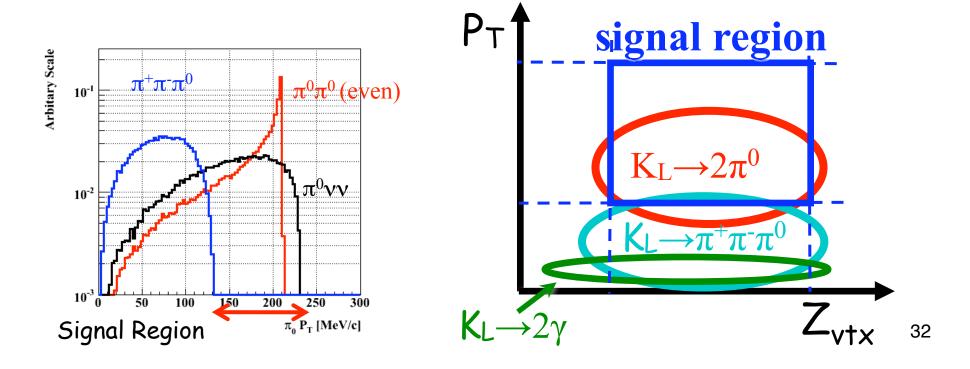




Identify kaon backgrounds

- define signal box in $\pi^0 P_T$ -Z_{vtx} using:
 - fiduciality cuts for Z_{vtx}
 - P_T above $K_{\pi3}$ threshold and above (V-A) maximum of 231 MeV/c
- no activity in vetoes

- kaon decays w/w.o. particles escaping detection:
 - low P_T or Z shifted upstream
 - have unphysical γ
 (E-θ) relation
 - larger 2γ energy ratio
 - fused clusters with wrong e.m. shower profile









Basic experimental method is sound: BR < 2.6×10-8 (at 90%CL). Need to improve ×10³!

	кото	E391a (Run2)	
Proton energy	30 GeV	12 GeV	
Proton intensity	2e ¹⁴	2.5e ¹²	
Spill/cycle	0.7/3.3sec	2/4sec	
Extraction Angle	16 deg	4 deg	
Solid Angle	9µStr	12.6µStr	
K _L yield/spill	8.1e ⁶	3.3e ⁵	x25
Run Time	12 months/ (3 Snowmass years)	1 month	×10
Decay Prob.	4%	2%	x2
Acceptance	3.6%	0.67%	×5