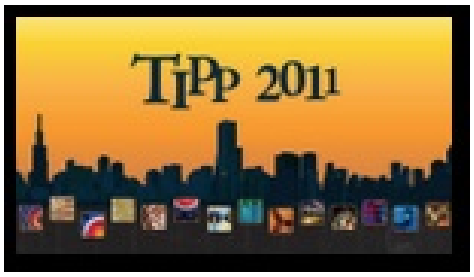

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Deeper Sampling CMOS Transient Waveform Recording ASICs

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Many applications in collider detector readout and particle astrophysics have adopted CMOS Switched Capacitor Array (SCA), Giga-sample/second transient waveform recording as a means to provide low-cost, highly integrated detector readout. In order to maintain high (100's of MHz) analog bandwidth, these SCAs have typically been limited to less than or equal to a thousand storage cells. However, for applications requiring many microseconds to form a detector trigger, or cases where the physical transit time of a signal across the detector array at the speed of light is 10's or even 100's or microseconds, an alternative is needed. In the BLAB3 and IRS ASIC architectures, a so-called 2-stage transfer mechanism has been adopted. This technique provides a small "sampling" array on the front-end of the ASIC, and buffered signals are then transferred to a much larger analog "storage" array. By this means ˜1M storage cells can be accommodated in a standard 0.25um CMOS process, the maximum being set by reticle limits on die size. Two generations of ASICs both with and without input amplifiers have been fabricated and evaluated and the results will be presented.

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