Introduction to PANDA Trigger and Data Acquisition System

Hao Xu
Hao.Xu@ihep.ac.cn
Institute of High Energy Physics, CAS, China
for the PANDA Collaboration

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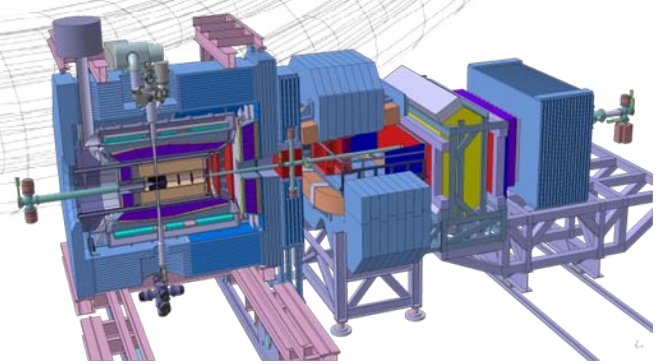

Agenda

- PANDA@FAIR overview
- The trigger-less DAQ system for PANDA
- DAQ demonstrator system for EMC
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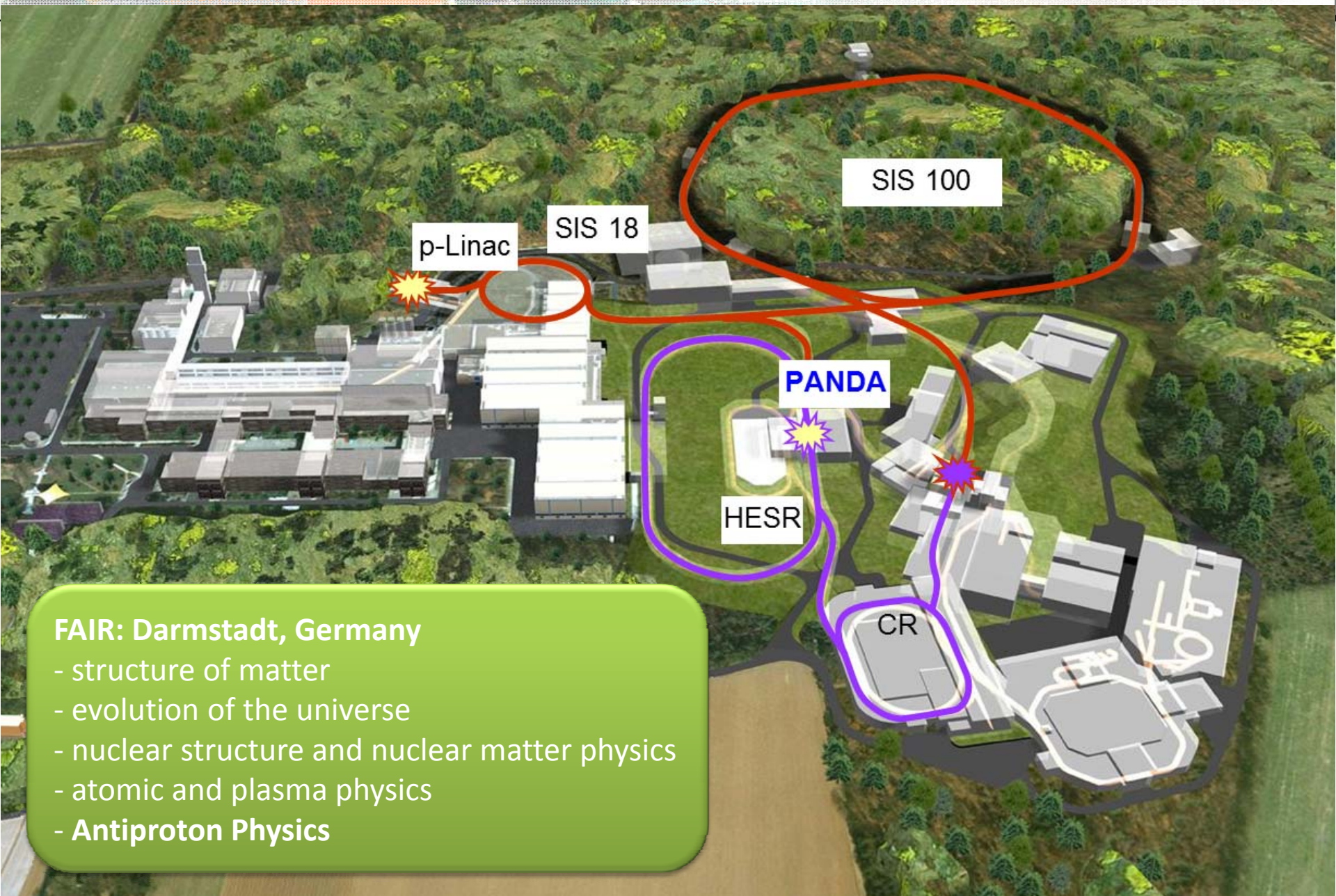
FAIR: Facility for Antiproton and Ion Research

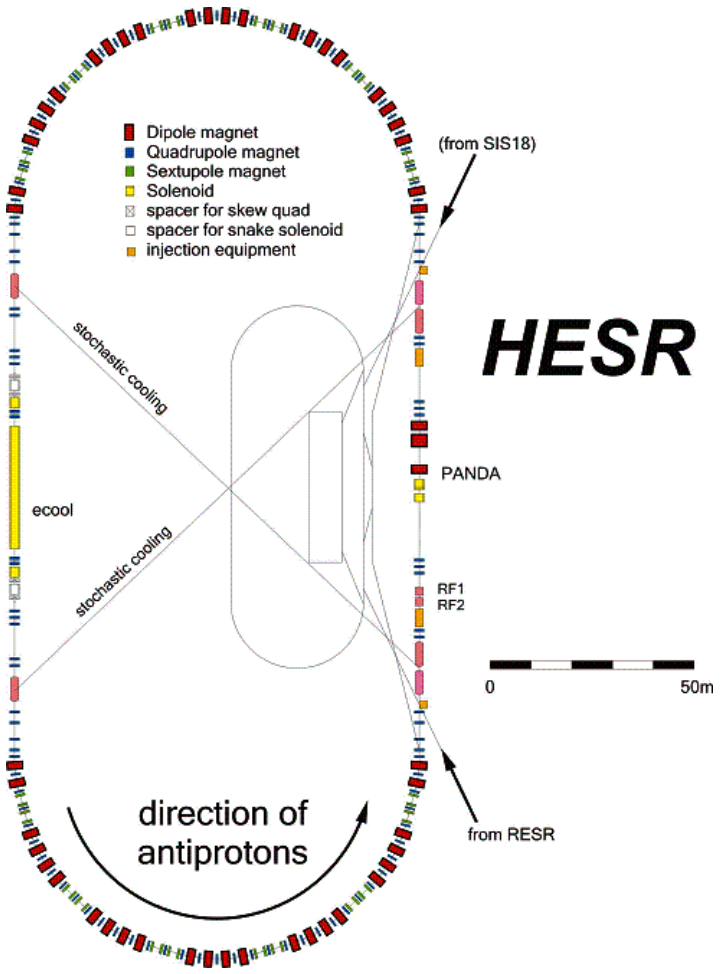


FAIR: Darmstadt, Germany

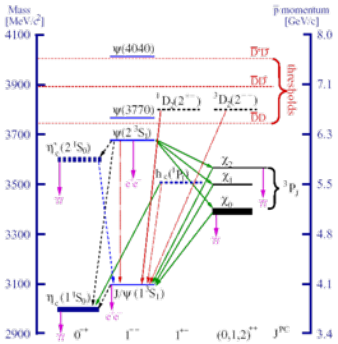
- structure of matter
- evolution of the universe
- nuclear structure and nuclear matter physics
- atomic and plasma physics
- **Antiproton Physics**

High Energy Storage Ring

- Parameter
  - Injection of pbar at 3.7 GeV
  - Slow synchrotron (1.5-15.0 GeV/c)
  - Storage ring for internal target operation
  - Luminosity up to L~ $2x10^{32}$ $cm^{-2}s^{-1}$
  - Beam cooling (stochastic & electron)

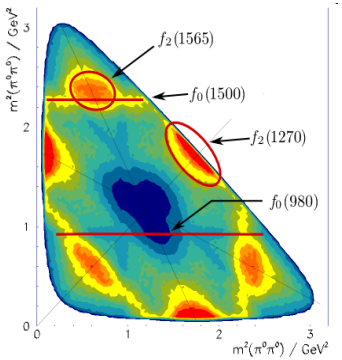


Physics Program



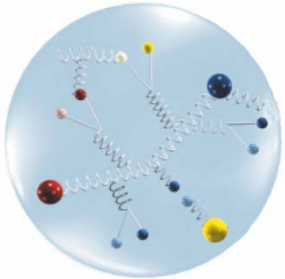
Charmonium Spectroscopy

Precision Spectroscopy
Study of Confinement Potential
Access to all these puzzling X,Y,and Z



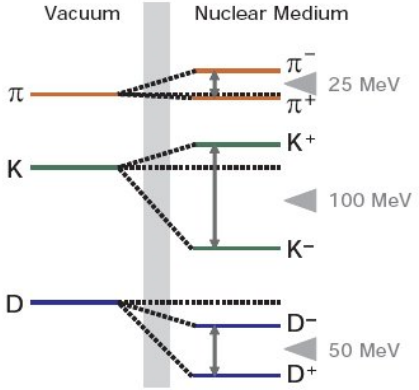
Search for Exotics

Look for Glueballs and Hybrids
Gluon rich environment
Disentangle Mixing via PWA



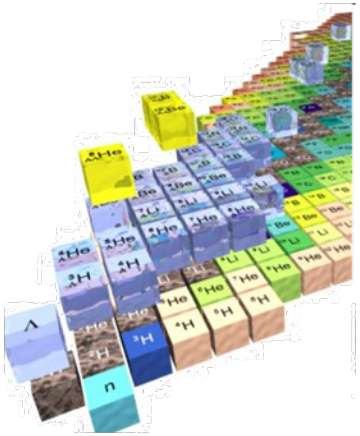
Nucleon Structure

Generalized Parton Distribution
Timelike Form Factor of the Proton
Drell-Yan Process



Charm in Medium

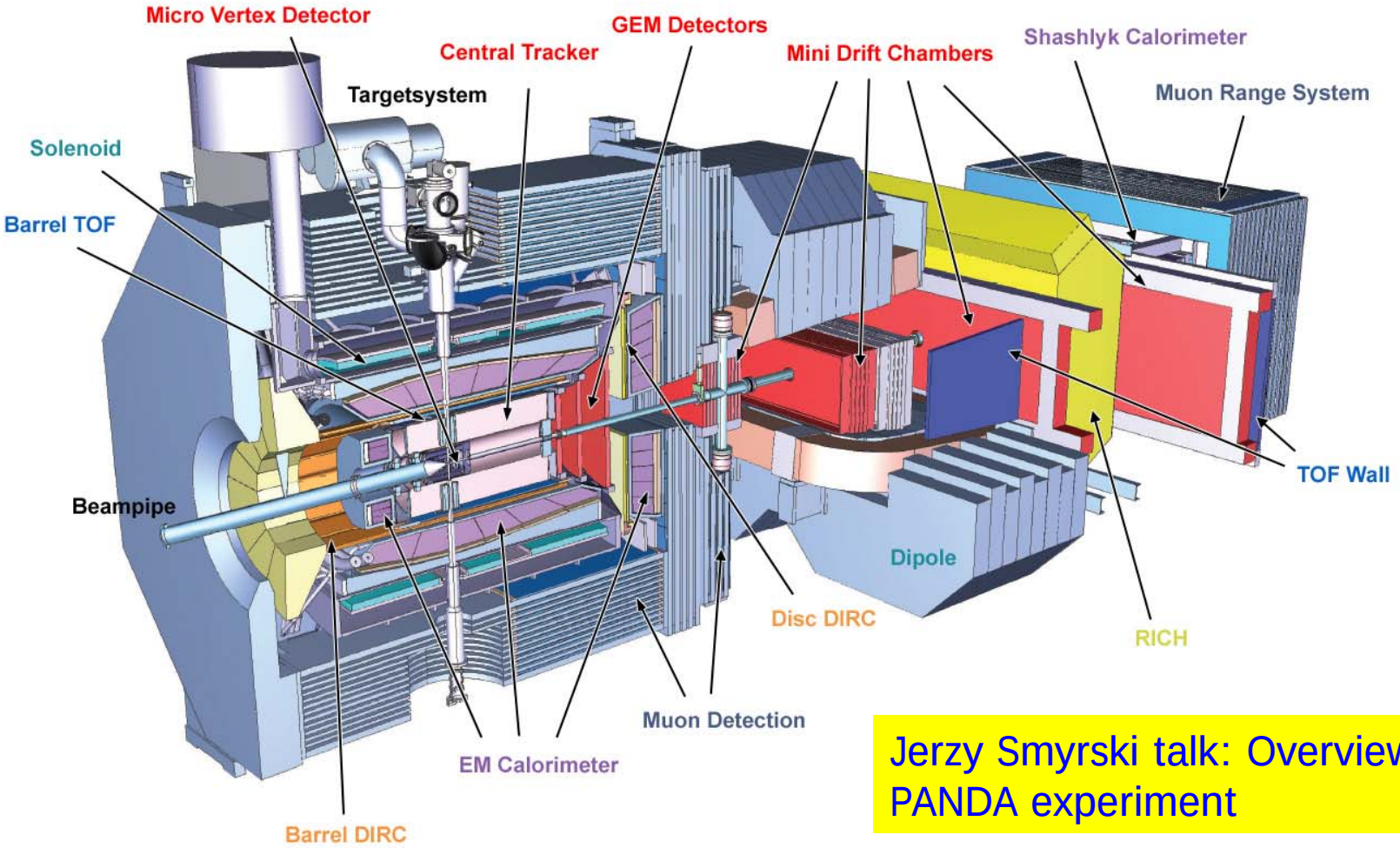
Study in-medium modification
of Hadrons



S=2 Hypernuclei

Nuclear structure
Baryon-Baryon interaction in $SU(3)_f$
H-dibaryon

PANDA Detector



Jerzy Smyrski talk: Overview of the PANDA experiment

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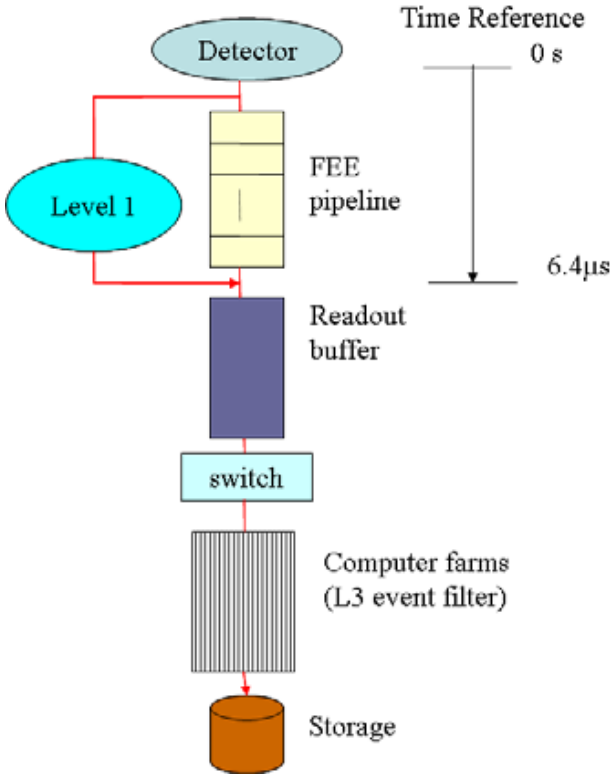
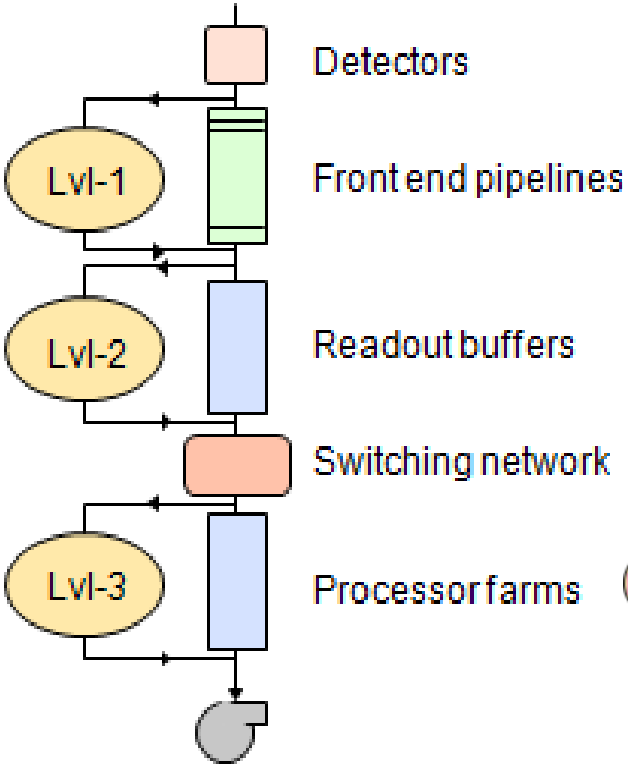
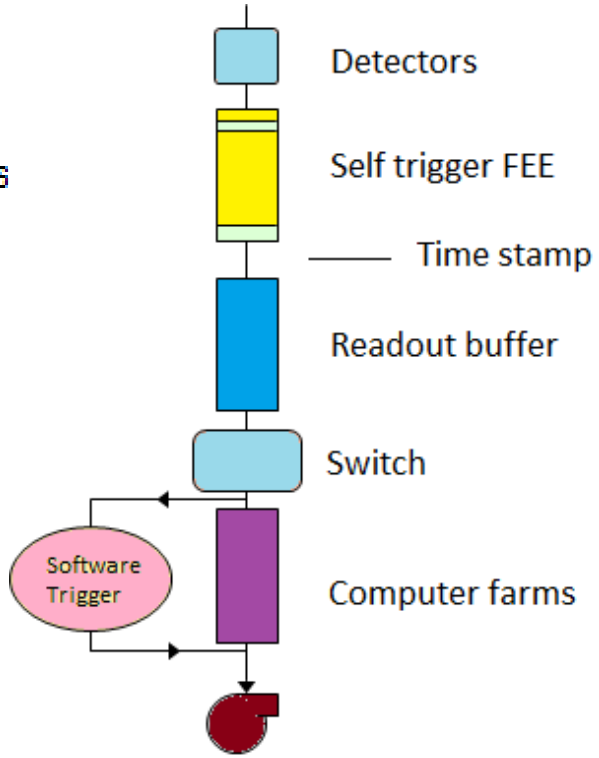
The Trigger-less DAQ







BESIII ***ATLAS, LHCb*** ***PANDA***

Trigger-less DAQ

- No external signal to initiate readout
- Continuous sampling readout
  - Front-End identify detector signals
- Event selection: Online Data Processor (FPGA, DSP, CPU,GPU…)
- Advantage
  - No hardware trigger logic
  - Flexible
- Draw backs
  - No event definition at readout stage
  - No T0
  - Higher data rate

Motivation for Trigger-less DAQ

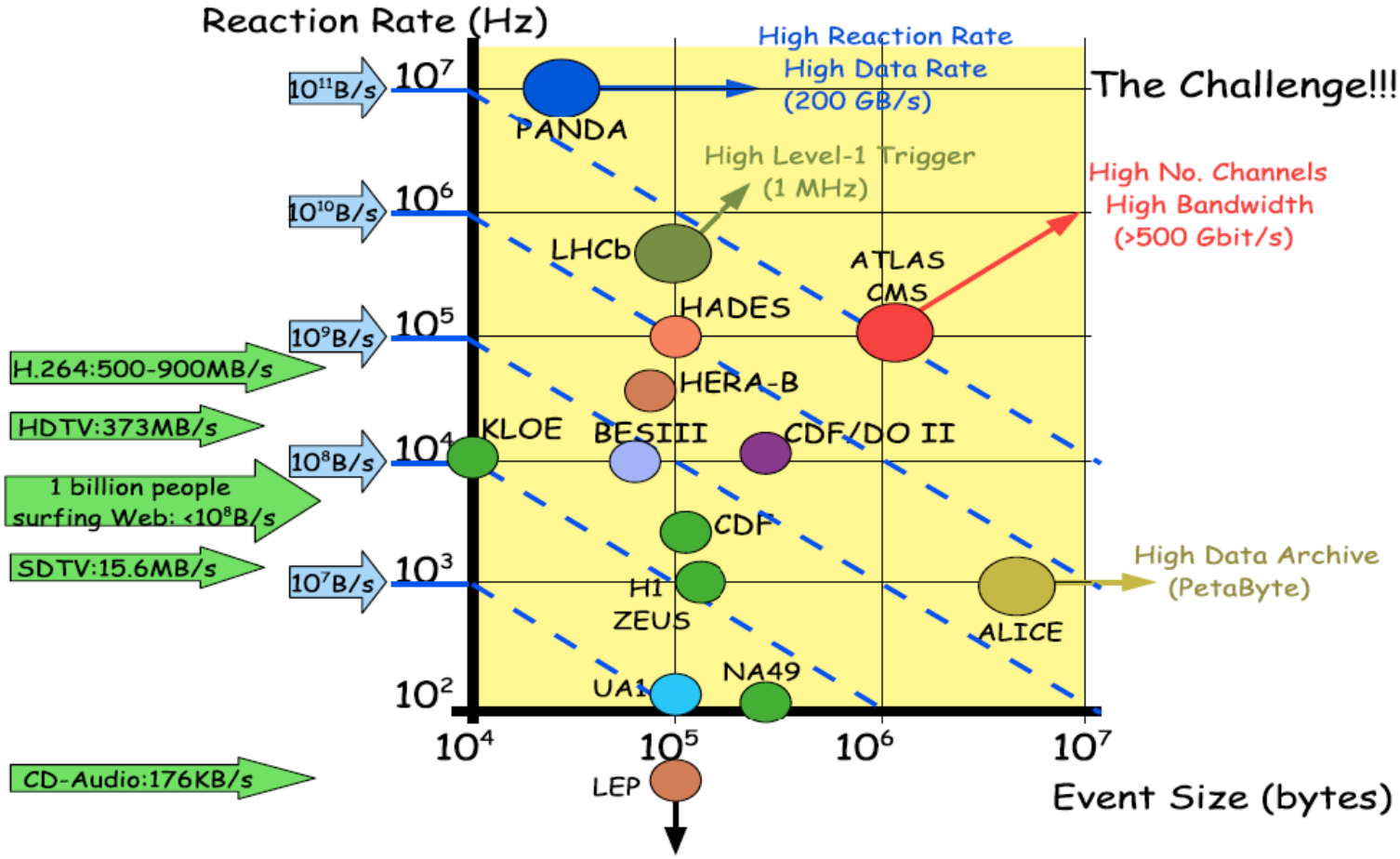
- Wide physics cases – different criteria for event selection
- Complicated event selection criteria
  - Identification of short lived particles - Impact Parameter
  - photon clusters in EMC with veto of charged particles in front e.g.ηc
  - Electron identification
  - Particle ID in MVD, TPC/Straw detectors (dE/dX)
  - Cherenkov PID
  - Λ reconstruction
  - Muon Identification
  - …

Almost every detector is needed for event selection

Design Challenges

- Interaction rates up to 30MHz
- typical event sizes 4 - 20 kB.
- data rates after front end preprocessing: 40GB/s - 200 GB/s
- high flexibility and selectivity

Data Rate and Event Size

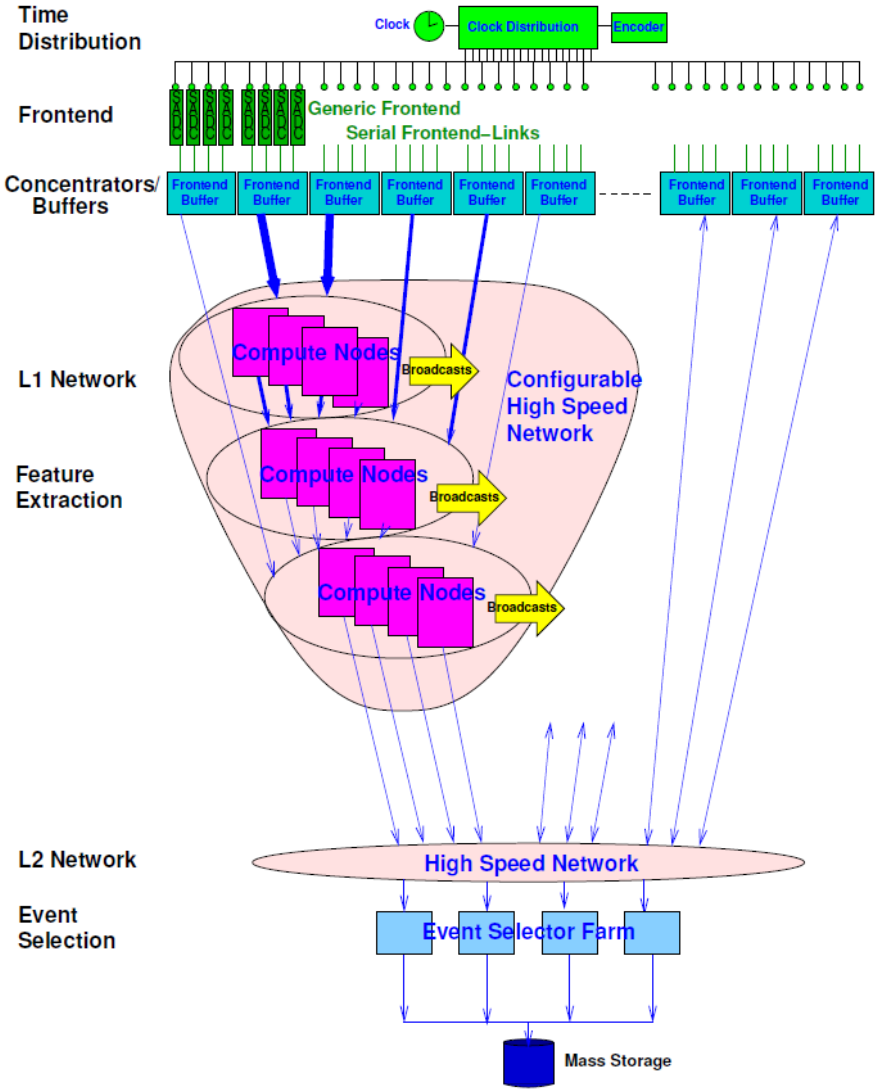


Solution

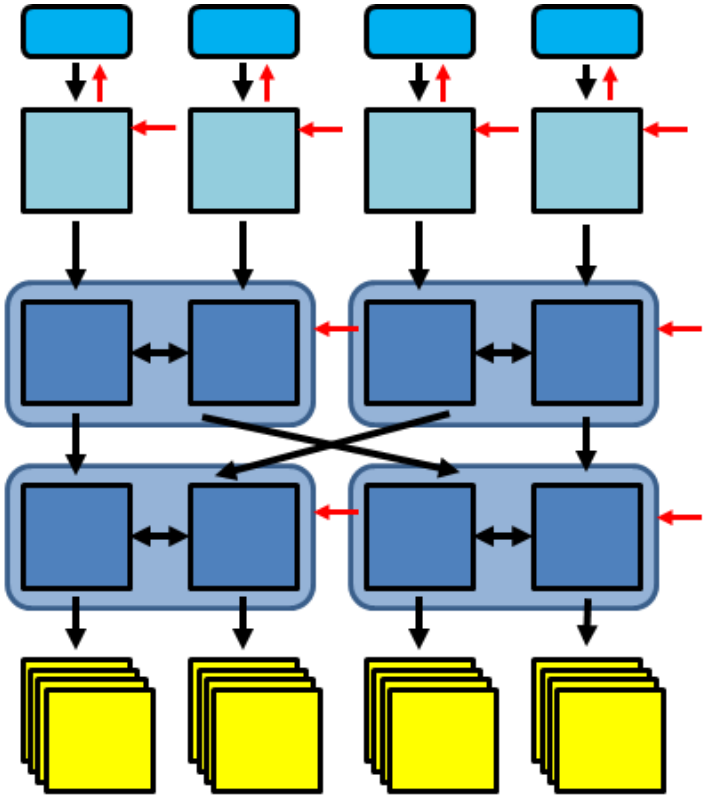
- continuously sampling data acquisition
- hardware trigger-less
- Precision clock distribution system

- Digital signal processing at FrontEnd level
- Event selection in programmable processing units
- Connection via high speed networks

System Architecture



Processing Steps



Detector Front-ends FEE-Data concentrator
- Feature extraction : time & amplitude
- Clusterization
- Data Zero suppression

Data Concentrator

First Stage "Event" Builder

Burst builder
- Combines data : one burst - one data block

Second Stage "Event" Builder

Compute Node

Compute Node, Computer farms
- Online data processing
- Accept/reject decision

Data links

Time distribution (via optical link)

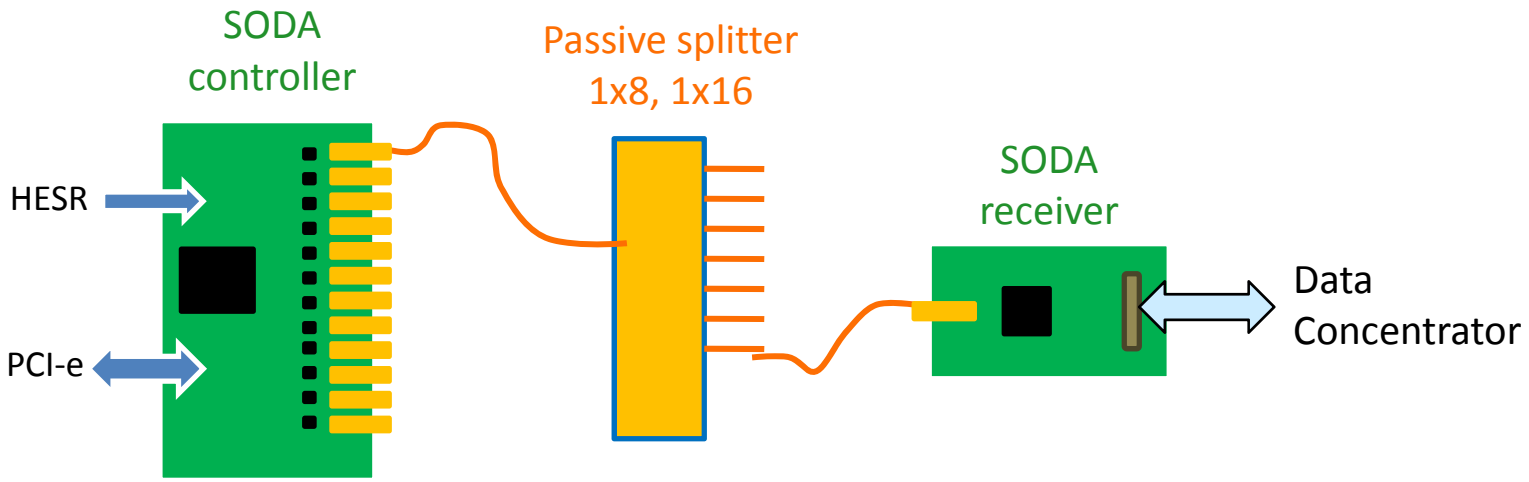
Key technologies

- SODA: Synchronization Of Data Acquisition
  - Time distribution system
- Compute Node: the ‘heart’ of T/DAQ system
  - Event filter/event selection/…

SODA Functionality

- Provision of clock reference < 20ps
- Synchronization with HESR operation
  - Burst or super burst
- Monitoring status of FE and DAQ components
- Data flow control
  - Define switch topology

SODA Architecture



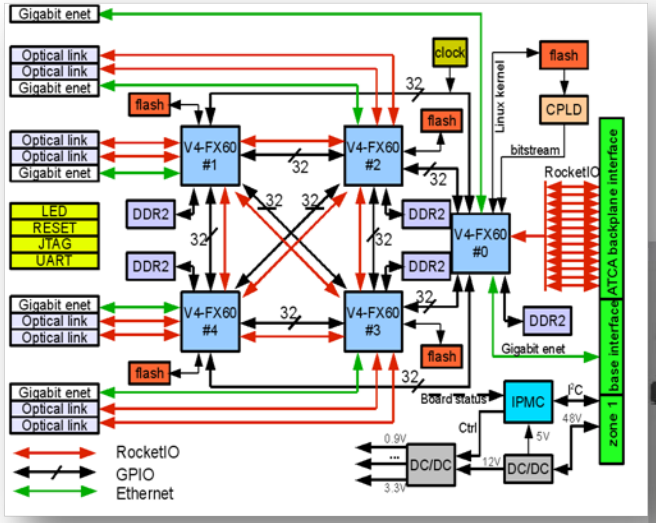
SODA controller : Broadcast synchronous commands with fixed latency. PCI-express interface to PC

Optical splitter : 1x8; 1x16; 1x32

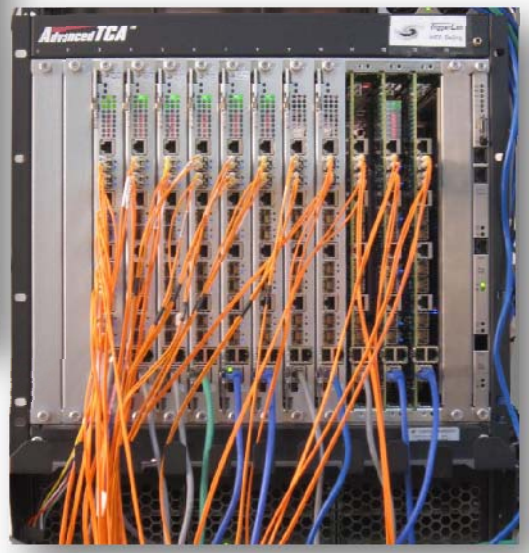
SODA receiver: Mounted directly on Data Concentrator module

* I. Konorov, "SODA: Time distribution system for the PANDA experiment ", Nucclear Science Symposium Conference Record (NSS/MIC), 2009 IEEE

Compute Node



5x Virtex-4 FX60-10/-11 FPGA
13x 2/3.125Gbps to backplane for interconnection
5x Gigabit Ethernet
8x 2/6.25Gbps Optical Links for data input
2 GB 400MHz DDR2 SDRAM
Real time Linux/vxworks

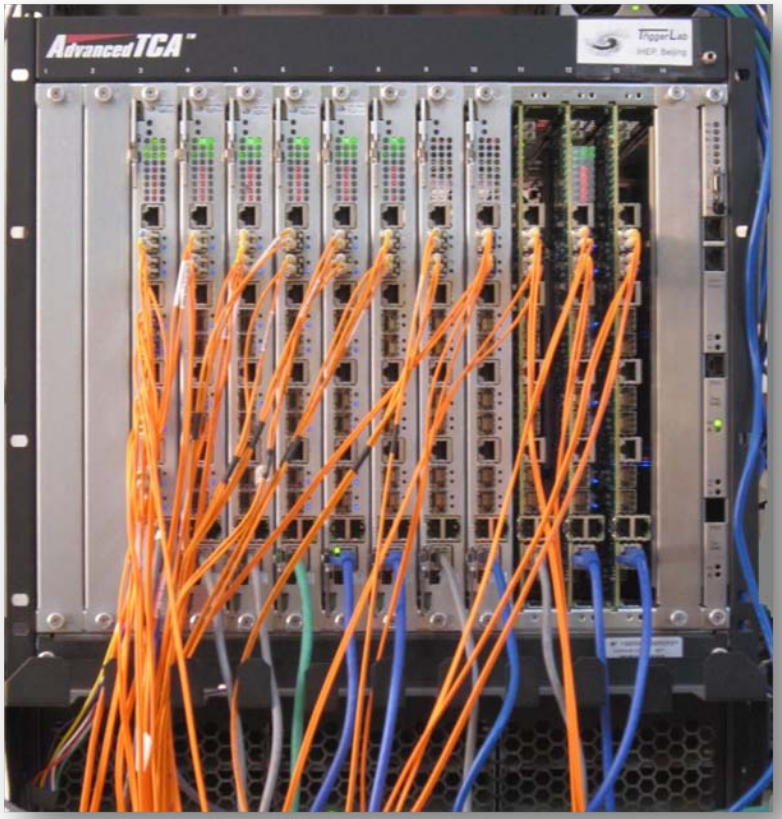


An universal high performance platform prepared for multiple applications .
ATCA standard (Full Mesh topology in backplane) and FPGA-based

Hao Xu talk: An ATCA-based High Performance Compute Node for Trigger and Data Acquisition in Large Experiments

Production for Development

- 10 boards production for performance test and Example firmware development
  - 3 boards assembled with virtex4 fx60-11 for SFP+
    - Optical link
      - 6.25Gbps
    - DDR2 SDRAM
      - 200MHz for MPLB
  - 7 boards assembled with virtex4 fx60-10 for SFP
    - Optical link
      - 2 Gbps
    - DDR2 SDRAM
      - 100MHz for MPLB



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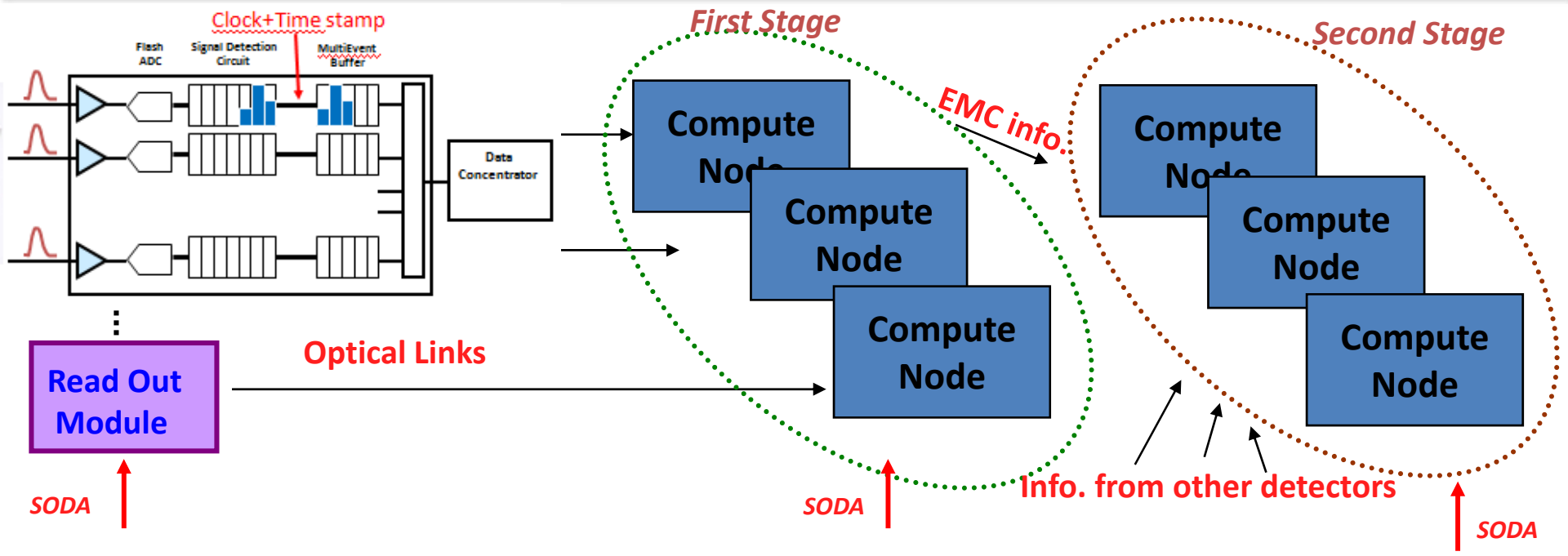
DAQ Demonstrator System for EMC

- Goal
  - Set up a basic system that can be interfaced to the FEE
  - Input from FEE
  - via optical fibre (2 /6Gbps)
  - GBit Ethernet
- Functionality
  - Up to 8 fibres per CN module
    - up to 14 CN Modules
  - (4+1) V4FX60 FPGAs per CN module
  - Firmware for data transport from FEE and to PC farm
  - Firmware for EMC cluster finding

EMC T/DAQ Schematic

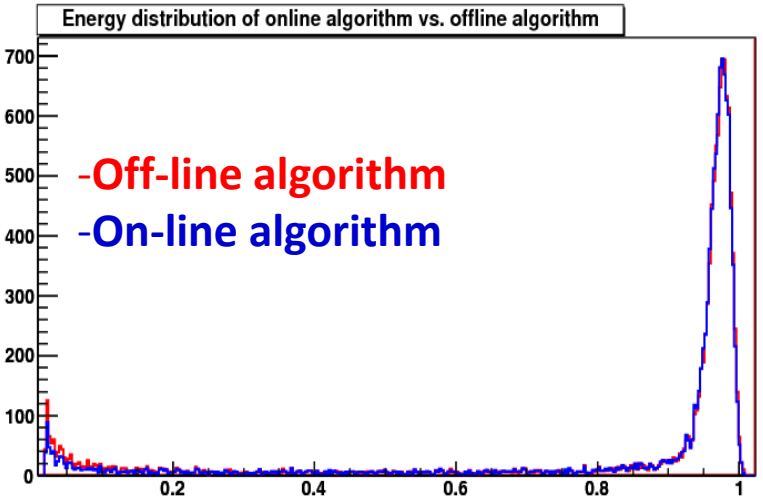


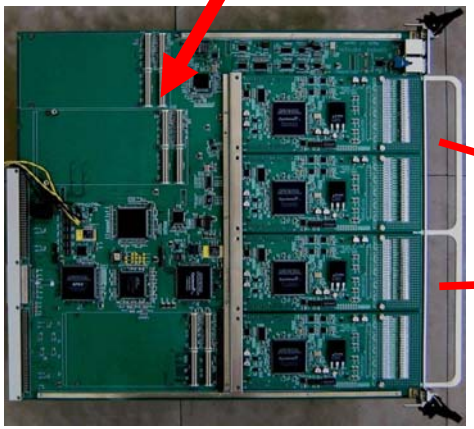
Tasks

1. Signal Feature extraction (Time, Amplitude) 2. Data Zero suppression 3. Precision time stamp	1. Clustering 2. Cluster Properties extraction 3. Pattern recognition	1. Correlation 2. Physical parameters calculation 3. Event building

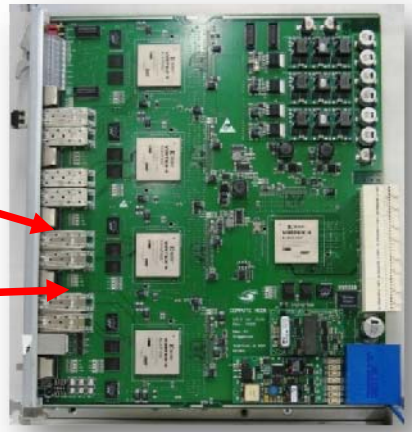
Test Setup

NFS Server
(data source)





Interface card



Compute node

NFS Server
(On-line processed data)

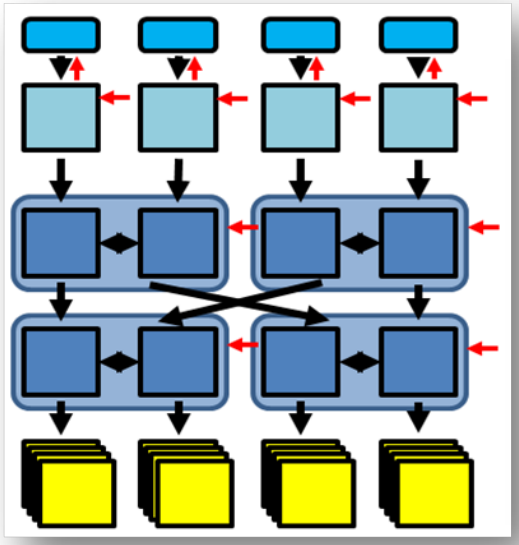
Simulation and Off-line Software

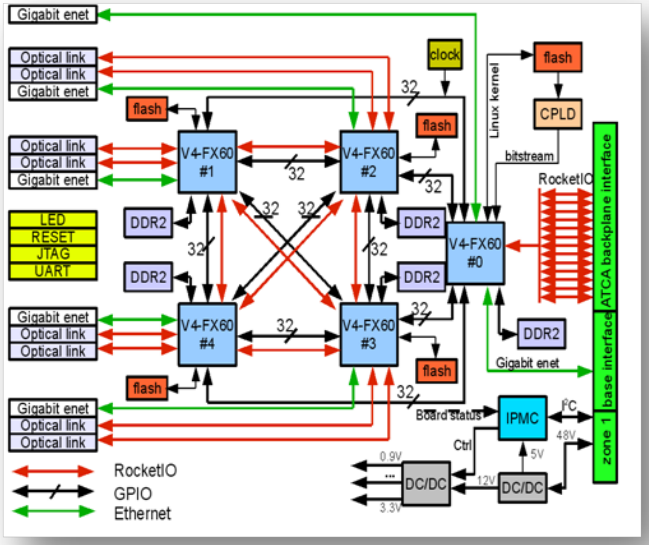
- In order to find best event-selection criteria software simulations are required
- Transition of event-based → time ordered Monte-Carlo simulation is necessary
- The PandaRoot is being modified

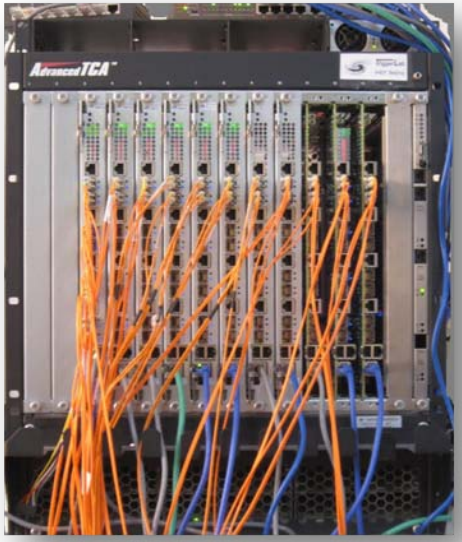
Summary

- PANDA trigger-less DAQ system is a very challenging and promising development and the only feasible way to achieve physics goals of PANDA experiment
- Implementation of a trigger-less DAQ system requires completely new development of hardware and software
- The ATCA-based Compute Nodes are produced and successfully tested
- The simulation and off-line data-analysis tool-chain is being adapted to the trigger-less DAQ concept.
- The prototype of PANDA EMC Trigger and Data Acquisition System under construction

Thank you for your attention







Who's involved in PANDA?

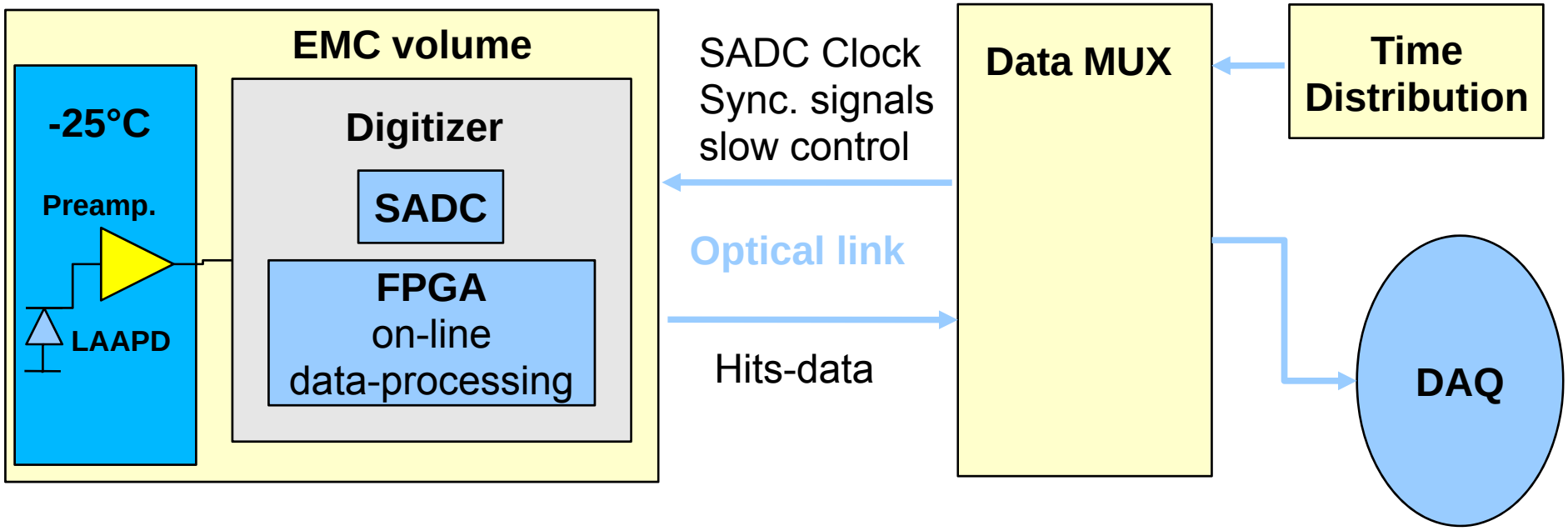
More than 400 physicists from 53 institutions in 16 countries

U Basel
IHEP Beijing
U Bochum
IIT Bombay
U Bonn
IFIN-HH Bucharest
U & INFN Brescia
U & INFN Catania
JU Cracow
TU Cracow
IFJ PAN Cracow
GSI Darmstadt
TU Dresden
JINR Dubna
(LIT,LPP,VBLHE)
U Edinburgh
U Erlangen
NWU Evanston

U & INFN Ferrara
U Frankfurt
LNF-INFN Frascati
U & INFN Genova
U Glasgow
U Gießen
KVI Groningen
IKP Jülich I + II
U Katowice
IMP Lanzhou
U Lund
U Mainz
U Minsk
ITEP Moscow
MPEI Moscow
TU München
U Münster
BINP Novosibirsk

IPN Orsay
U & INFN Pavia
IHEP Protvino
PNPI Gatchina
U of Silesia
U Stockholm
KTH Stockholm
U & INFN Torino
Politechnico di Torino
U & INFN Trieste
U Tübingen
TSL Uppsala
U Uppsala
U Valencia
SMI Vienna
SINS Warsaw
TU Warsaw

Read-out chain concept



Status of development:

- First prototypes of Digitizer available: developed at University of Uppsala
- Data-processing algorithm implemented in VHDL and in the testing/tuning phase
- Optical-link protocols are being developed (hit-data transfer, SADC clock transfer, time-synchronisation)
- First demonstrator ready – autumn 2011

EMC Readout

- Continuous data sampling with sampling ADC
- On-line data-processing
  - Digital filtering
  - On-line pile-up recovery
- Hit detection and feature-extraction (energy, timestamp)
- Timestamp