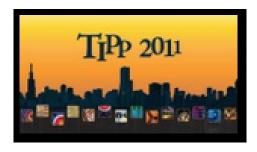
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The GANDALF Multi-Channel Time-to-Digital Converter (TDC)

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The GANDALF 6U-VME64x/VXS module [1,2] has been designed to cope with a variety of readout tasks in high energy and nuclear physics experiments. The exchangeable mezzanine cards allow an employment of the system in very different applications such as analog-to-digital or time-to-digital conversions, coincidence matrix formation, fast pattern recognition or fast trigger generation.

Based on this platform, we present a 128-channel TDC which is implemented in a single Xilinx Virtex-5 FPGA using a shifted-clock sampling method. In this concept each input signal is continuously sampled by eight flip-flops with equidistant phase-shifted clocks. Predictable placement of the logic components and uniform routing inside the FPGA fabric is a particular challenge of this design. We present measurement results for the time resolution, the nonlinearity and the rate capability of the TDC readout system. This project is supported by BMBF and EU FP7.

[1] S. Bartknecht et al., "Development of a 1 GS/s high-resolution sampling ADC system," Nucl. Instr. and Meth. A, vol. 623, pp. 507-509, 2010.

[2] S. Bartknecht et al., "Development and Performance Verification of the GANDALF High-Resolution Transient Recorder System," accepted for publication in IEEE Trans. Nucl. Sci.

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